ZL30145

SyncE (10 GbE) SONET/SDH Rate Conversion and Jitter Attenuator PLL

Data Sheet

March 2013

Features

- Can be used in systems to support the requirements of ITU-T G.8262 for synchronous Ethernet Equipment slave Clocks (EEC option 1 and 2)
- Meets jitter generation requirements of Telcordia GR-253-CORE for OC-192, OC-48, OC-12 and OC-3 rates
- Meets jitter generation requirements of ITU-T G.813 for STM-64, STM-16, STM-4 and STM-1 rates
- Synchronizes to standard telecom or Ethernet clock and provides jitter filtered output clock for SONET/SDH and Synchronous Ethernet line cards
- Synchronizes to telecom reference clocks (2 kHz, N*8 kHz up to 77.76 MHz, 155.52 MHz) or to Ethernet reference clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz)
- Generates standard SONET/SDH clock rates (e.g., 19.44 MHz, 38.88 MHz, 77.76 MHz, 155.52 MHz, 622.08 MHz) or Ethernet clock rates (e.g., 25 MHz, 50 MHz, 125 MHz, 156.25 MHz, 312.5 MHz) for synchronizing Ethernet PHYs
- Selectable loop bandwidth of 14 Hz, 28 Hz, or 890 Hz

Ordering Information

ZL30145GGG	64 Pin CABGA	Trays
ZL30145GGG2	64 Pin CABGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Configurable through a serial interface (SPI or I^2C)
- DPLL can be configured to provide synchronous or asynchronous clock outputs
- Supports IEEE 1149.1 JTAG Boundary Scan

Applications

- ITU-T G.8262 Line Cards which support 1 GbE and 10 GbE interfaces
- SONET line cards up to OC-192
- SDH line cards up to STM-64

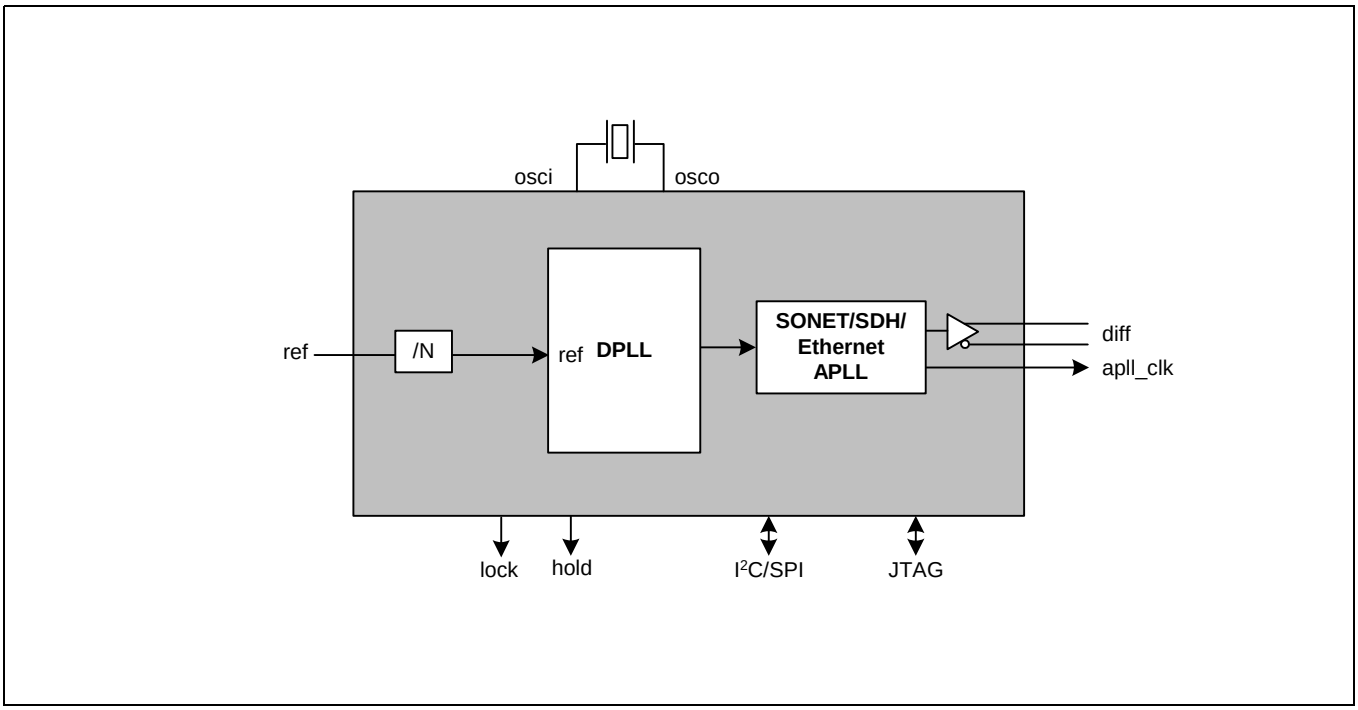

Figure 1 - Simplified Functional Block Diagram

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Change Summary

The following table captures changes from July 2009 issue to March 2013 issue.

Page	Item	Change
Multiple	Zarlink logo and name reference	Updated to Microsemi® logo and name.

Below are the changes from the February 2009 issue to the July 2009 issue.

Page	Item	Change
18	2.6, “Reference Monitoring for Custom Configurations“	Added instructions for SCM and CFM limits when using low frequency customs frequencies.
21	2.7, “Output Clocks“	Added reference to ZLAN-254.

Pin Description

Pin #	Name	I/O Type	Description
Input Reference			
B1	ref	I_u	**Input References (LVCMOS, Schmitt Trigger).** This input reference is available to the DPLL for synchronizing output clocks. It can lock to any multiple of 8 kHz up to 77.76 MHz including 25 MHz and 50 MHz. It has additional configurable pre-dividers allowing input frequencies of 62.5 MHz,125 MHz or 155.52 MHz. This pin is internally pulled up to V_{dd}.
Output Clocks and Frame Pulses			
A7 B8	diff_p diff_n	O	**Differential Output Clock (LVPECL).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks (6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz). When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks (25 MHz, 50 MHz, 62.5 MHz, 125 MHz, 156.25 MHz, 312.5 MHz). See “Output Clocks” on page 21 for more details on clock frequency settings. The default frequency for this output is 622.08 MHz.
D8	apll_clk	O	**APLL Output Clock (LVCMOS).** When in SONET/SDH mode, this output can be configured to provide any one of the available SONET/SDH clocks up to 77.76 MHz. When in Ethernet mode, this output can be configured to provide any of the Ethernet clocks up to 125 MHz. See “Output Clocks” on page 21 for more details on clock frequency settings. The default frequency for this output is 77.76 MHz.
Control			
G5	rst_b	I	**Reset (LVCMOS, Schmitt Trigger).** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. Reset should be asserted for a minimum of 300 ns.
B3	diff_en	I_u	**Differential Output Enable (LVCMOS, Schmitt Trigger).** When set high, the differential LVPECL output driver is enabled. When set low, the differential driver is tristated reducing power consumption. This pin is internally pulled up to Vdd.
Status			
E1	lock	O	**Lock Indicator (LVCMOS).** This is the lock indicator pin for DPLL. This output goes high when the DPLL’s output is frequency and phase locked to the input reference.
H1	hold	O	**Holdover Indicator (LVCMOS).** This pin goes high when the DPLL enters the the holdover mode.

Pin #	Name	I/O Type	Description
Serial Interface			
C1	sck_scl	I/B	**Clock for Serial Interface (LVCMOS).** Serial interface clock. When i2c_en = 0, this pin acts as the sck pin for the serial interface. When i2c_en = 1, this pin acts as the scl pin (bidirectional) for the I^2C interface.
D2	si_sda	I/B	**Serial Interface Input (LVCMOS).** Serial interface data pin. When i2c_en = 0, this pin acts as the si pin for the serial interface. When i2c_en = 1, this pin acts as the sda pin (bidirectional) for the I^2C interface.
D1	so	O	**Serial Interface Output (LVCMOS).** Serial interface data output. When i2c_en = 0, this pin acts as the so pin for the serial interface. When i2c_en = 1, this pin is unused and should be left unconnected.
C2	cs_b_asel0	I_u	**Chip Select for SPI/Address Select 0 for I^2C (LVCMOS).** When i2c_en = 0, this pin acts as the chip select pin (active low) for the serial interface. When i2c_en = 1, this pin acts as the asel0 pin for the I^2C interface.
E2	int_b	O	**Interrupt Pin (LVCMOS).** Indicates a change of device status prompting the processor to read the enabled interrupt service registers (ISR). This pin is an open drain, active low and requires an external pulled-up to Vdd.
H2	i2c_en	I_u	**I^2C Interface Enable (LVCMOS).** If set high, the I^2C interface is enabled, if set low, the SPI interface is enabled. Internally pull-up to Vdd.
APLL Loop Filter			
A5	apll_filter	A	**External Analog PLL Loop Filter terminal.**
B5	filter_ref0	A	**Analog PLL External Loop Filter Reference.**
C5	filter_ref1	A	**Analog PLL External Loop Filter Reference.**
JTAG and Test			
G4	tdo	O	**Test Serial Data Out (Output).** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G2	tdi	I_u	**Test Serial Data In (Input).** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to Vdd. If this pin is not used then it should be left unconnected.
G3	trst_b	I_u	**Test Reset (LVCMOS).** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to Vdd. If this pin is not used then it should be connected to GND.
H3	tck	I	**Test Clock (LVCMOS):** Provides the clock to the JTAG test logic. If this pin is not used then it should be pulled down to GND.
F2	tms	I_u	**Test Mode Select (LVCMOS).** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.

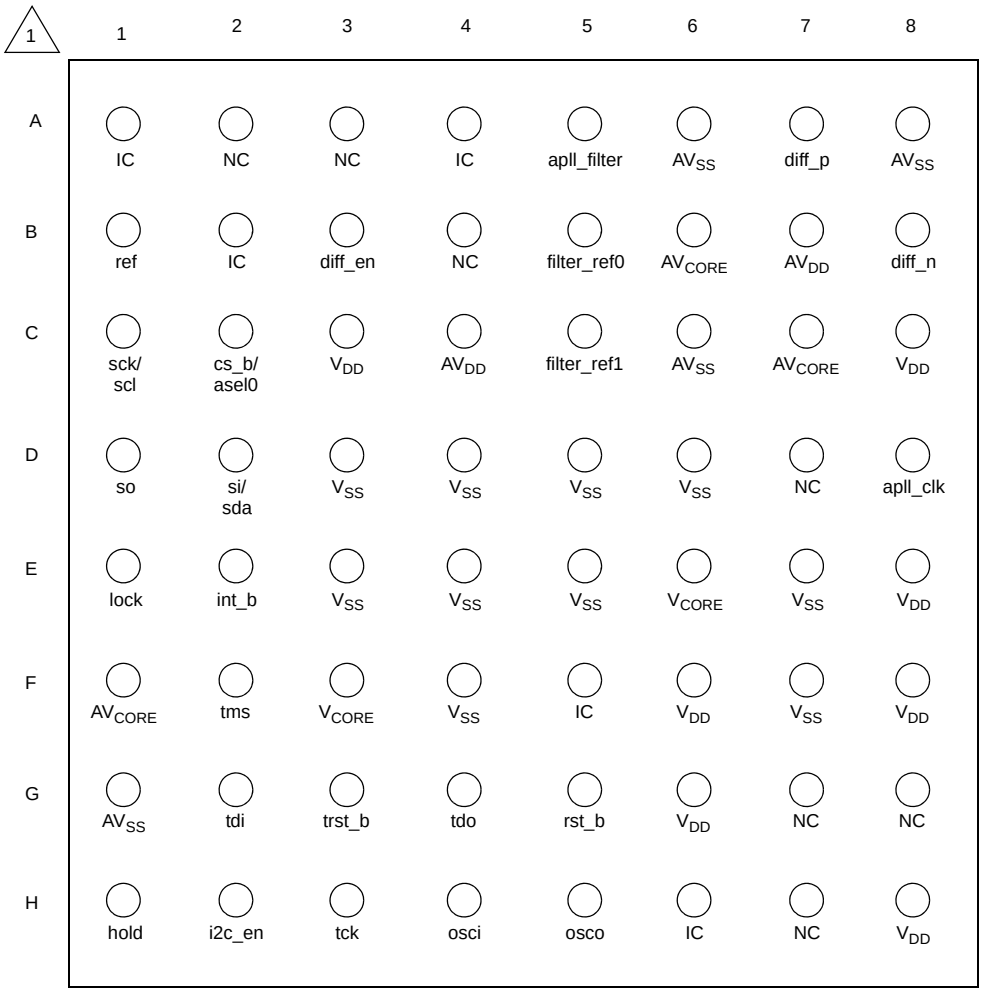
Pin #	Name	I/O Type	Description
Master Clock			
H4	osci	I	**Oscillator Master Clock Input (LVCMOS).** This input accepts a 20 MHz reference from a clock oscillator (XO) or crystal XTAL. The stability and accuracy of the clock at this input determines the free-run accuracy and the holdover stability of the output clocks.
H5	osco	O	**Oscillator Master Clock Output (LVCMOS).** This pin must be left unconnected when the osci pin is connected to a clock oscillator.
Miscellaneous			
A1 A4 F5	IC		**Internal Connection.** Leave unconnected.
B2 H6	IC		**Internal Connection.** Must be connect to ground.
A2 A3 B4 D7 G7 G8 H7	NC		**No Connection.** Leave unconnected.
Power and Ground			
C3 C8 E8 F6 F8 G6 H8	V_{DD}	P P P P P P P	**Positive Supply Voltage.** +3.3V_{DC} nominal.
E6 F3	V_{CORE}	P P	**Positive Supply Voltage.** +1.8V_{DC} nominal.
B7 C4	AV_{DD}	P P	**Positive Analog Supply Voltage.** +3.3V_{DC} nominal.
B6 C7 F1	AV_{CORE}	P P P	**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.

Pin #	Name	I/O Type	Description
D3 D4 D5 D6 E3 E4 E5 E7 F4 F7	V_{SS}	G G G G G G G G G G	**Ground.** 0 Volts.
A6 A8 C6 G1	AV_{SS}	G G G G	**Analog Ground.** 0 Volts.

I - Input
I_d - Input, Internally pulled down
I_u - Input, Internally pulled up
O - Output
A - Analog
P - Power
G - Ground

1.0 Pin Diagram

TOP VIEW



1 - A1 corner is identified with a dot.

2.0 High Level Overview

The ZL30145 is a highly integrated device that provides timing for line cards. The DPLL automatically locks to one input reference and provides two synchronized output clocks for synchronizing SONET/SDH and Synchronous Ethernet line cards.

The ZL30145 has a on-chip digital phase-locked loop (DPLL) designed to provide rate conversion and jitter attenuation for Synchronous Ethernet, (SyncE), Synchronous Digital Hierarchy (SDH) and Synchronous Optical Network (SONET) networking equipment. The ZL30145 generates very low jitter clocks that meet the jitter requirements of ITU-T G.8262, Telcordia GR-253-CORE OC-48, OC-12, OC-3, OC-1 rates and ITU-T G.813 STM-16, STM-4 and STM-1 rates.

2.1 DPLL Features

The ZL30145 provides one Digital Phase-Locked Loop (DPLL) for clock synchronization. Table 1 shows a feature summary for the DPLL.

Feature	DPLL
Modes of Operation	Free-run, Normal (locked), holdover
Loop Bandwidth (BW)	User selectable: 14 Hz, 28 Hz[1], or wideband[2] (890 Hz / 56 Hz / 14 Hz)
Lock Time	< 1 s
Pull-in Range	Fixed: 130 ppm
Input Ref Frequencies	2 kHz, N * 8 kHz up to 77.76 MHz, including 25 MHz, 50 MHz, in addition to 62.5 MHz, 125 MHz., and 155.52 MHz
External Status Pin Indicators	Lock, holdover

Table 1 - DPLL Features

1. Limited to 14 Hz for 2 kHz references
2. In the wideband mode, the loop bandwidth depends on the frequency of the reference input. For reference frequencies greater than 8 kHz, the loop bandwidth = 890 Hz. For reference frequencies equal to 8 kHz, the loop bandwidth = 56 Hz. The loop bandwidth is equal to 14 Hz for reference frequencies of 2 kHz.

2.2 DPLL Mode Control

The DPLL supports three modes of operation - free-run, normal, and holdover. The mode of operation is controlled by an automatic state machine as shown in Figure 2.

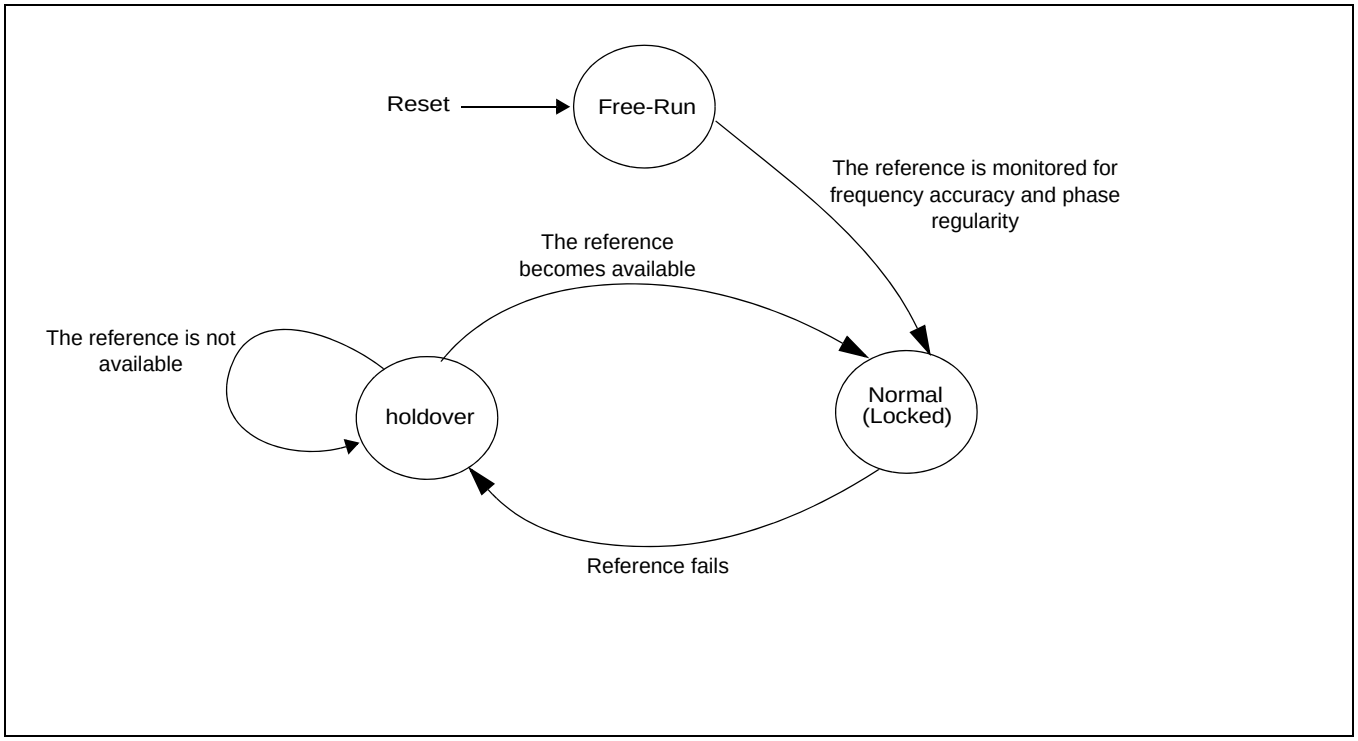


Figure 2 - Automatic Mode State Machine

Free-run

The free-run mode occurs immediately after a reset cycle or when the DPLL has never been synchronized to a reference input. In this mode, the frequency accuracy of the output clocks is equal to the frequency accuracy of the external master oscillator.

Normal (locked)

The usual mode of operation for the DPLL is the normal mode where the DPLL phase locks to the reference input and generates output clock with a frequency accuracy equal to the frequency accuracy of the reference input.

Holdover

When the DPLL operating in the normal mode loses its reference input, it will enter the holdover mode and continue to generate output clocks based on historical frequency data collected while the DPLL was synchronized. The transition between normal and holdover modes is controlled by the DPLL so that its initial frequency offset is better than 100 ppb. The frequency drift after this transition period is dependant on the frequency drift of the external master oscillator.

2.3 Loop Bandwidth

The loop bandwidth determines the amount of jitter filtering that is provided by the DPLL. The loop bandwidth for the DPLL is programmable using the *bandwidth* field of the *dpll_ctrl_0* register (0x1D).

2.4 Reference Input

There is one reference clock input (**ref)** available to the DPLL. The reference input is used to synchronize the output clock.

The **ref** input accepts a single-ended LVCMOS clock with a frequency ranging from 2 kHz to 77.76 MHz. Built-in frequency detection circuitry automatically determines the frequency of the reference if its frequency is within the set of pre-defined frequencies as shown in Table 2. Once detected, the resulting frequency of the reference can be read from the detected_ref[0] registers (0x10).

2 kHz	16.384 MHz
8 kHz	19.44 MHz
64 kHz	38.88 MHz
1.544 MHz	77.76 MHz
2.048 MHz	
6.48 MHz	
8.192 MHz	

Table 2 - Set of Pre-Defined Auto-Detect Clock Frequencies

Two additional custom reference frequencies (Custom A and Custom B) are also programmable using the *custA_mult[1:0]* and *custB_mult[1:0]* registers (0x67, 0x68, 0x71, 0x72). These custom frequencies are programmable as 8 kHz * N up to 77.76 MHz (where N = 1 to 9720), or 2 kHz (when N = 0). The *ref_freq_mode_0* register (0x65) are used to configure each of the reference inputs as auto-detect, custom A, or custom B.

The reference input (**ref**) has programmable pre-dividers which allows them to lock to frequencies higher than 77.76 MHz or to non-standard frequencies. By default the pre-dividers divide by 1, but they can be programmed to divide by 1.5, 2, 2.5, 3, 4, 5, 6, 7, and 8 using the *ref_div* bits of the *predivider_ctrl* register (0x7E). For example, an input frequency of 125 MHz can be divided down by 5 using the pre-dividers to create a 25 MHz input reference. The 25 MHz can then be programmed as a custom input frequency. Similarly, a 62.5 MHz input clock can be divided by 2.5 to create 25 MHz. **Note that division by non-integer values (e.g., 1.5, 2.5) is achieved by using both the rising and falling edges of the input reference. This may cause higher jitter levels at the output clocks when the reference input does not have a 50% duty cycle.**

2.5 Reference Monitoring

The input reference (**ref**) is monitored for frequency accuracy and phase regularity and it is continuously monitored to ensure that it is a valid reference. The process of qualifying the reference depends on 3 levels of monitoring.

Single Cycle Monitor (SCM)

The SCM block measures the period of each reference clock cycle to detect phase irregularities or a missing clock edge. In general, if the measured period deviates by more than 50% from the nominal period, then an SCM failure (scm_fail) is declared.

Coarse Frequency Monitor (CFM)

The CFM block monitors the reference frequency over a measurement period of 30 µs so that it can quickly detect large changes in frequency. A CFM failure (cfm_fail) is triggered when the frequency has changed by more than 3% or approximately 30000 ppm.

Precise Frequency Monitor (PFM)

The PFM is used to keep track of the frequency of the reference clock. It measures its frequency over a 10 second period and indicates a failure when the measured frequency exceeds 83ppm. To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the SCM or CFM. The PFM provides a level of hysteresis between the acceptance range (64ppm) and the rejection range (83ppm) to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range.

SCM, CFM, and PFM failures are indicated in the ref_mon_fail register (0x05). If any one of these failures are detected and are not individually masked then the ZL30145 will go into holdover. As shown in Figure 3, the SCM, CFM, and PFM indicators are logically ORed together to form a reference failure indicator. An interrupt is triggered when the failure indicator is triggered. The status of the failure indicators can be read in the *ref_fail_isr* interrupt service register (0x02). A change in the bit status of this register will cause the interrupt pin (**int_b**) to go low. It is possible to mask this interrupt with the *ref_fail_isr_mask* register (0x09) which is represented as "mask_isr_n".

It is possible to mask an individual reference monitor from triggering a reference failure by setting the *ref_mon_fail_mask* register (0x0C). These are represented by mask_scm_n, mask_cfm_n, and mask_pfm_n in Figure 3.

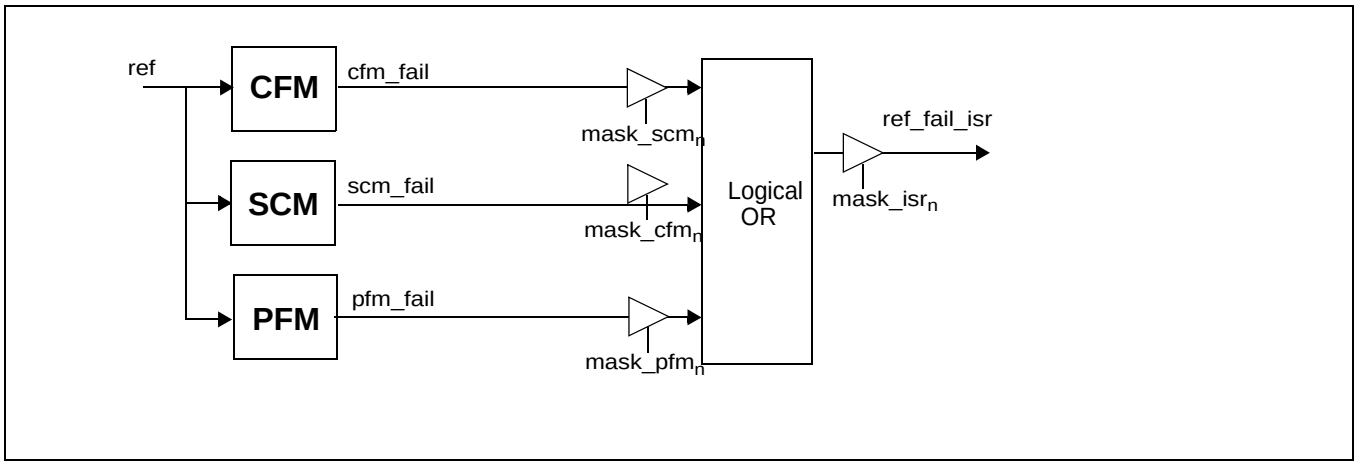


Figure 3 - Reference Monitoring Block Diagram

2.6 Reference Monitoring for Custom Configurations

As described in section 2.4, “Reference Input“, two additional custom reference input frequencies (Custom A, Custom B) are definable allowing a reference input to accept any multiple of 8 kHz up to 77.76 MHz.

Each of the custom configurations also have definable SCM and CFM limits. The SCM limits are programmable using the *custA_scm_low, custA_scm_high_lim, custB_scm_low, custB_scm_high* registers (0x69, 0x6A, 0x73, 0x74). The SCM low and high limits determine the acceptance window for the clock period as shown in Figure 4. Any clock edge that does not fall into the acceptance window will trigger an SCM failure. High and low limits are programmed as multiples of a 300 MHz cycle (3.33 ns).

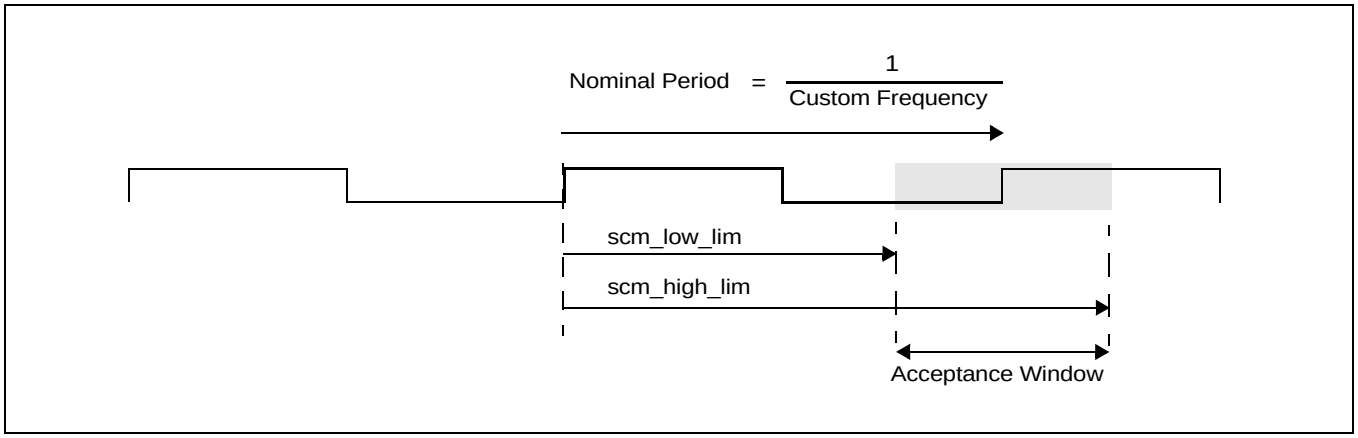


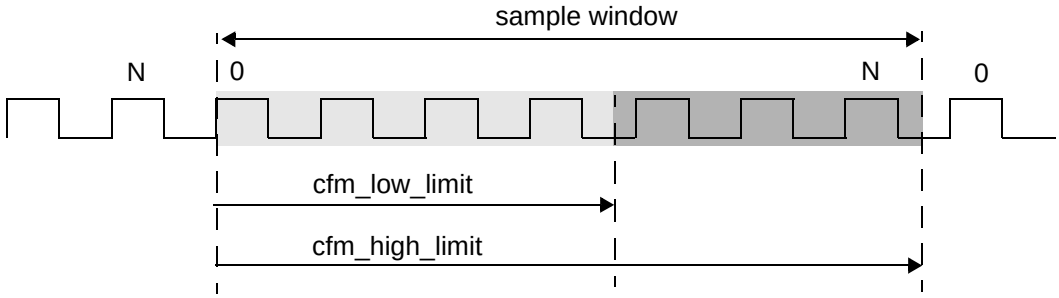
Figure 4 - Defining SCM Limits for Custom Configurations

Since the SCM is used to identify a missing clock edge, the acceptance window should be set to approximately +/-50% of the nominal period. Using a smaller window may trigger unwanted SCM failures.

For example, if the Custom A frequency was defined as 50 MHz (using registers 0x67, 0x68), its nominal period is 20 ns. To fail the input reference when its period falls below 10 ns (-50% of the nominal period), the *custA_scm_low* register is programmed to 0x03 (3 x 1/300MHz = 10 ns). To fail the input reference if its period exceeds 30 ns (+50% of the nominal period), the *custA_scm_high* register is programmed with 0x09 (9 x 1/300MHz = 30 ns).

For low speed input references less than 1.8 MHz, the SCM counter does not provide enough range to reliably perform its function. Therefore for custom inputs of less than 1.8 MHz the device should set the scm_low_lim and scm_high_lim to 0 and the CFM should be used as the single cycle monitor.

The CFM quickly determines large changes in frequency by verifying that there are N amount of input reference clock cycles within a programmable sample window. The value of N is programmable in the *custA_cfm_cycle* and the *custB_cfm_cycle* registers (0x6F, 0x79). The size of the sample window is defined in terms of high and low limits and are programmed as multiples of 80 MHz cycles. These are defined using the *custA_cfm_low_0*, *custA_cfm_low_1*, *custA_cfm_high_0*, *custA_cfm_high_1*, *custB_cfm_low_0*, *custB_cfm_low_1*, *custB_cfm_high_0*, *custB_cfm_high_1* registers (0x6B-0x6E, 0x75-0x78). A divide-by-4 circuit can be enabled to increase the resolution of the sample window. This is recommended when the input reference frequency exceeds 19.44 MHz. The divide-by-4 is enabled using the custA_div and custB_div registers (0x70, 0x7A). Equations for calculating the high and low limits are shown in Figure 5.



$$\textbf{cfm\_low\_limit} = \frac{\textbf{D}}{\text{cust\_freq} + 3\%} \times \textbf{N} \times 80\ \text{MHz} \qquad \textbf{cfm\_high\_limit} = \frac{\textbf{D}}{\text{cust\_freq} - 3\%} \times \textbf{N} \times 80\ \text{MHz}$$

where **N** and **D** are dependant on the setting of the custom frequency. Recommended values are shown in the following table:

Input Frequency Range	D (Divider)	N (Number of cycles)
38.88 MHz < freq ≤ 77.76 MHz	4	256
19.44 MHz < freq ≤ 38.88 MHz	4	128
8.192 MHz < freq ≤ 19.44 MHz	1	256
2.048 MHz < freq ≤ 8.192 MHz	1	128
1.8 MHz < freq ≤ 2.048 MHz	1	32
2 kHz < freq ≤ 1.8 MHz (Recommended CFM limits = +/- 50%	1	1

Example: Custom configuration A is set for 50 MHz **(custA_mult13_8 = 0x18, custA_mult13_8 = 0x6A)**

The values for D and N are determined using the table above with respect to a 50 MHz input reference.

D = 4 **(custA_div = 0x01)**

N = 256 **(custA_cfm_cycle = 0xFF)**

The CFM low and high values are calculated using the equations above:

$$\text{cfm\_low\_limit} = \frac{4}{51.5\ \text{MHz}} \times 256 \times 80\ \text{MHz} = 1591_{dec} = 0637_{hex}$$

(custA_cfm_low15_8 = 0x06)
(custA_cfm_low7_0 = 0x37)

$$\text{cfm\_high\_limit} = \frac{4}{48.5\ \text{MHz}} \times 256 \times 80\ \text{MHz} = 1689_{dec} = 0699_{hex}$$

(custA_cfm_high15_8 = 0x06)
(custA_cfm_high7_0 = 0x99)

Figure 5 - Custom CFM Configuration for 50 MHz

2.7 Output Clocks

The ZL30145 offers one low-jitter differential LVPECL clock (**diff**) and one APLL LVCMOS (**apll_clk**) output clock.

The single ended APLL LVCMOS output clock (**apll_clk**) frequency is programmable using the *apll_clk_freq* register (0x52). Valid frequencies are listed in Table 3. The *eth_en* and the f_sel bits are set using the *apll_run* register (0x51).

apll_clk_freq bit settings	**apll_clk Output Frequency**	
	SONET/SDH Mode	**Ethernet Mode - Low Speed**
	eth_en = 0 f_sel = 0	eth_en = 1 f_sel = 1
0001	Reserved	125 MHz
0010	77.76 MHz	62.5 MHz
0011	38.88 MHz	Reserved
0100	19.44 MHz	Reserved
0101	9.72 MHz	50 MHz
0110	Reserved	25 MHz
0111	Reserved	12.5 MHz
1010	51.84 MHz	Reserved
1011	25.92 MHz	Reserved
1100	12.96 MHz	Reserved
1101	6.48 MHz	Reserved

Table 3 - APLL LVCMOS Output Clock Frequencies

The differential output clock (**diff**) frequency is programmable using the *diff_sel* bit of the *diff_sel* register (0x61). When in SONET/SDH mode (eth_en = 0, f_sel = 0), any of the valid SONET/SDH clock frequencies shown in Table 4 can be selected. When in Ethernet mode (eth_en = 1), the APLL can generate two groups of frequencies - low speed (f_sel_diff = 1) or high speed (f_sel_diff = 0). Valid frequencies are listed in Table 4. The frequency group selector (f_sel_diff) is programmable using the apll_run register (0x51). When low speed ethernet mode and high speed ethernet modes are enabled at the same time (i.e., (eth_en =1, fsel = 1 and f_sel_diff = 0), please refer to Application Note ZLAN-254 for details on the appropriate device configuration settings

diff_clk_sel bit settings	**diff Output Frequency**		
	SONET/SDH Mode	**Ethernet Mode - Low Speed**	**Ethernet Mode - High Speed**
	eth_en = 0 f_sel_diff = 0	eth_en = 1 f_sel_diff = 1	eth_en = 1 f_sel_diff = 0
000	19.44 MHz	Reserved	Reserved
001	38.88 MHz	125 MHz	Reserved
010	77.76 MHz	62.5 MHz	Reserved
011	155.52 MHz	Reserved	156.25 MHz
100	311.04 MHz	Reserved	312.5 MHz
101	622.08 MHz	50 MHz	Reserved
110	6.48 MHz	25 MHz	Reserved
111	51.84 MHz	12.5 MHz	Reserved

Table 4 - APLL Differential Output Clock Frequencies

2.7.1 Output Clock Squelching

A clock squelching feature is available which allows forcing the output clock to a specific logic level. The *apll_clk_run* of the *apll_run*_register (0x51) control the ethernet single ended output (**apll_clk**).

2.7.2 Disabling Output Clocks

Unused outputs can be set to a high impedance state to reduce power consumption. The differential outputs can be disabled using the diff_en bit of the *diff_ctrl* register (0x60). The apll_clk output can be disabled using the *apll_clk_en* of the *apll_enable* register (0x50).

2.8 Configurable Input-to-Output and Output-to-Output Delays

The ZL30146 allows programmable static delay compensation for controlling input-to-output and output-to-output delays of its clocks and frame pulses.

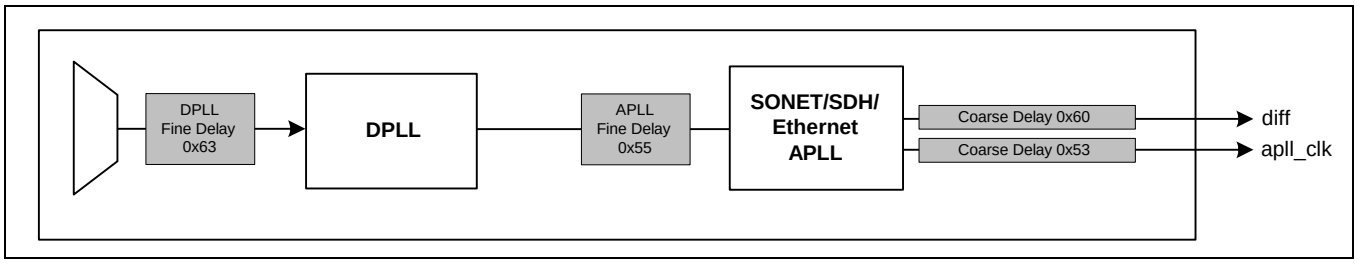


Figure 6 - Phase Delay Adjustments

The SONET/SDH/Ethernet APLL can be configured to lead or lag the selected input reference clock using the DPLL Fine Delay register (0x63). This allows delay adjustments in steps of 119.2 ps definable as an 8-bit two's complement value in the range of -128 to +127. Negative values delay the output clock, positive values advance the output clock. This gives a total delay adjustment in the range of -15.26 ns to +15.14 ns.

In addition to the delay introduced by the DPLL Fine Delay, the SONET/SDH/Ethernet APLL has the ability to add their own fine delay adjustments by programming registers 0x55. These registers are programmed as 8-bit two's complement values representing delays defined in steps of 119.2 ps with a range of -15.26 ns to +15.14 ns.

The single-ended output clock (**apll_clk**) can be independently offset by 90, 180, and 270 degrees using the coarse delay registers (0x53).

The differential clock output (**diff**) can be delayed by -1.6 ns, 0 ns, +1.6 ns, or +3.2 ns. This delay is programmable using the *diff_adjust* bit of the *diff_ctrl* register (0x60).

2.9 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators. Oscillators up to 32ppm of frequency accuracy may be used with the ZL30145.

2.10 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 7. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

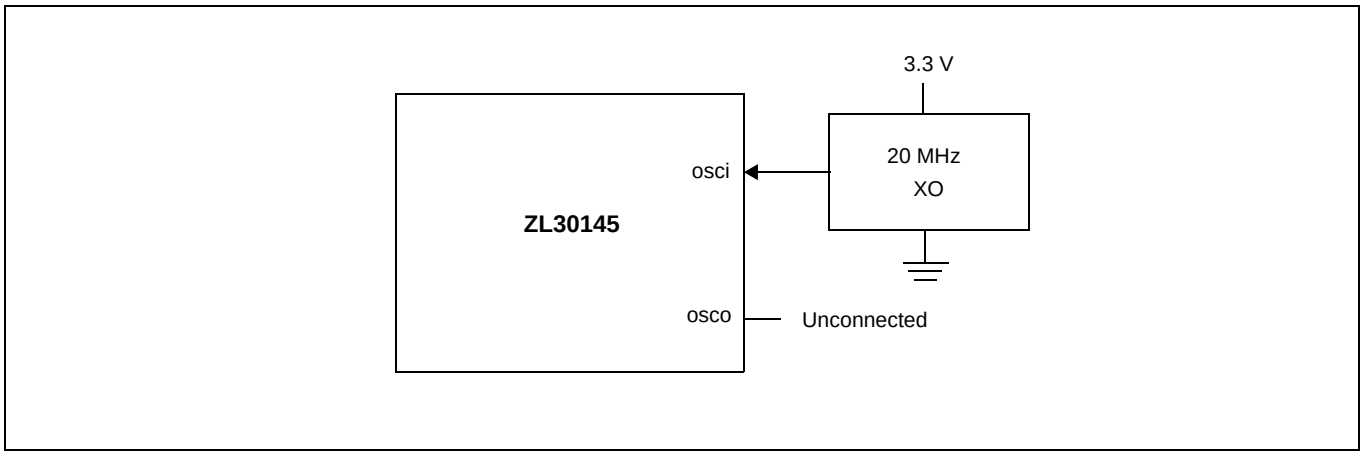


Figure 7 - Clock Oscillator Circuit

2.11 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up. The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

2.12 Power Supply Filtering

Jitter levels on the ZL30145 output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the ZL30145 device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-212.

2.13 Reset Circuit

To ensure proper operation, the device must be reset by holding the rst_b pin low for at least 300 ns after power-up. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 8. This circuit provides approximately 60 µs of reset low time. The rst_b input has schmitt trigger properties to prevent level bouncing.

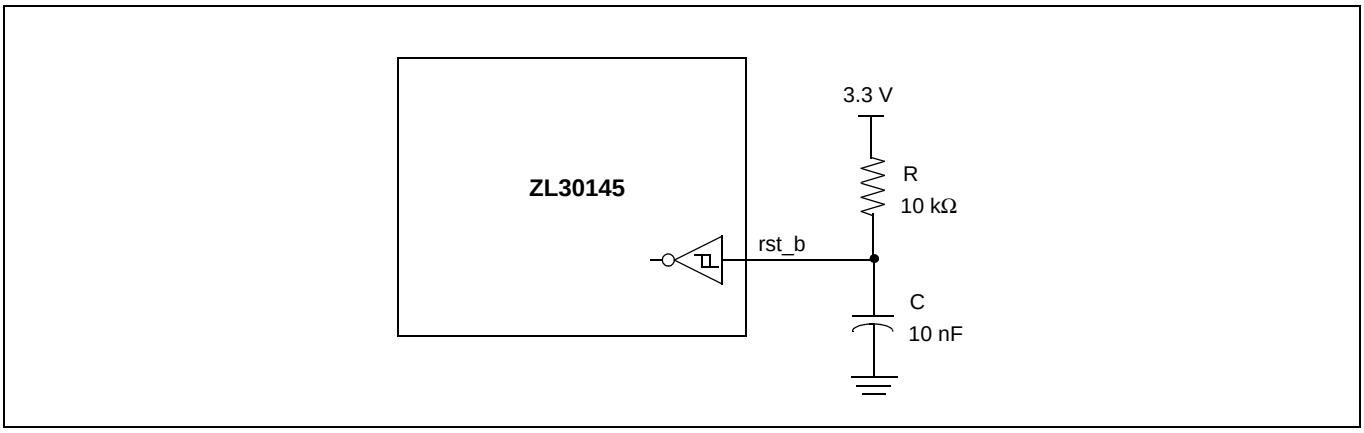


Figure 8 - Typical Power-Up Reset Circuit

2.14 APLL Filter Components and Recommended Layout

The low jitter APLL in the ZL30145 uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

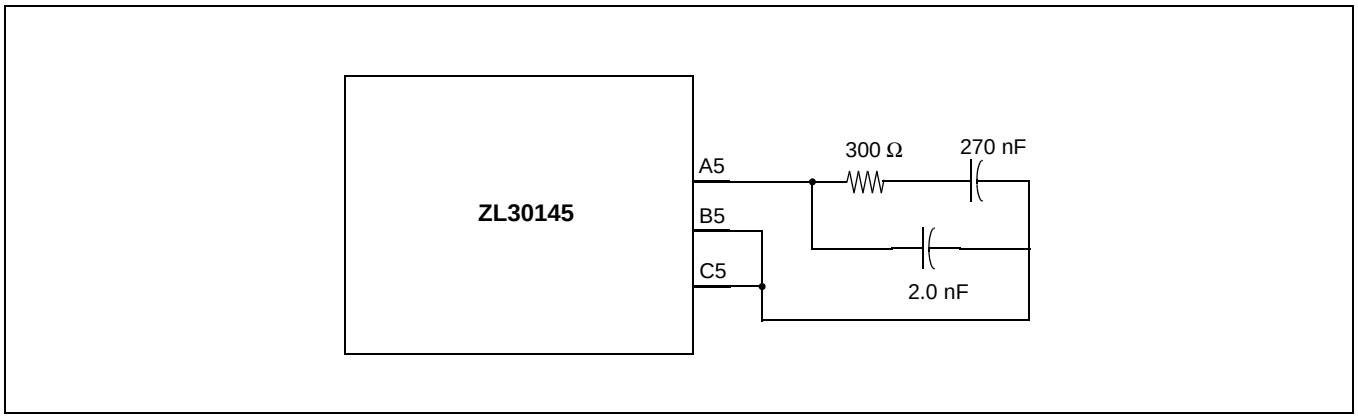


Figure 9 - APLL Filter Component Values

The recommended PCB layout for the external filter components is shown in Figure 10.

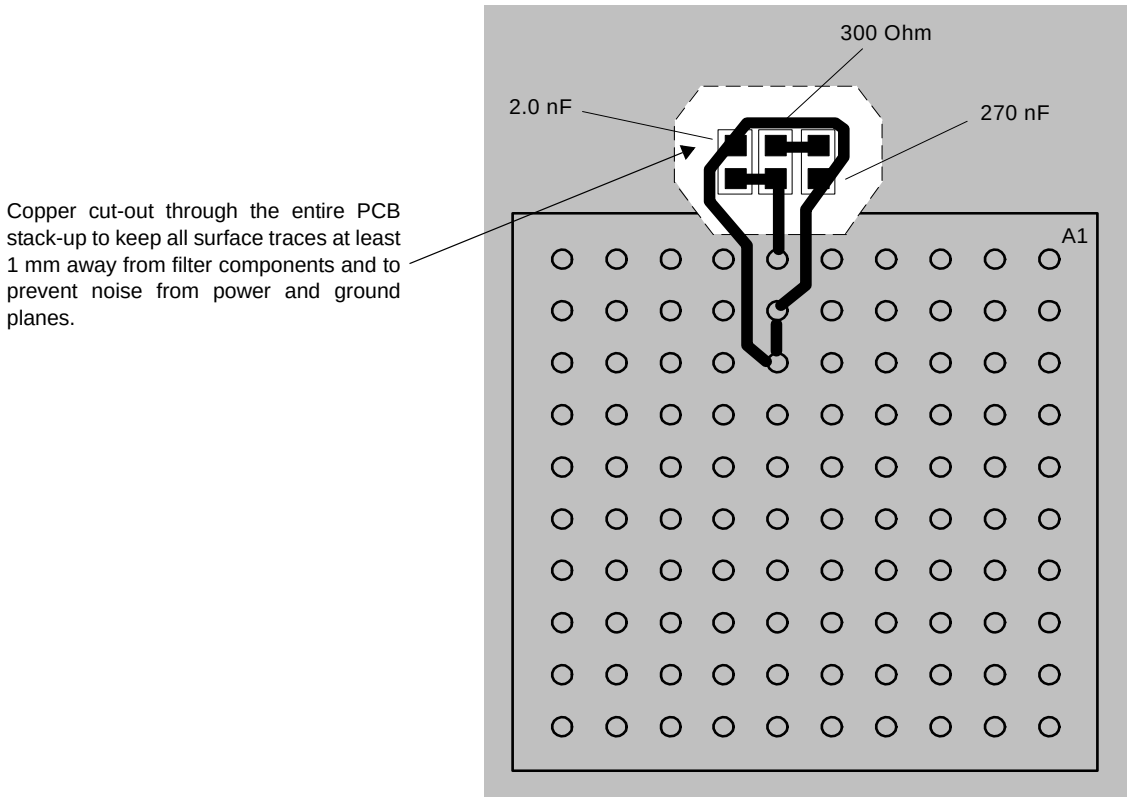


Figure 10 - Recommended APLL Filter Layout

2.15 Serial Interface

A host processor controls and receives status from the ZL30145 using either a SPI or an I^2C interface. The type of interface is selected using the **i2c_en** pin. As shown in Figure 11, when i2c_en is set high (or left unconnected) the serial interface is compatible with an I^2C bus and is compatible with SPI when set low.

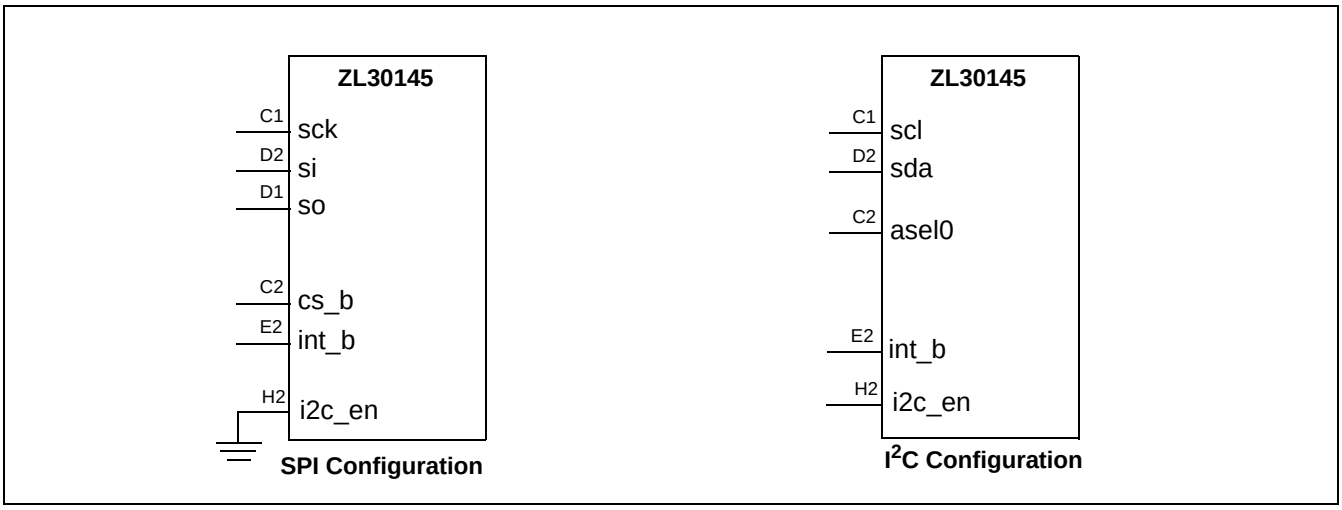


Figure 11 - Serial Interface Configuration

2.15.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b**_asel0 is high. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The SPI supports half-duplex processor mode which means that during a write cycle to the ZL30145, output data from the **so** pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle from the ZL30145.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 12, Figure 13 and Figure 14. Timing characteristics are shown in Table 6, Figure 24, and Figure 25.

2.15.2 SPI Functional Waveforms

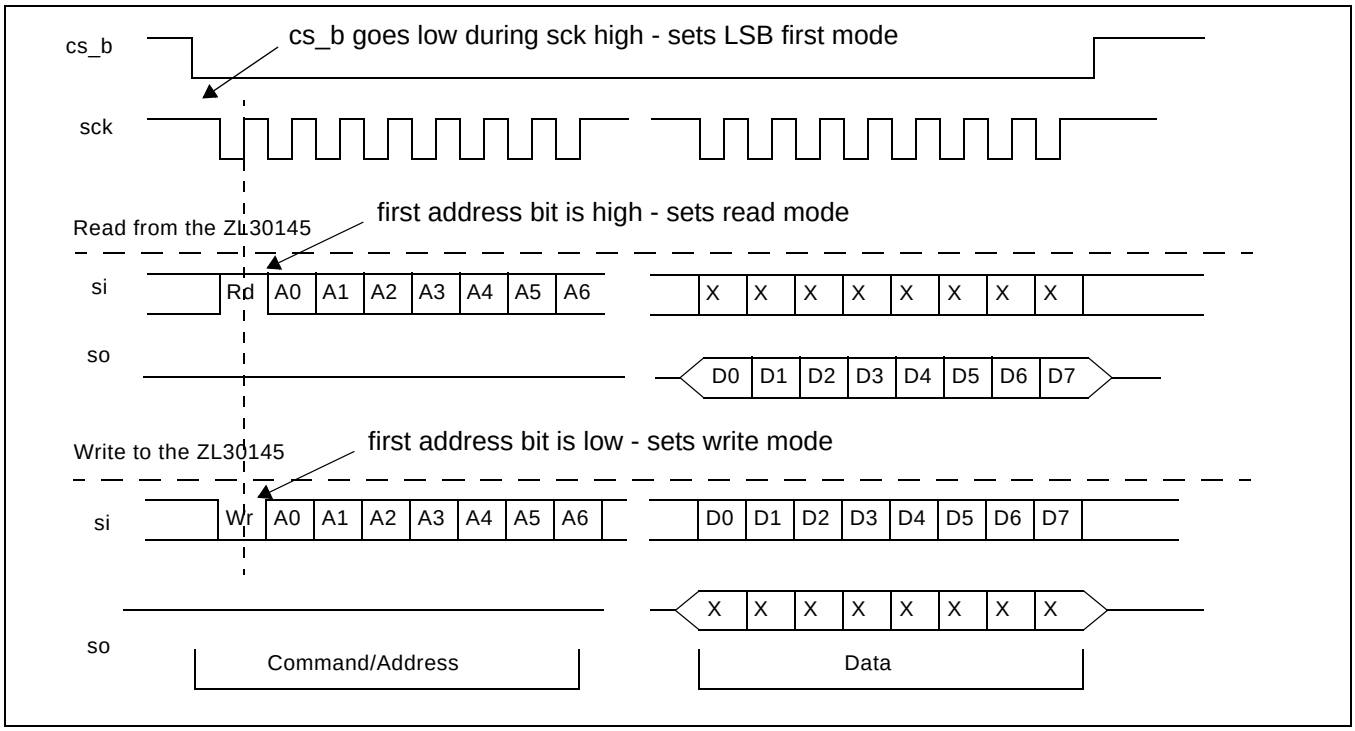


Figure 12 - LSB First Mode - One Byte Transfer

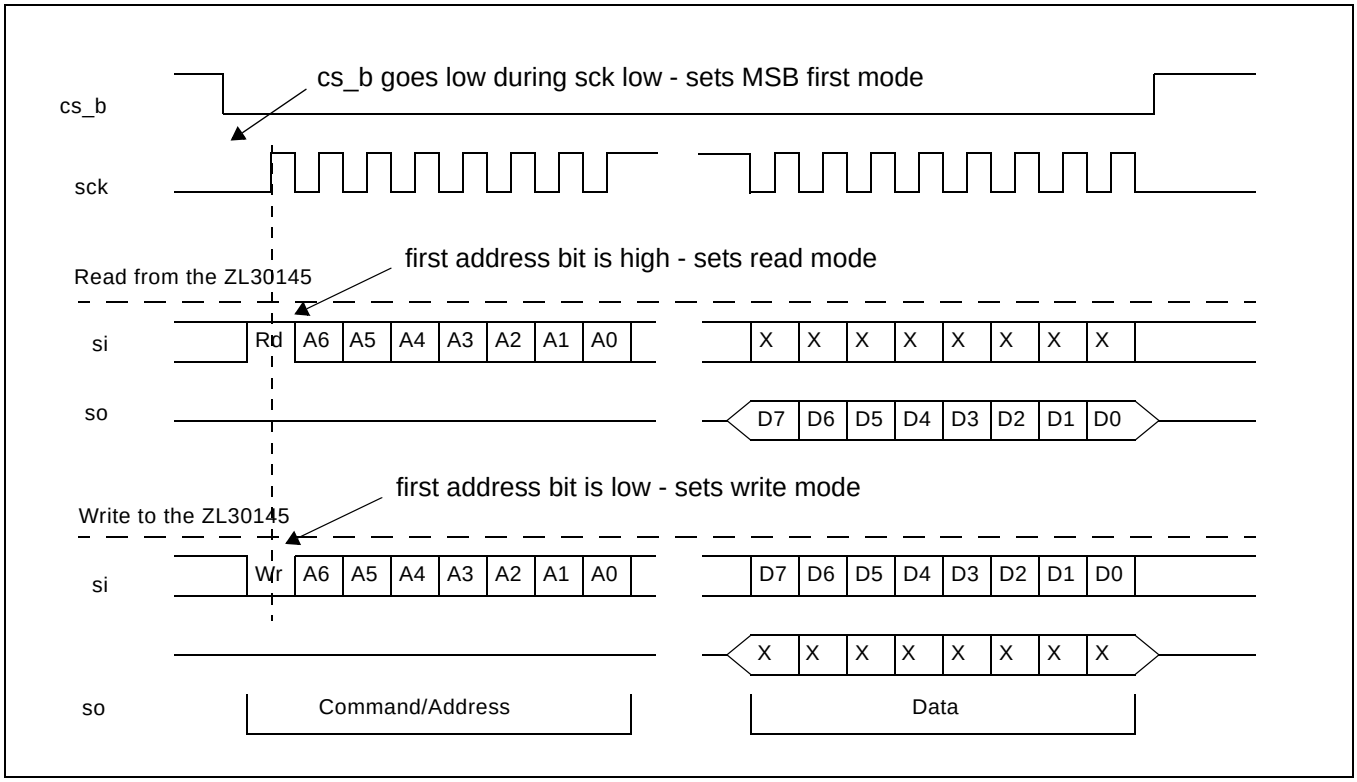


Figure 13 - MSB First Mode - One Byte Transfer

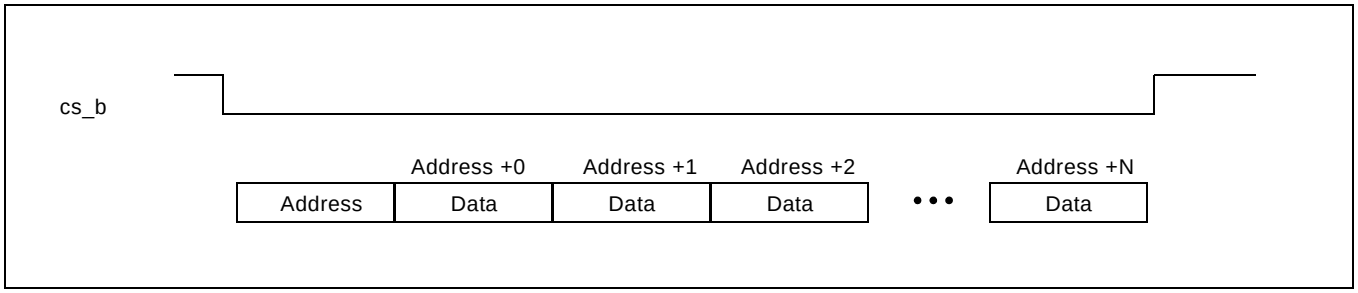


Figure 14 - Example of a Burst Mode Operation

2.15.3 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 15, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

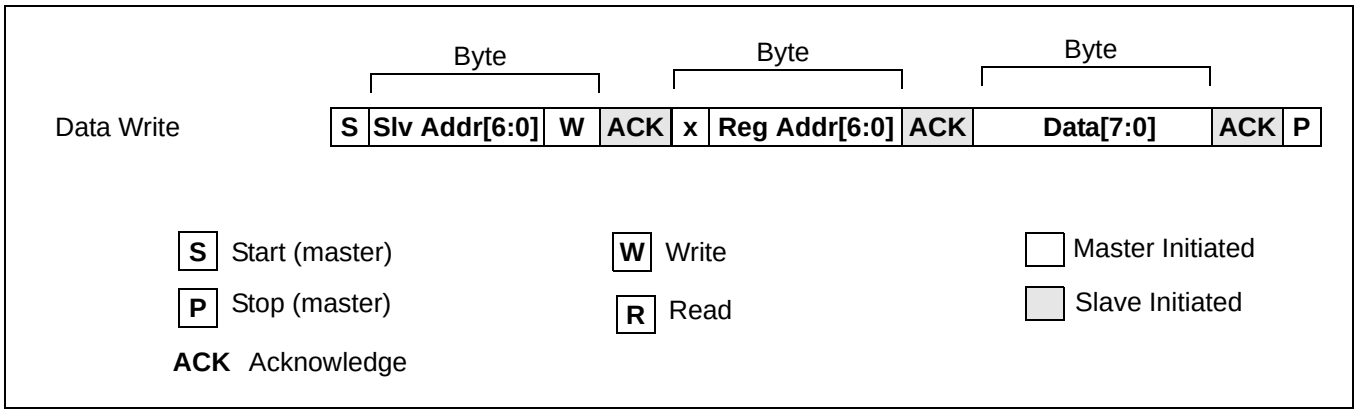


Figure 15 - I²C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 16.

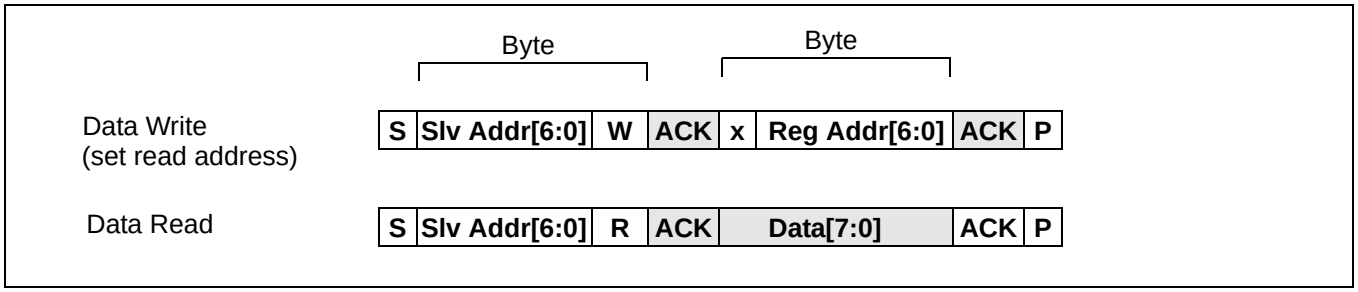


Figure 16 - I²C Data Write Protocol

The **7-bit device (slave) address** of the ZL30145 contains a 6 bit fixed address plus a variable bit which is set with the **asel0** pin. This allows two ZL30145s to share the same I²C bus. The address configuration is shown in Figure 17.

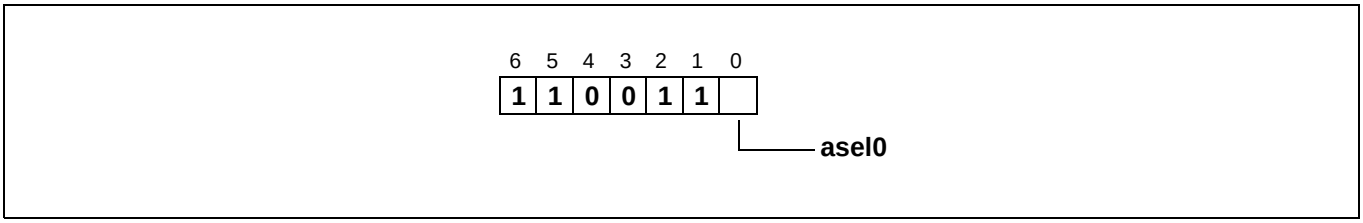


Figure 17 - ZL30145 I²C 7-bit Slave Address

The ZL30145 also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 18 (write) and Figure 19 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically incremented address. The maximum auto incremented address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto incremented address does not wrap around to 0x00 after reaching 0x7F.

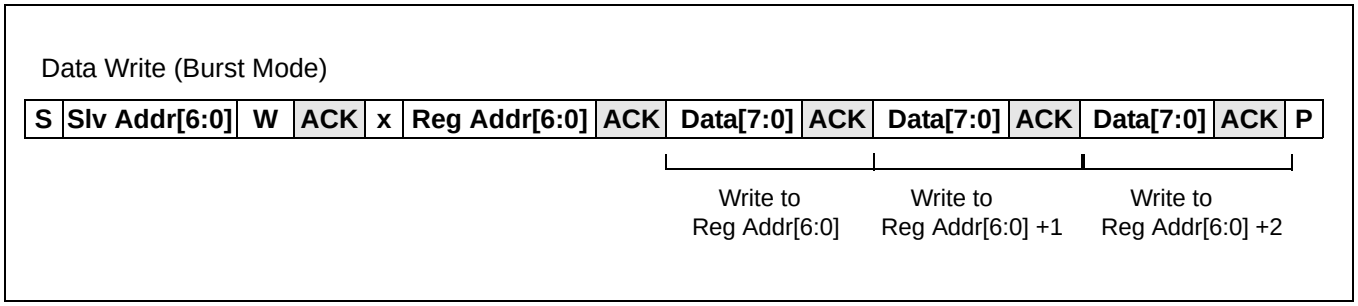


Figure 18 - I²C Data Write Burst Mode

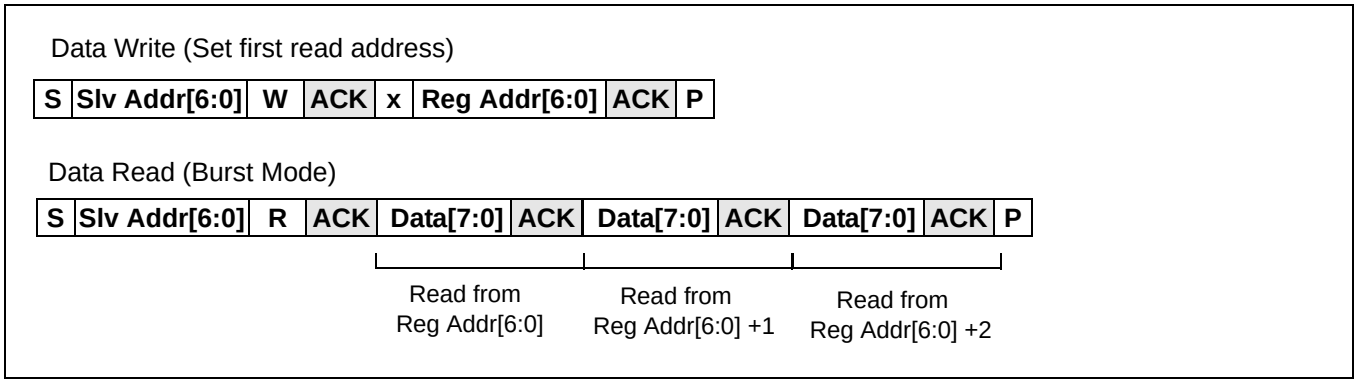


Figure 19 - I²C Data Read Burst Mode

The timing specification for the I²C interface is shown in Figure 26 and Table 7.

3.0 Software Configuration

The ZL30145 is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

3.0.1 Interrupts

The device has several status registers to indicate its current state of operation. The interrupt pin (**int_b**) becomes active (low) when a critical change in status occurs. Examples of critical events that would trigger an interrupt are:

- Reference failure
- Changes in mode of operation (lock, holdover)

Most of the interrupt register bits behave like "sticky bits" which means that once they are triggered, they will stay triggered even if the condition that caused the interrupt is removed. When a register containing sticky bits is read, the sticky bits are automatically cleared.

3.0.2 Multi-byte Register Values

The ZL30145 register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order. The 8-bit register containing the least significant byte (LSB) must be accessed first, and the register containing the most significant byte (MSB) must be accessed last. An example of a multi-byte register is shown in Figure 20. When reading a multi-byte value, the value across all of its registers remains stable until the MSB is read. When writing a multi-byte value, the value is latched when the MSB is written.

Example:
The programmable frame pulse phase offset for p_fp is programmed using a 22-bit value which is spread over three 8-bit registers. The LSB is contained in address 0x40, the middle byte in 0x41, and the MSB in 0x42. When reading or writing this multi-byte value, the LSB must be accessed first, followed by the middle byte, and the MSB last.

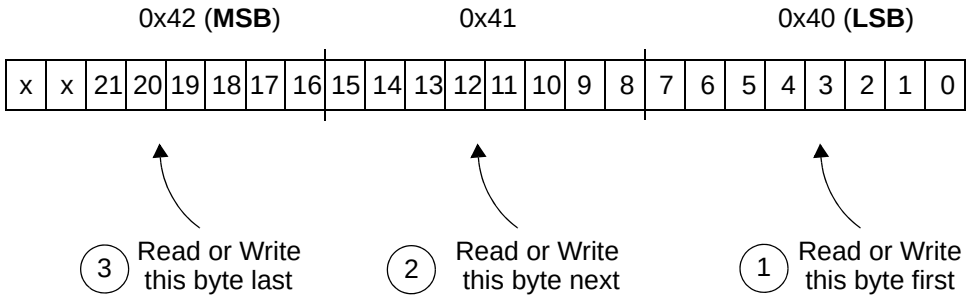


Figure 20 - Accessing Multi-byte Register Values

The following table provides a summary of the registers available for status updates and configuration of the device.

Page_Addr (Hex)	Register Name	Description	Type
Miscellaneous Registers			
0x00	id_reg	Chip and version identification	R
0x01	Reserved		
Interrupts			
0x02	ref_fail_isr	Reference failure interrupt service register	R
0x03	dpll_isr	DPLL interrupt service register	StickyR
0x04	Reserved		
0x05	ref_mon_fail	ref failure indications	Sticky R
0x06 - 0x08	Reserved		
0x09	ref_fail_isr_mask	Reference failure interrupt service register mask	R/W
0x0A	dpll_isr_mask	DPLL interrupt service register mask	R/W
0x0B	Reserved		
0x0C	ref_mon_fail_mask	Control register to mask each failure indicator for ref	R/W
0x0D - 0x0F	Reserved		
Reference Monitor Setup			
0x10	detected_ref_0	ref auto-detected frequency value status register	R
0x11 - 0x1C	Reserved		
DPLL Control Registers			
0x1D	dpll_ctrl_0	Control register for the DPLL filter bandwidth	R/W
0x1E-0x20	Reserved		
0x21	dpll_ref_fail_mask	Control register to mask each failure indicator (SCM, CFM, and PFM) used for automatic holdover	R/W
0x22 - 0x27	Reserved		
0x28	dpll_std_lock_fail	DPLL lock and holdover status register	R

Table 5 - Register Map

Page_Addr (Hex)	Register Name	Description	Type
0x29 - 0x35	Reserved		
Programmable Synthesizer Configuration Registers			
0x36 - 0x4F	Reserved		
0x50	apll_enable	Control register to enable eth_clk and the APLL block	R/W
0x51	apll_run	Control register to generate apll_clk. Also used for enabling ethernet output clocks.	R/W
0x52	apll_clk_freq	Control register for the apll_clk frequency selection	R/W
0x53	apll_clk_offset90	Control register for the apll_clk phase position coarse tuning	R/W
0x54	Reserved		
0x55	apll_offset_fine	Control register for the apll path	R/W
0x56 - 0x5F	Reserved		
Differential Output Configuration			
0x60	diff_clk_ctrl	Control register to enable diff_clk	R/W
0x61	diff_clk_sel	Control register to select the diff_clk frequency	R/W
0x62-0x64	Reserved		
Custom Input Frequency Configuration			
0x65	ref_freq_mode_0	Control register to set whether to use auto detect, CustomA or CustomB for ref	R/W
0x66	Reserved		
0x67	custA_mult_0	Control register for the [7:0] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x68	custA_mult_1	Control register for the [13:8] bits of the custom configuration A. This is the N integer for the N*8kHz reference monitoring.	R/W
0x69	custA_scm_low	Control register for the custom configuration A: single cycle SCM low limiter	R/W

Table 5 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x6A	custA_scm_high	Control register for the custom configuration A: single cycle SCM high limiter	R/W
0x6B	custA_cfm_low_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM low limit	R/W
0x6C	custA_cfm_low_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM low limit	R/W
0x6D	custA_cfm_hi_0	Control register for the custom configuration A: The [7:0] bits of the single cycle CFM high limit	R/W
0x6E	custA_cfm_hi_1	Control register for the custom configuration A: The [15:0] bits of the single cycle CFM high limiter	R/W
0x6F	custA_cfm_cycle	Control register for the custom configuration A: CFM reference monitoring cycles - 1	R/W
0x70	custA_div	Control register for the custom configuration A: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x71	custB_mult_0	Control register for the [7:0] bits of the custom configuration B. This is the 8 k integer for the N*8kHz reference monitoring.	R/W
0x72	custB_mult_1	Control register for the [13:8] bits of the custom configuration B. This is the 8 k integerfortheN*8kHzreferencemonitoring.	R/W
0x73	custB_scm_low	Control register for the custom configuration B: single cycle SCM low limiter	R/W
0x74	custB_scm_high	Control register for the custom configuration B: single cycle SCM high limiter	R/W
0x75	custB_cfm_low_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM low limiter.	R/W
0x76	custB_cfm_low_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM low limiter.	R/W
0x77	custB_cfm_hi_0	Control register for the custom configuration B: The [7:0] bits of the single cycle CFM high limiter.	R/W

Table 5 - Register Map (continued)

Page_Addr (Hex)	Register Name	Description	Type
0x78	custB_cfm_hi_1	Control register for the custom configuration B: The [15:0] bits of the single cycle CFM high limiter.	R/W
0x79	custB_cfm_cycle	Control register for the custom configuration B: CFM reference monitoring cycles - 1	R/W
0x7A	custB_div	Control register for the custom configuration B: enable the use of ref_div4 for the CFM and PFM inputs	R/W
0x7B to 0x7D	Reserved		
Input Reference Pre-Divider Control			
0x7E	predivider_control	Controls pre-dividers for ref	R/W
0x7F	Reserved		

Table 5 - Register Map (continued)

4.0 Detailed Register Map

Page_Address: **0x00**
Register Name: **id_reg**
Default Value: **See description**
Type: R/W

Bit Field	Function Name	Description
4:0	chip_id	Chip Identification = `11111`
6:5	chip_revision	Chip revision number.
7	reset_ready	Reset ready indication. When this bit is set to 1 the reset cycle has completed.

Address: **0x02**
Register Name: **ref_fail_isr**
Default Value: 0xFF
Type: R

Bit Field	Function Name	Description
0	ref_fail	This bit is set to 1 when ref has a failure
7:1	Reserved	

Address: **0x03**
Register Name: **dpll_isr**
Default Value: **See description**
Type: R Sticky

Bit Field	Function Name	Description
0	locked	This bit is set to high when DPLL achieves lock. The bit is cleared automatically when this register is read.
1	lost_lock	This bit is set to high when DPLL loses lock. The bit is cleared automatically when this register is read.
2	holdover	This bit is set to high when DPLL enters holdover. The bit is cleared automatically when this register is read.
7:3	reserved	

Address: **0x05**
Register Name: **ref_mon_fail**
Default Value: **See description**
Type: Sticky R

Bit Field	Function Name	Description
0	ref_scm_failed	SCM failure indication
1	ref_cfm_failed	CFM failure indication
2	reserved	
3	ref_pfm_failed	PFM failure indication
7:4	Reserved	

Address: **0x09**
Register Name: **ref_fail_isr_mask**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
0	ref_fail_isr_mask	Reference failure interrupt service register mask.Masking a bit to zero will disable interrupt generation. xxxxxxx0: masks ref failure
7:1	Reserved	Leave as default

Address: **0x0A**
Register Name: **dpll_isr_mask**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
2:0	dpll_isr_mask	DPLL interrupt service register mask. Enabling a mask bit to one will allow interrupt generation xxxxxxx0: masks locked condition xxxxxx0x: masks lost_lock condition xxxxx0xx: masks holdover condition
7:3	Reserved	Leave as default

Address: **0x0C**
Register Name: **ref_mon_fail_mask (**Control register to mask each failure indicator for ref)
Default Value: 0xFF
Type: R/W

Bit Field	Function Name	Description
0	ref_mon_fail_mask_SCM	Set to 0 (zero) to mask ref SCM failure
1	ref_mon_fail_mask_CFM	Set to 0 (zero) to mask ref CFM failure
2	Reserved	Leave as default
3	ref_mon_fail_mask_PFM	Set to 0 (zero) to mask ref PFM failure

Address: **0x0C**
Register Name: **ref_mon_fail_mask (**Control register to mask each failure indicator for ref)
Default Value: 0xFF
Type: R/W

Bit Field	Function Name	Description
7:4	Reserved	Leave as default

Address: **0x10**
Register Name: **detected_ref_0**
Default Value: **See description**
Type: R

Bit Field	Function Name	Description
3:0	ref_frq_detected	ref auto-detected frequency value 0000: -> 2 kHz 0001: -> 8 kHz 0010: -> 64 kHz 0011: -> 1.544 MHz 0100: -> 2.048 MHz 0101: -> 6.48 MHz 0110: -> 8.192 MHz 0111: -> 16.384 MHz 1000: -> 19.44 MHz 1001: -> 38.88 MHz 1010: -> 77.76 MHz 1111:-> Not yet detected
7:4	Reserved	Leave as default

Address: **0x1D**
Register Name: **dpll_ctrl_0**
Default Value: **See description**
Type: R/W

Bit Field	Function Name	Description
0	reserved	Leave as default
3:1	bandwidth	011: 14 Hz 100: 28 Hz (limited to 14 Hz for 2 kHz references) 101: 890 Hz (limited to 14 Hz and 56 Hz for 2 kHz and 8 kHz references respectively) - default value All other settings are reserved.
7:4	reserved	Leave as default

Address: **0x21**
Register Name: **dpll_ref_fail_mask**
Default Values: 0x3C
Type: R/W

Bit Field	Function Name	Description
3:0	Reserved	Leave as default
7:4	ref_hold_mask	Mask for failure indicators (SCM, CFM and PFM) used for automatic holdover. bit 4: SCM bit 5: CFM bit 6: Reserved (leave as default) bit 7: PFM 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled)

Address: **0x28**
Register Name: **dpll_std_lock_fail**
Default Value: **See description**
Type: R

Bit Field	Function Name	Description
0	holdover	This bit goes high whenever the PLL goes into holdover mode
1	lock	This bit goes high when the PLL is locked to the input reference
2	cur_ref_fail	This bit goes high when ref has a failure.
7:3	Reserved	Leave as default

Address: **0x50**
Register Name: **apll_enable**
Default Value: 0x8F
Type: R/W

Bit Field	Function Name	Description
0	apll_clk_en	1: enable apll_clk 0: apll_clk is set to HiZ
6:1	Reserved	Leave as default
7	apll__en	1: enable the APLL 0: disable the APLL

Address: **0x51**
Register Name: **apll_run**
Default Value: 0x0F
Type: R/W

Bit Field	Function Name	Description
0	apll_clk_run	1: generate apll_clk 0: apll_clk is set low
3:1	Reserved	Leave as default

Address: **0x51**
Register Name: **apll_run**
Default Value: 0x0F
Type: R/W

Bit Field	Function Name	Description
4	f_sel0	Along with eth_en bit selects if the apll_clk output generates SONET/SDH or Ethernet frequencies 0: SONET/SDH clocks 1: Ethernet clocks
5	f_sel_diff	Selects low-speed or high-speed frequency group for diff output 0: Selects the high-speed frequency group 1: Selects the low-speed frequency group
6	eth_en	Select if the APLL generates SONET/SDH **or** Ethernet frequencies 0: SONET/SDH clocks 1: Ethernet clocks
7	Reserved	Leave as default

Address: **0x52**
Register Name: **apll_clk_freq**
Default Value: 0x42
Type: R/W

Bit Field	Function Name	Description
3:0	apll_clk_freq	Sets the frequency of the apll_clk clock output. Refer to Table 3, “APLL LVCMOS Output Clock Frequencies” on page 21 for list of available frequencies
7:4	Reserved	Leave as default

Address: **0x53**
Register Name: **apll_clk_offset90**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
1:0	apll_clk_offset90	apll_clk phase position coarse tuning 00: 00 degrees 01: 90 degrees 10: 180 degrees 11: 270 degrees
7:2	Reserved	Leave as default

Address: **0x55**
Register Name: **apll_offset_fine**
Default Value: **0x00**
Type: **R/W**

Bit Field	Function Name	Description
7:0	apll_offset_fine	Phase alignment fine tuning for the APLL clock path. The delay is defined as an 8-bit two's complement value in 119.2 ps steps.

Address: **0x60**
Register Name: **diff_clk_ctrl**
Default Value: 0xA3
Type: R/W

Bit Field	Function Name	Description
0	Reserved	Leave as default
1	diff_en	1: enable diff 0: diff is set to HiZ
5:2	Reserved	Leave as default
7:6	diff_clk_adjust	Adjusts alignment of differential output to the CMOS outputs in steps of 1.6 ns. A lower value advances the differential output, a higher value delays it. The default value aligns for conditions as specified in the data sheet

Address: **0x61**
Register Name: **diff_clk_sel**
Default Value: 0x55
Type: R/W

Bit Field	Function Name	Description
3:0	Reserved	Leave as default
6:4	diff_sel	Selects the output frequency for diff. Refer to Table 4, “APLL Differential Output Clock Frequencies” on page 22 for specific frequency settings.
7	Reserved	Leave as default

Address: **0x65**
Register Name: **ref_freq_mode_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
1:0	ref_freq_mode	0: Auto_Frequency detect 1: CustomA configuration 2: CustomB configuration 3: Reserved
7:2	Reserved	Leave as default

Address: **0x67**
Register Name: **custA_mult_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.4, “Reference Input“ for detail on this register settings.

Address: **0x68**
Register Name: **custA_mult_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
5:0	custA_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom A frequency. This defined as a multiple of 8 kHz. See section 2.4, “Reference Input“ for detail on this register settings.
7:6	Reserved	Leave as default

Address: **0x69**
Register Name: **custA_scm_low**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_scm_low_lim	Defines the SCM low limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6A**
Register Name: **custA_scm_high**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_scm_high_lim	Defines the SCM high limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6B**
Register Name: **custA_cfm_low_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6C**
Register Name: **custA_cfm_low_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6D**
Register Name: **custA_cfm_hi_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6E**
Register Name: **custA_cfm_hi_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom A frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x6F**
Register Name: **custA_cfm_cycle**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custA_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration A. Set as CFM reference monitoring cycles - 1. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x70**
Register Name: **custA_div**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
0	custA_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.
7:1	Reserved	Leave as default

Address: **0x71**
Register Name: **custB_mult_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_mult7_0	Bits 7:0 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.4, “Reference Input“ for detail on this register settings.

Address: **0x72**
Register Name: **custB_mult_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
5:0	custB_mult13_8	Bits 13:8 of a 14-bit value that defines the input reference Custom B frequency. This defined as a multiple of 8 kHz. See section 2.4, “Reference Input“ for detail on this register settings.
7:6	Reserved	Leave as default

Address: **0x73**
Register Name: **custB_scm_low**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_scm_low_lim	Defines the SCM low limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x74**
Register Name: **custB_scm_high**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_scm_high_lim	Defines the SCM high limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x75**
Register Name: **custB_cfm_low_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_low7_0	Bits 7:0 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x76**
Register Name: **custB_cfm_low_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_low15_8	Bits 15:8 of a 16-bit value that defines the CFM low limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x77**
Register Name: **custB_cfm_hi_0**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_hi7_0	Bits 7:0 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x78**
Register Name: **custB_cfm_hi_1**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_hi15_8	Bits 15:8 of a 16-bit value that defines the CFM high limit for the Custom B frequency. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x79**
Register Name: **custB_cfm_cycle**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
7:0	custB_cfm_cycle	Defines the number of cycles that are monitored in the given sample window for custom configuration B. Set as CFM reference monitoring cycles - 1. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.

Address: **0x7A**
Register Name: **custB_div**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
0	custB_div	When enabled (set to 1) the CFM divides the reference input frequency by 4 to increase the measurement window. This is recommended when the reference frequency is greater than 19.44 MHz. See section 2.6, “Reference Monitoring for Custom Configurations“ for more details.
7:1	Reserved	Leave as default

Address: **0x7E**
Register Name: **predivider_ctrl**
Default Value: 0x00
Type: R/W

Bit Field	Function Name	Description
3:0	ref_div	Reference 0 frequency divide ratio 0000: Divide by 1 0001: Divide by 2 0010: Divide by 3 0011: Divide by 4 0100: Divide by 5 0101: Divide by 6 0110: Divide by 7 0111: Divide by 8 1010: Divide by 1.5. 1100: Divide by 2.5. 1101 - 1111: reserved Note: Output jitter generation may be higher when using divide by 1.5 and 2.5 ratios
7:4	Reserved	Leave as default

5.0 AC and DC Electrical Characteristics

DC Electrical Characteristics - Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	-0.5	4.6	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated.

Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD}, AV_{DD}	3.1	3.3	3.5	V
2	Core supply voltage	V_{CORE}, AV_{CORE}	1.7	1.8	1.9	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated.

DC Electrical Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	1.8 V Core Supply Current	$I_{1.8\_CORE}$		121	159	mA	osci = 20 MHz, All outputs disabled.
2	I/O Supply Current (Differential Outputs)	I_{DIFF}		37	46	mA	All differential outputs operating at max frequency and biased with a 200 Ohm resistor to ground
3	I/O Supply Current (CMOS Outputs)	I_{CMOS}		51	72	mA	All CMOS outputs operating at max frequency and loaded with 15 pF
4	Total Power Dissipation	P_{T_D}		508	715	mW	All outputs operating at max frequency and loaded with 15 pF
5	CMOS high-level input voltage	V_{IH}	$0.7*V_{DD}$			V	Applies to osci pin
6	CMOS low-level input voltage	V_{IL}			$0.3*V_{DD}$	V	
7	Input leakage current	I_{IL}	-15		15	µA	$V_I = V_{DD}$ or 0 V
8	Input leakage current low for pull-up pads	I_{IL_PU}	-121		-23	µA	V_I = 0 V
9	Input leakage current high for pull-down pads	I_{IL_PD}	23		121	µA	$V_I = V_{DD}$
10	Schmitt trigger Low to High threshold point	V_{t+}	1.35		1.85	V	All CMOS inputs are schmitt level triggered
11	Schmitt trigger High to Low threshold point	V_{t-}	0.80		1.15	V	
12	CMOS high-level output voltage	V_{OH}	2.4			V	I_{OH} = 8mA on clk & fp output. I_{OH} = 4mA other outputs
13	CMOS low-level output voltage	V_{OL}			0.4	V	I_{OL}= 8mA on clk & fp output. I_{OL} = 4mA other outputs
14	LVPECL: High-level output voltage	V_{OH_LVPECL}	V_{DD}-1.08	V_{DD}-0.96	V_{DD}-0.88	V	
15	LVPECL: Low-level output voltage	V_{OL_LVPECL}	V_{DD}-1.81	V_{DD}-1.71	V_{DD}-1.62	V	
16	LVPECL: Differential output voltage	V_{OD_LVPECL}	0.6	0.8	0.93	V	

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated.

AC Electrical Characteristics* - Input To Output Timing For Ref Reference (See Figure 21).

	Characteristics	Symbol	Min.	Max.	Units
1	LVCMOS Clock Output (apll_clk)	t_D	-1.0	+4.0	ns
2	LVPECL Differential Clock Output (diff)	t_D	-0.5	+5.5	ns

* Input to output timing is measured over the specified operating voltage and temperature ranges using the same input and output spot frequencies of 2 kHz, 8 kHz, 1.544 MHz, 2.048 MHz, 6.48 MHz, 8.192 MHz, 16.384 MHz, 19.44 MHz, 38.88 MHz, and 77.76 MHz.

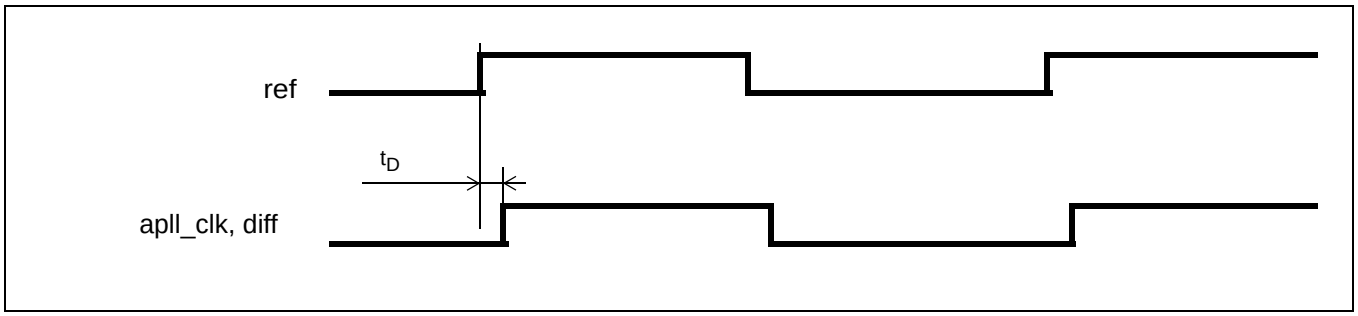


Figure 21 - Input To Output Timing

AC Electrical Characteristics - Output Clock Duty Cycle[1] (See Figure 22).

	Characteristics	Symbol	Min.	Max.	Units	Notes
1	LVCMOS Output Duty Cycle[2]	t_{SYM}	45	55	%	2 kHz < f_{clk} ≤ 125 MHz
			40	60	%	50 MHz
2	LVPECL Output Duty Cycle[3]	t_{SYM}	45	55	%	2 kHz < f_{clk} ≤ 622 MHz
			40	60	%	50 MHz

1. Duty cycle is measured over the specified operating voltage and temperature ranges at specified spot frequencies.

2. Measured on spot frequencies of 1.544 MHz, 2.048 MHz, 3.088 MHz, 4.096 MHz, 6.312 MHz, 8.192 MHz, 8.448 MHz, 16.384 MHz, 25 MHz, 32.768 MHz, 34.368 MHz, 44.736 MHz, 65.536 MHz, 125 MHz.

3. Measured on spot frequencies of 6.48 MHz, 19.44 MHz, 25 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz, 125 MHz, 155.52 MHz, 311.04 MHz, 622.08 MHz.

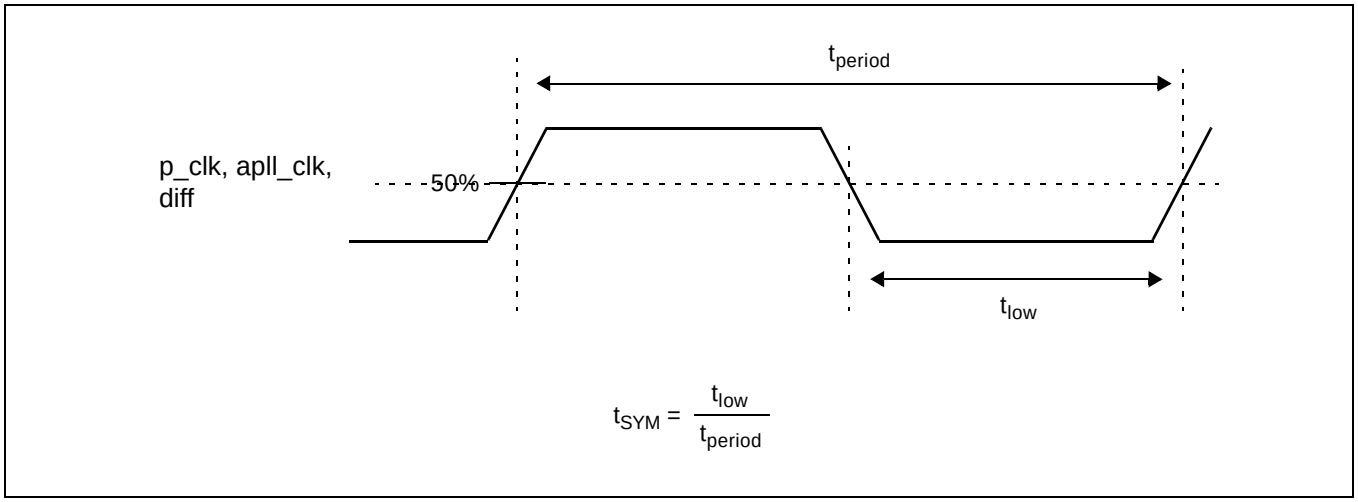


Figure 22 - Output Duty Cycle

AC Electrical Characteristics* - Output Clock Fall and Rise Times[1] (See Figure 23).

	Characteristics	Symbol	Min.	Max.	Units	C_{LOAD}
1	Output Rise Time	t_{rise}	2.3	4.5	ns	30 pF
2	Output Rise Time	t_{rise}	2.0	3.9	ns	25 pF
3	Output Rise Time	t_{rise}	1.6	3.2	ns	20 pF
4	Output Rise Time	t_{rise}	1.3	2.6	ns	15 pF
5	Output Rise Time	t_{rise}	1.0	1.9	ns	10 pF
6	Output Rise Time	t_{rise}	0.6	1.3	ns	5 pF
7	Output Fall Time	t_{fall}	2.1	5.2	ns	30 pF
8	Output Fall Time	t_{fall}	1.8	4.5	ns	25 pF
9	Output Fall Time	t_{fall}	1.5	3.7	ns	20 pF
10	Output Fall Time	t_{fall}	1.2	3.0	ns	15 pF
11	Output Fall Time	t_{fall}	0.9	2.3	ns	10 pF
12	Output Fall Time	t_{fall}	0.6	1.5	ns	5 pF

1. Output fall and rise times are specified over the operating voltage and temperature ranges at 10 MHz.

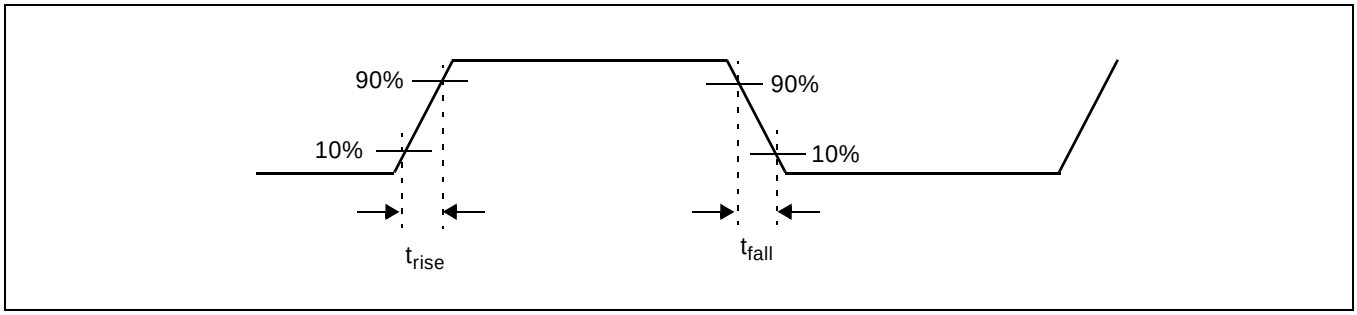


Figure 23 - Output Clock Fall and Rise Times

AC Electrical Characteristics - Serial Peripheral Interface Timing

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 6 - Serial Peripheral Interface Timing

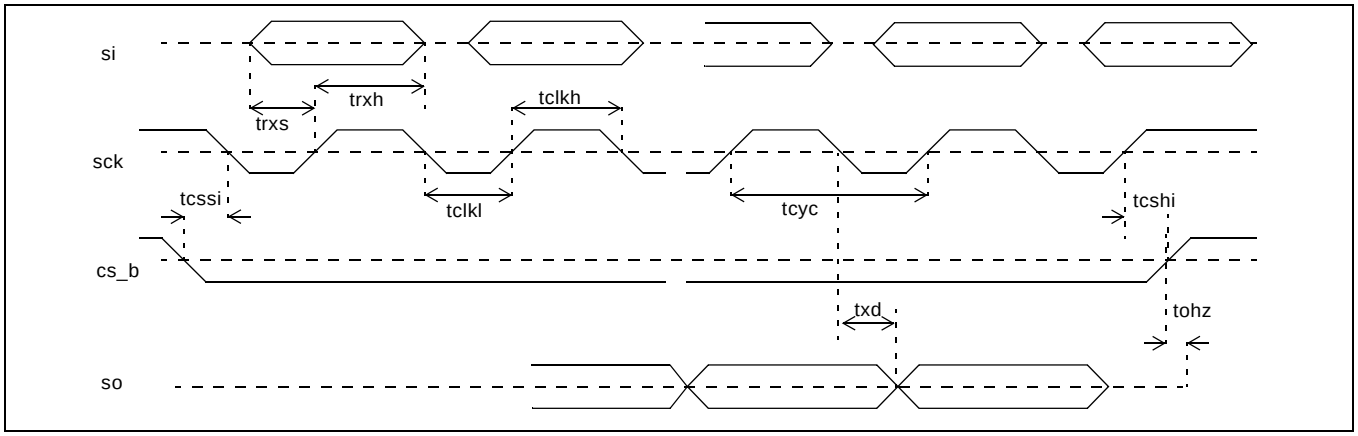


Figure 24 - Serial Peripheral Interface Timing - LSB First Mode

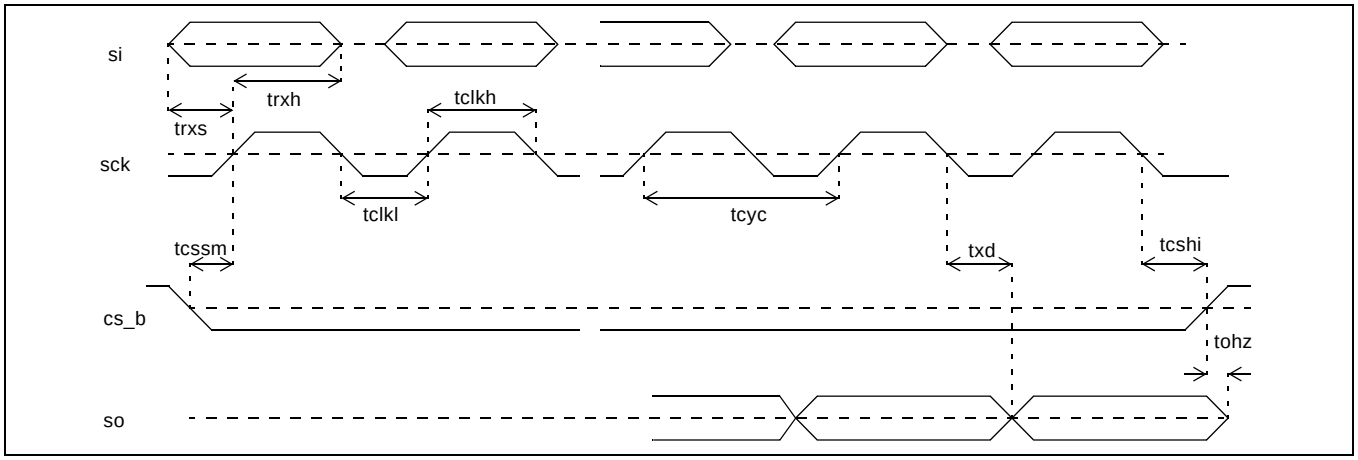


Figure 25 - Serial Peripheral Interface Timing - MSB First Mode

AC Electrical Characteristics - I^2C Timing

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by pull-up resistor
Fall time	t_f	$20 + 0.1C_b$		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 7 - I^2C Serial Microport Timing

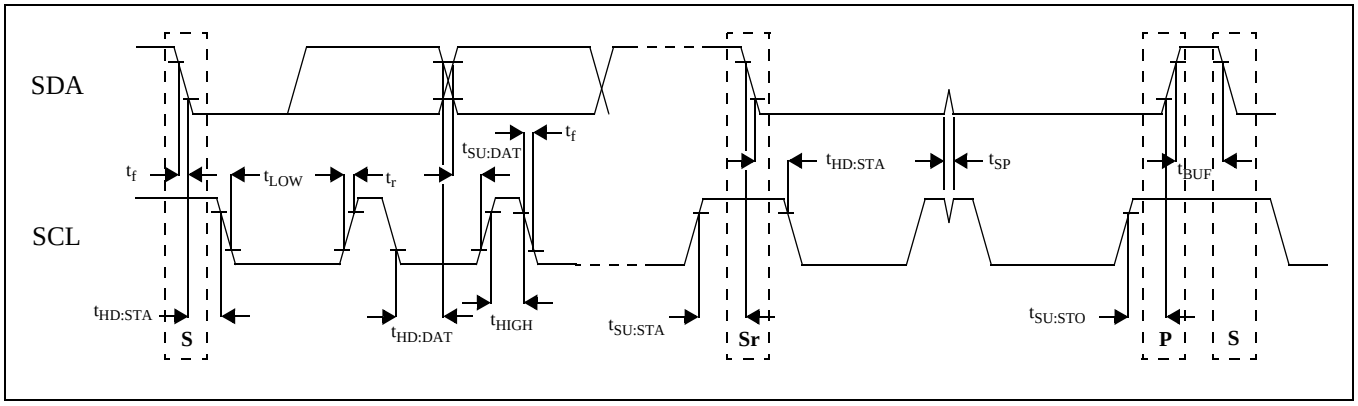


Figure 26 - I^2C Serial Microport Timing

Performance Characteristics - Output Jitter Generation On Differential LVPECL Output (diff) with apll_clk output disabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	1.3	1.7	ps_{RMS}
			0.1 UI_{P-P}	643.00	14.6	17.5	ps_{P-P}
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	643.00	8.7	10.7	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	643.00	8.8	10.9	ps_{P-P}
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.7	1.1	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.0	11.0	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.0	11.1	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.01 UIrms	4.020	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	40.20	8.5	10.6	ps_{P-P}
OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	0.8	1.0	ps_{RMS}
			0.1 UI_{P-P}	40.20	9.5	11.6	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	40.20	8.6	10.7	ps_{P-P}
OC-192	622.08 MHz	50 kHz to 80 MHz	0.01 UIrms	1.00	0.7	0.9	ps_{RMS}
			0.1 UI_{P-P}	10.00	6.9	8.7	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.14	8.2	10.3	ps_{P-P}
		4 MHz to 80 MHz	0.1 UI_{P-P}	10.00	1.8	2.5	ps_{P-P}

Interface	Output Frequency	Jitter Measurement Filter	Jitter Generation		
			Typ[1]	Max[2]	Units
Ethernet Clock Rates	25 MHz	12 kHz to 10 MHz	1.3	1.8	ps_{RMS}
			12.6	16.4	ps_{P-P}
	125 MHz	12 kHz to 20 MHz	0.8	1.0	ps_{RMS}
			9.4	11.7	ps_{P-P}
	156.25 MHz	12 kHz to 20 MHz	0.8	1.0	ps_{RMS}
			9.5	11.6	ps_{P-P}

[1] Typical jitter specifications are measured with the differential outputs enabled and all other outputs disabled when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with the differential outputs enabled and apll_clk output disabled.

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff) with apll_clk output enabled.

Interface	Output Frequency	Jitter Measurement Filter	GR-253 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
OC-3	19.44 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	1.6	2.3	ps_{RMS}
			0.1 UI_{P-P}	643.00	15.4	19.7	ps_{P-P}
	77.76 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.8	1.3	ps_{RMS}
			0.1 UI_{P-P}	643.00	9.2	12.4	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.01 UI_{RMS}	64.30	0.8	1.3	ps_{RMS}
			0.1 UI_{P-P}	643.00	9.3	12.7	ps_{P-P}
OC-12	77.76 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.9	1.5	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.6	13.3	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.01 UI_{RMS}	16.08	0.9	1.4	ps_{RMS}
			0.1 UI_{P-P}	160.80	9.6	13.3	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.01 UIrms	4.020	0.8	1.4	ps_{RMS}
			0.1 UI_{P-P}	40.20	9.1	12.9	ps_{P-P}
OC-48	155.52 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	1.0	1.5	ps_{RMS}
			0.1 UI_{P-P}	40.20	10.1	13.7	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.01 UIrms	4.020	0.8	1.4	ps_{RMS}
			0.1 UI_{P-P}	40.20	9.2	13.0	ps_{P-P}
OC-192	622.08 MHz	50 kHz to 80 MHz	0.01 UIrms	1.00	0.7	1.0	ps_{RMS}
			0.1 UI_{P-P}	10.00	7.3	9.2	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.14	8.6	10.7	ps_{P-P}
		4 MHz to 80 MHz	0.1 UI_{P-P}	10.00	2.1	3.2	ps_{P-P}

Interface	Output Frequency	Jitter Measurement Filter	Jitter Generation		
			Typ[1]	Max[2]	Units
Ethernet Clock Rates	25 MHz	12 kHz to 10 MHz	1.4	1.9	ps_{RMS}
			13.0	16.7	ps_{P-P}
	125 MHz	12 kHz to 20 MHz	0.8	1.0	ps_{RMS}
			9.5	11.7	ps_{P-P}
	156.25 MHz	12 kHz to 20 MHz	0.9	1.1	ps_{RMS}
			9.7	11.8	ps_{P-P}

[1] Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of $25^{o}C$.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with apll_clk output enabled while generating any of the frequencies available from the SONET/SDH/Ethernet synthesizer.

Performance Characteristics - Output Jitter Generation On Differential LVPECL Outputs (diff) with apll_clk output enabled.

Interface	Output Frequency	Jitter Measurement Filter	G.813 Jitter Requirement		Jitter Generation		
					Typ[1]	Max[2]	Units
Option 1							
STM-1	19.44 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	13.9	17.8	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	16.3	20.6	ps_{P-P}
	77.76 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	6.8	9.7	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	10.3	13.6	ps_{P-P}
	155.52 MHz	65 kHz to 1.3 MHz	0.1 UI_{P-P}	643	6.8	9.8	ps_{P-P}
		500 Hz to 1.3 MHz	0.5 UI_{P-P}	3215	10.5	13.9	ps_{P-P}
STM-4	77.76 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	4.8	8.4	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	10.5	14.2	ps_{P-P}
	155.52 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	4.4	5.6	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	10.5	14.3	ps_{P-P}
	622.08 MHz	250 kHz to 5 MHz	0.1 UI_{P-P}	161	3.9	5.0	ps_{P-P}
		1 kHz to 5 MHz	0.5 UI_{P-P}	804	10.0	13.9	ps_{P-P}
STM-16	155.52 MHz	1 MHz to 20 MHz	0.1 UI_{P-P}	40.2	4.0	5.4	ps_{P-P}
		5 kHz to 20 MHz	0.5 UI_{P-P}	201	10.6	14.3	ps_{P-P}
	622.08 MHz	1 MHz to 20 MHz	0.1 UI_{P-P}	40.2	2.4	4.4	ps_{P-P}
		5 kHz to 20 MHz	0.5 UI_{P-P}	201	9.7	13.6	ps_{P-P}
STM-64	622.08 MHz	4 MHz to 80 MHz	0.1 UI_{P-P}	10	2.1	3.2	ps_{P-P}
		20 kHz to 80 MHz	0.5 UI_{P-P}	50.2	8.7	10.7	ps_{P-P}
Option 2							
STM-1	77.76 MHz	12 kHz to 1.3 MHz	0.1 UI_{P-P}	643	9.1	12.4	ps_{P-P}
	155.52 MHz	12 kHz to 1.3 MHz	0.1 UI_{P-P}	643	9.3	12.7	ps_{P-P}
STM-4	77.76 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	9.6	13.3	ps_{P-P}
	155.52 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	9.6	13.3	ps_{P-P}
	622.08 MHz	12 kHz to 5 MHz	0.1 UI_{P-P}	161	9.1	12.9	ps_{P-P}
STM-16	155.52 MHz	12 kHz to 20 MHz	0.1 UI_{P-P}	40.2	10.1	13.7	ps_{P-P}
	622.08 MHz	12 kHz to 20 MHz	0.1 UI_{P-P}	40.2	9.2	13.0	ps_{P-P}
STM-64	622.08 MHz	4 MHz to 80 MHz	0.1 UI_{P-P}	10	2.1	3.2	ps_{P-P}
		20 kHz to 80 MHz	0.3 UI_{P-P}	30.1	8.6	10.7	ps_{P-P}

[1] Typical jitter specifications are measured under the power-up default configuration when operating under nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with apll_clk output enabled while generating any of the frequencies available from the SONET/SDH/Ethernet synthesizer.

Performance Characteristics - Measured Output Jitter On APLL CMOS Output (apll_clk) with the diff output enabled.

Output Frequency	Jitter Measurement Filter	Jitter Generation		
		Typ[1]	Max[2]	Units
SONET/SDH 6.48 MHz, 19.44 MHz, 38.88 MHz, 51.84 MHz, 77.76 MHz	12 kHz to 5 MHz	2.3	3.1	ps_{RMS}
		22.8	28.7	ps_{P-P}
	unfiltered	3.2	4.3	ps_{RMS}
		33.1	42.0	ps_{P-P}
Ethernet 25 MHz	637 kHz to Nyquist	1.7	2.9	ps_{RMS}
		11.8	19.6	ps_{P-P}
	12 kHz to 10 MHz	1.8	2.9	ps_{RMS}
		15.2	22.8	ps_{P-P}
Ethernet 125 MHz	637 kHz to Nyquist	0.6	1.0	ps_{RMS}
		5.0	8.9	ps_{P-P}
	12 kHz to 20 MHz	0.9	1.4	ps_{RMS}
		10.4	14.2	ps_{P-P}

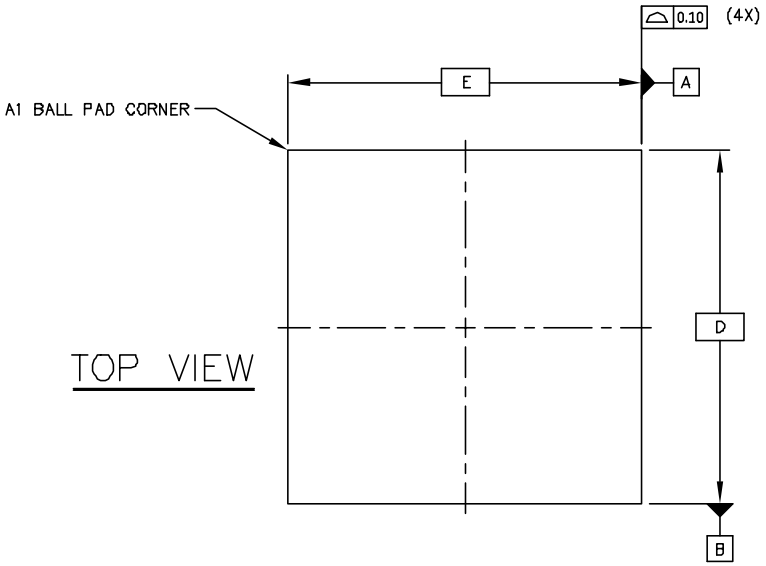
[1] Typical jitter specifications are measured when operating at nominal voltages of 1.8 V and 3.3 V and at an ambient temperature of 25°C.

[2] Maximum jitter specifications takes into account process variations and is measured over the entire operating temperature range and voltage range with the diff output enabled.

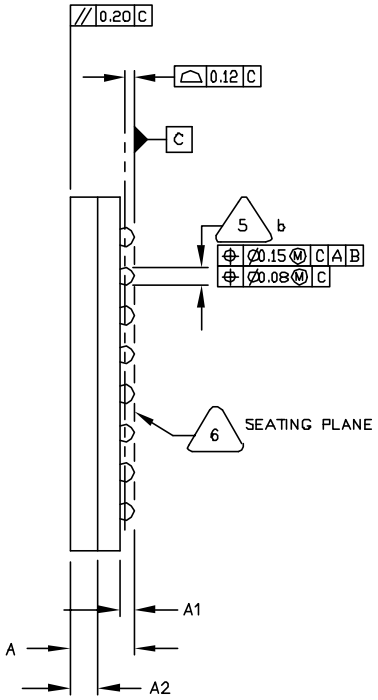
6.0 Thermal Characteristics

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air	31.6	°C/W
Junction to Case Thermal Resistance	θ_{jc}	Still Air	10.3	°C/W

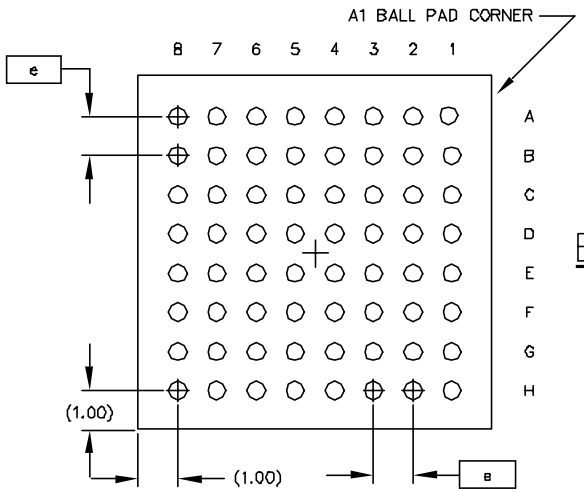
Table 8 - Thermal Data



TOP VIEW



SIDE VIEW



BOTTOM VIEW

64 SOLDER BALLS

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.52	1.62	1.72
A1	0.31	0.36	0.41
A2	0.65	0.70	0.75
b		0.46 Typ.	
D		9.00 REF.	
E		9.00 Ref.	
e		1.0 Ref	
n		64	

6. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

5. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.

4. THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS IS 64.

3. Not to Scale.

2. THE BASIC SOLDER BALL GRID PITCH IS 1.00mm.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

ISSUE	1			
ACN	CDCA			
DATE	15April05			
APPRD.				

Microsemi

Previous package codes

N/A

Package Code GG

Package Outline for 64ball 9x9mm, 1.0 mm Pitch, 4 layer, CABGA

111039