ZL30254

2-In, 2-Out 8kHz/25MHz to 125/156.25MHz Clock Multiplier and Jitter Attenuator

Data Sheet

April 2016

Features

Input Clocks

- Two CMOS inputs, both 8kHz or 25MHz
- Inputs continually monitored for frequency accuracy (±1%)
- Automatic revertive reference switching

Low-Bandwidth DPLL

- 25Hz bandwidth for jitter attenuation
- ±120ppm tracking range
- Digital hold on loss of all inputs

Clock Multiplier APLL and Output Clocks

- Easy-to-configure, encapsulated design requires no external VCXO or loop filter components
- Two CML outputs, both 125MHz or 156.25MHz
- Outputs easily interface with CML, LVDS or LVPECL components
- Output jitter <1ps RMS (12kHz-20MHz)

Ordering Information

ZL30254LDG1	32 Pin QFN	Trays
ZL30254LDF1	32 Pin QFN	Tape and Reel

Matte Tin

Package size: 5 x 5 mm

-40°C to +85°C

General Features

- Operates from low-cost 49.152MHz fundamental-mode crystal
- Status output pins indicate selected input clock, holdover, and locked/unlocked states
- Input clock selection control pin

Applications

- Jitter attenuation, reference selection from dual 8kHz or 25MHz inputs, frequency multiplication to 125MHz or 156.25MHz

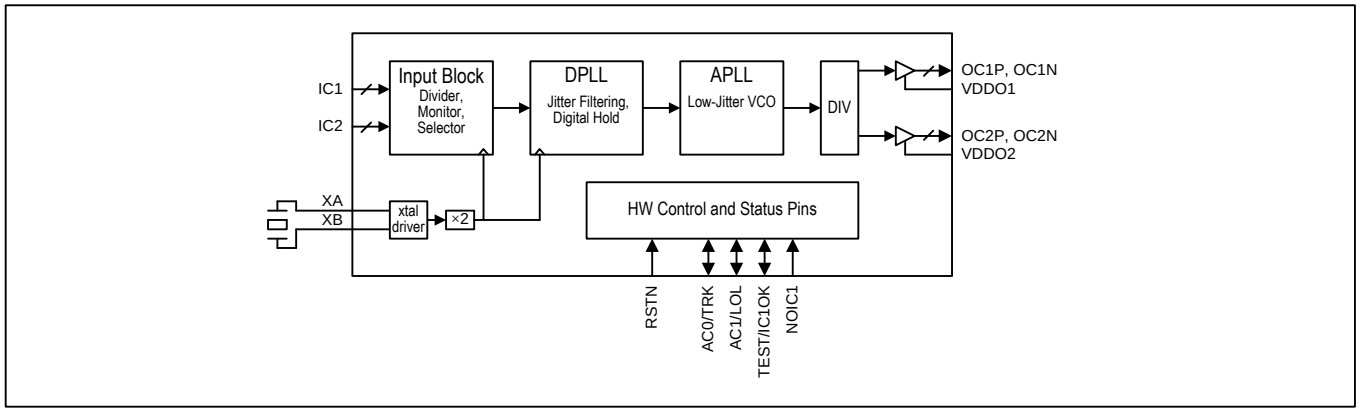


Figure 1 - Functional Block Diagram

1. Application Examples

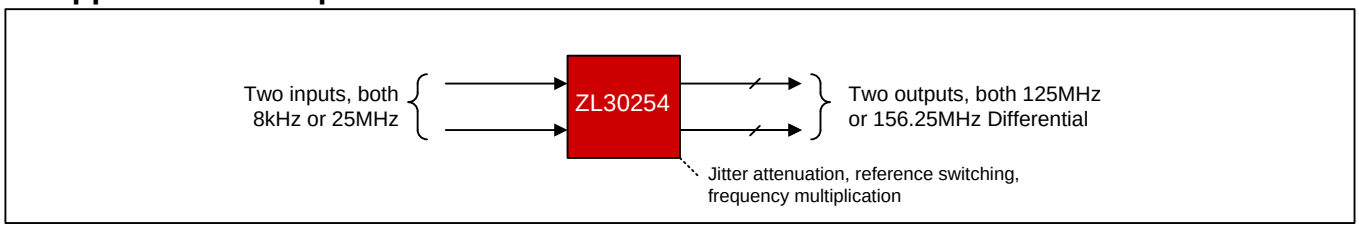


Figure 2 – Typical Application

2. Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

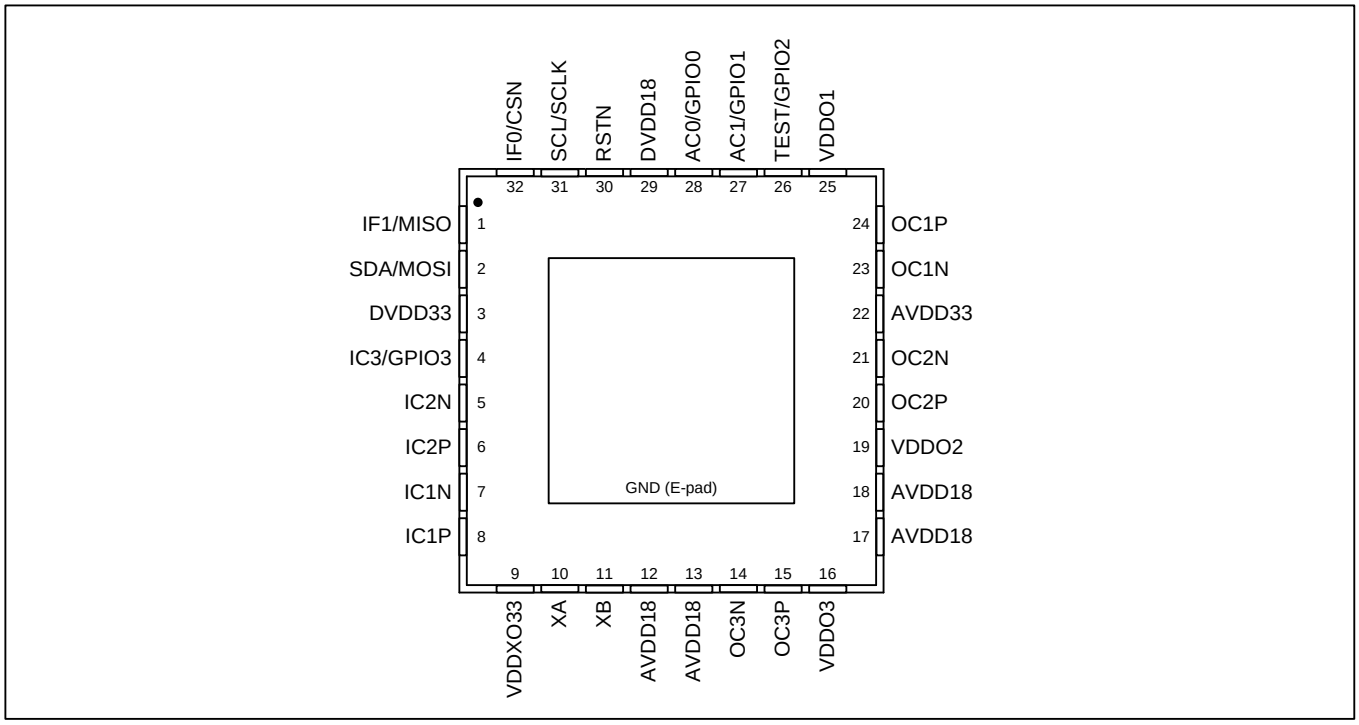


Figure 3 - Pin Diagram

3. Pin Descriptions

All device inputs and outputs are LVCMOS unless described otherwise. The Type column uses the following symbols: I – input, I_{PU} – input with 50kΩ internal pullup resistor, O – output, A – analog, P – power supply pin..

Table 1 - Pin Descriptions

<table>
<tr><th>Pin #</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>8
6</td><td>IC1
IC2</td><td>I</td><td>Input Clock Pins
Single-ended signal format. For input signal amplitude >2.5V, connect the signal directly to the pin. For input signal amplitude ≤2.5V, AC-couple the signal to the pin.</td></tr>
<tr><td>10
11</td><td>XA
XB</td><td>A / I</td><td>Crystal Pins
An on-chip crystal driver circuit is designed to work with an external crystal connected to the XA and XB pins. See section 4.1.2 for crystal characteristics and recommended external components.</td></tr>
<tr><td>24
23
20
21</td><td>OC1P
OC1N
OC2P
OC2N</td><td>O</td><td>Output Clock Pins
CML signal format. See Table 8 and Figure 6 for electrical specifications and recommended external circuitry for interfacing to LVDS, LVPECL or CML input pins on neighboring devices.</td></tr>
<tr><td>30</td><td>RSTN</td><td>I_{PU}</td><td>Reset (Active Low). When this global asynchronous reset is pulled low, all internal circuitry is reset to default values. The device is held in reset as long as RSTN is low. Minimum low time is 100ms.</td></tr>
<tr><td>28
27</td><td>AC0/TRK
AC1/LOL</td><td>I/O</td><td>Auto-Configure [1:0] Inputs / DPLL Tracking and Loss-of-Lock Outputs

Auto Configure: On the rising edge of RSTN these pins behave as AC[1:0] and specify one of four I/O frequency combinations:

<table>
<tr><th>AC1</th><th>AC0</th><th>IC1</th><th>IC2</th><th>OC1</th><th>OC2</th></tr>
<tr><td>0</td><td>0</td><td>8kHz</td><td>8kHz</td><td>125MHz</td><td>125MHz</td></tr>
<tr><td>0</td><td>1</td><td>8kHz</td><td>8kHz</td><td>156.25MHz</td><td>156.25MHz</td></tr>
<tr><td>1</td><td>0</td><td>25MHz</td><td>25MHz</td><td>125MHz</td><td>125MHz</td></tr>
<tr><td>1</td><td>1</td><td>25MHz</td><td>25MHz</td><td>156.25MHz</td><td>156.25MHz</td></tr>
</table>

DPLL Tracking and Loss-of-Lock Outputs: After reset these pins are TRK and LOL. They indicate DPLL state as follows:

<table>
<tr><th>TRK</th><th>LOL</th><th>DPLL State</th></tr>
<tr><td>0</td><td>0</td><td>Digital hold</td></tr>
<tr><td>0</td><td>1</td><td>Digital hold</td></tr>
<tr><td>1</td><td>0</td><td>Tracking and locked to selected input</td></tr>
<tr><td>1</td><td>1</td><td>Tracking but not locked to selected input.
IC1OK pin indicates which input (1=IC1, 0=IC2).</td></tr>
</table>

Any pullup or pulldown resistors used to set the values of these pins at reset should be 1kΩ.</td></tr>
<tr><td>26</td><td>TEST/IC1OK</td><td>I/O</td><td>Factory Test Input / IC1 OK Status Output

Factory Test: On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN. A pulldown resistor used to set the value of this pin at reset should be 1kΩ.

IC1OK Status Output: 0=IC1 is invalid, 1=IC1 is valid</td></tr>
</table>

Pin #	Name	Type	Description
4	NOIC1	I/O	**No (Invalidate) IC1 Input** 0 = IC1 status determined normally by internal monitor 1 = IC1 forced invalid, DPLL switches to IC2 (if IC2 valid) or digital hold (if IC2 invalid)
32	TST0	I/O	**Factory Test Pin.** Pin must be wired to DVDD33 through a resistor (10kΩ recommended).
1	TST1	I/O	**Factory Test Pin.** Pin must be wired to DVDD33 through a resistor (10kΩ recommended).
2	TST2	I/O	**Factory Test Pin.** Pin must be wired to DVDD33 through a resistor (10kΩ recommended).
31	TST3	I/O	**Factory Test Pin.** Pin must be wired to DVDD33 through a resistor (10kΩ recommended).
7	CAP1	A	**Capacitor 1 to VSS** Connect a 0.1µF capacitor between this pin and VSS. Pin is internally biased to approximately 1.3V. Do not connect to anything else including other CAP pin.
5	CAP2	A	**Capacitor 2 to VSS** Connect a 0.1µF capacitor between this pin and VSS. Pin is internally biased to approximately 1.3V. Do not connect to anything else including other CAP pin.
12 13 17 18	AVDD18	P	**Analog Power Supply.** 1.8V ±5%.
22	AVDD33	P	**Analog Power Supply.** 3.3V ±5%.
29	DVDD18	P	**Digital Power Supply.** 1.8V ±5%.
3	DVDD33	P	**Digital Power Supply.** 3.3V ±5%.
25	VDDO1	P	**Output OC1 Power Supply.** 3.3V ±5%.
19	VDDO2	P	**Output OC2 Power Supply.** 3.3V ±5%.
16	VDD33	P	**Power Supply.** 3.3V ±5%.
9	VDDXO33	P	**Analog Power Supply for Crystal Driver Circuitry.** 3.3V ±5%.
14 15	DNC		**Do Not Connect to these pins.**
E-pad	VSS	P	**Ground. 0 Volts.**

4. Functional Description

4.1 Local Oscillator or Crystal

Section 4.1.1 describes how to connect an external oscillator and the required characteristics of the oscillator. Section 4.1.2 describes how to connect an external crystal to the on-chip crystal driver circuit and the required characteristics of the crystal.

4.1.1 External Oscillator

A signal from an external oscillator can be connected to the XA pin (XB must be left unconnected).

Table 6 specifies the range of possible frequencies for the XA input. Several vendors including Vectron, Rakon and TXC offer low-cost, low-jitter XOs with output frequencies in this range. To minimize jitter, the signal must be properly terminated and must have very short trace length. A poorly terminated single-ended signal can greatly increase output jitter, and long single-ended trace lengths are more susceptible to noise.

The jitter on output clock signals depends on the phase noise and frequency of the external oscillator. For the device to operate with the lowest possible output jitter, the external oscillator should have the following characteristics:

- Phase Jitter: less than 0.1ps RMS over the 12kHz to 5MHz integration band
- Frequency: The higher the better, all else being equal

4.1.2 External Crystal and On-Chip Driver Circuit

The on-chip crystal driver circuit is designed to work with a fundamental mode, AT-cut crystal resonator. See Table 2 for recommended crystal specifications.

See Figure 4 for the crystal equivalent circuit and the recommended external capacitor connections. To achieve a crystal load (C_L) of 10pF, an external 16pF is placed in parallel with the 4pF internal capacitance of the XA pin, and an external 16pF is placed in parallel with the 4pF internal capacitance of the XB pin. The crystal then sees a load of 20pF in series with 20pF, which is 10pF total load. Note that the 16pF capacitance values in Figure 4 include all capacitance on those nodes. If, for example, PCB trace capacitance between crystal pin and IC pin is 2pF then 14pF capacitors should be used to make 16pF total.

The crystal, traces, and two external capacitors should be placed on the board as close as possible to the XA and XB pins to reduce crosstalk of active signals into the oscillator. Also no active signals should be routed under the crystal circuitry.

Note: Crystals have temperature sensitivies that can cause frequency changes in response to ambient temperature changes. In applications where significant temperature changes are expected near the crystal, it is recommended that the crystal be covered with a thermal cap, or an external XO or TCXO should be used instead.

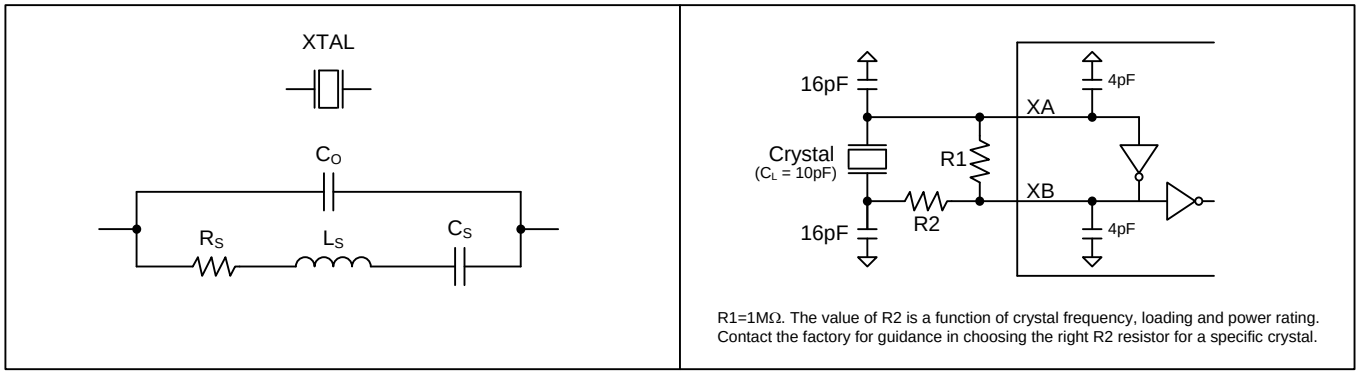


Figure 4 - Crystal Equivalent Circuit / Recommended Crystal Circuit

Table 2 - Crystal Selection Parameters

Parameter		Symbol	Min.	Typ.	Max.	Units
Crystal oscillation frequency[1]		f_{OSC}		49.152		MHz
Shunt capacitance		C_O		2	5	pF
Load capacitance		C_L		10		pF
Equivalent series resistance (ESR)[2]	f_{OSC} < 40MHz	R_S			60	Ω
	f_{OSC} > 40MHz	R_S			50	Ω
Maximum crystal drive level			100			µW

Note 1: Higher frequencies give lower output jitter, all else being equal.
Note 2: These ESR limits are chosen to constrain crystal drive level to less than 100µW. If the crystal can tolerate a drive level greater than 100µW then proportionally higher ESR is acceptable.

Parameter	Symbol	Min.	Typ.	Max.	Units
Crystal Frequency Stability vs. Power Supply	f_{FVD}		0.2	0.5	ppm per 10% Δ in VDD

4.1.3 Clock Doubler

Figure 1 shows the clock doubler ("x2" block) following the crystal driver block. The doubler is used to double the frequency of the internal crystal driver circuit or a clock signal on the XA pin.

The duty cycle of the input clock to the doubler must be as close to 50% as possible because a non-50% duty cycle causes cycle-to-cycle jitter in the doubler's output signal.

4.2 Input Clocks

The IC1 and IC2 input clocks signals are CMOS signal format. The frequency of the two inputs is either 8kHz or 25MHz as specified by the setting of the AC0 and AC1 pins at device reset. See Table 1 for details.

4.2.1 Input Clock Monitoring

Each ICx input clock is continuously monitored for activity and frequency accuracy. The activity monitor counts the number of input clock cycles that occur during a configurable interval. This provides the fastest detection when the input clock is stopped or far off frequency. Frequency monitoring is handled by a percent frequency monitor (±1%). Any input clock that fails activity monitoring or frequency monitoring is declared invalid.

4.2.2 Input Clock Selection

During normal operation, the device automatically selects input clock IC1 if it is valid; otherwise it selects IC2 if it is valid; otherwise the device goes into digital hold (see section 4.3.1). Switching among inputs is revertive, i.e. if the device is locked to IC2 and IC1 becomes valid then the device will automatically switch back to IC1.

The NOIC1 pin can be used to perform manual selection of an input clock. When NOIC1 is high, IC1 is forced invalid. The device then switches to IC2 if it is valid; otherwise the device goes into digital hold.

4.3 DPLL

Digital PLLs have stable, repeatable performance that is insensitive to process variations, temperature, and voltage. The DPLL in this device uses a digitally controlled oscillator (DCO) to generate the DPLL output clock. The DPLL output clock is then provided to an APLL for clock multiplication.

The DPLL in the device has a fixed 25Hz bandwidth and a ±120ppm tracking range. (Note that the crystal is the measurement reference for this tracking range. A ppm offset of the crystal causes a corresponding ppm offset of the tracking range.)

No knowledge of loop equations or gain parameters is required to configure and operate the device. No external components are required for the DPLL except a crystal or XO connected to the XA pin to provide the DPLL's master clock (see section 4.1).

4.3.1 DPLL States

Tracking (Locked and Unlocked). When a valid input clock is available, the DPLL transitions to the tracking state (TRK=1) and is either locked to an input clock (LOL=0) or unlocked (LOL=1).

Digital-Hold. When all input clocks become invalid, the DPLL enters the digital-hold state (TRK=0) in which the output frequency has the same fractional frequency offset it had previously when the DPLL was locked to an input clock. The DPLL automatically transitions from the digital-hold state back to the tracking state when an input clock is declared valid.

4.4 Clock Multiplier APLL

The low-jitter clock-multiplier APLL in the device is self-contained and requires no external components and no knowledge of loop equations. It is factory-configured for 125MHz or 156.25MHz output clocks.

4.5 Output Clock Signals

The OC1 and OC2 output clock signals are CML signal format. The frequency of the two outputs is either 125MHz or 156.25MHz as specified by the setting of the AC0 and AC1 pins at device reset. See Table 1 for details.

4.6 Reset Logic

The RSTN pin asynchronously resets the entire device. When the RSTN pin is low all internal registers are reset to their default values. **The RSTN pin must be asserted once after power-up.** Reset should be asserted for at least 100ms. After reset is deasserted the device requires approximately 100ms to configure itself and be ready to operate.

4.7 Power-Supply Considerations

Due to the multi-power-supply nature of the device, some I/Os have parasitic diodes between a 1.8V supply and a 3.3V supply. When ramping power supplies up or down, care must be taken to avoid forward-biasing these diodes because it could cause latchup. Two methods are available to prevent this. The first method is to place a Schottky diode external to the device between the 1.8V supply and the 3.3V supply to force the 3.3V supply to be within one parasitic diode drop of the 1.8V supply. The second method is to ramp up the 3.3V supply first and then ramp up the 1.8V supply.

5. Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	-0.3	1.98	V
Supply voltage, nominal 3.3V	VDD33	-0.3	3.63	V
Voltage on any I/O pin	VPIN	-0.3	5.5	V
Storage Temperature Range	T_{ST}	-55	+125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (VSS) unless otherwise stated.

Note 1: The typical values listed in the tables of Section 5 are not production tested.
Note 2: Specifications to -40°C and 85°C are guaranteed by design or characterization and not production tested.

Table 3 - Recommended DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Supply voltage, nominal 1.8V	VDD18	1.71	1.8	1.89	V
Supply voltage, nominal 3.3V	VDD33	3.135	3.3	3.465	V
Operating temperature	T_A	-40		+85	°C

Table 4 - Electrical Characteristics: Supply Currents

Characteristics	Symbol	Min.	Typ.	Max	Units	Notes
Total current, all 1.8V supply pins	I_{DD18}		155	TBD	mA	Note 1
Total current, all 3.3V supply pins	I_{DD33}		153	TBD	mA	Note 1

Note 1: Typical values measured at 1.80V and 3.30V supply voltages and 25°C ambient temperature.

Table 5 - Electrical Characteristics: Non-Clock CMOS Pins

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, all digital inputs	V_{IH}	2.0			V	
Input low voltage, all digital inputs	V_{IL}			0.8	V	
Input leakage current, RSTN pin	I_{ILPU}	-85		10	µA	Note 1
Input leakage current, all other digital inputs	I_{IL}	-10		10	µA	Note 1
Input capacitance	C_{IN}		3	10	pF	
Output leakage (when high impedance)	I_{LO}	-10		10	µA	Note 1
Output high voltage	V_{OH}	2.4			V	I_O = -3.0mA
Output low voltage	V_{OL}			0.4	V	I_O = 3.0mA

Note 1: $0V < V_{IN} <$ VDD33 for all other digital inputs.

Table 6 - Electrical Characteristics: XA Clock Input

This table covers the case when there is no external crystal connected and an external oscillator or clock signal is connected to the XA pin.

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, XA	V_{IH}	1.65			V	
Input low voltage, XA	V_{IL}			0.8	V	
Input frequency on XA pin	f_{IN}		49.152		MHz	
Minimum input clock high, low time	t_H, t_L		3		ns	

Table 7 - Electrical Characteristics: Clock Inputs, IC1 and IC2

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Input high voltage, all digital inputs	V_{IH}	2.0			V	Note 1
Input low voltage, all digital inputs	V_{IL}			0.8	V	
Minimum input clock high, low time	t_H, t_L		3		ns	
Input resistance, single-ended to VDD18	$R_{INVDD18}$		50		kΩ	
Input resistance, single-ended to VSS	R_{INVSS}		130		kΩ	

Note 1: Signals with amplitude greater than 2.5V must be DC-coupled. Signals with amplitudes less than 2.5V should be AC coupled.

Table 8 - Electrical Characteristics: Clock Outputs

Characteristics	Symbol	Min.	Typ.	Max.	Units	Notes
Output frequency	f_{OCML}		125 or 156.25		MHz	
Output high voltage, single-ended, OCxP or OCxN	$V_{OH,S}$		VDDOx – 0.2		V	AC coupled to 50Ω termination
Output low voltage, single-ended, OCxP or OCxN	$V_{OL,S}$		VDDOx – 0.6		V	
Output common mode voltage	$V_{CM,S}$		VDDOx – 0.4		V	
Output differential voltage	$\|V_{OD,S}\|$	320	400	500	mV	
Output differential voltage, peak-to-peak	$\|V_{OD,S,PP}\|$	640	800	1000	mV_{P-P}	
Difference in Magnitude of Differential Voltage for Complementary States	V_{DOS}			50	mV	
Output Rise/Fall Time	t_R, t_F		150		ps	20%-80%
Output Duty Cycle		45	50	55	%	
Output Impedance	R_{OUT}		50		Ω	Single Ended, to VDDOx
Mismatch in a pair	ΔR_{OUT}			10	%	

Note 1: The differential CML outputs can easily be interfaced to LVDS, LVPECL, CML and other differential inputs on neighboring ICs using a few external passive components. See Figure 6 for details.

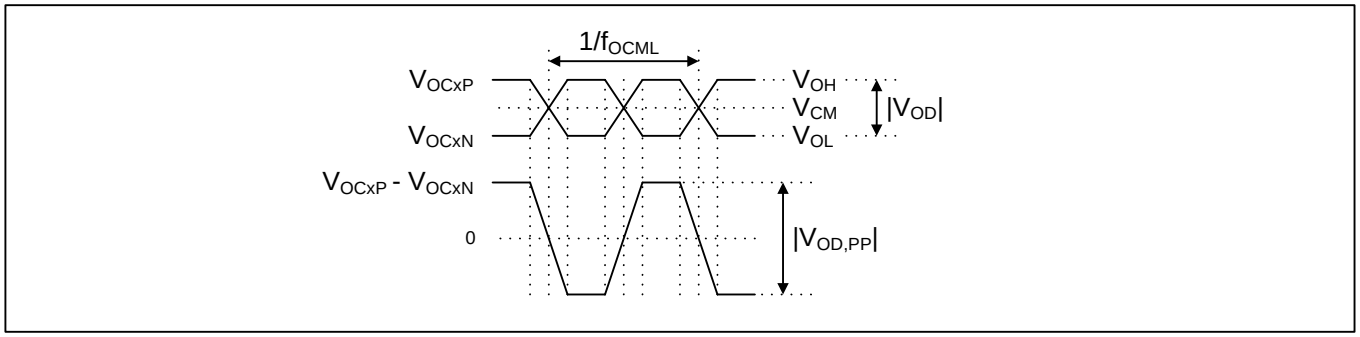


Figure 5 - Electrical Characteristics: CML Clock Outputs

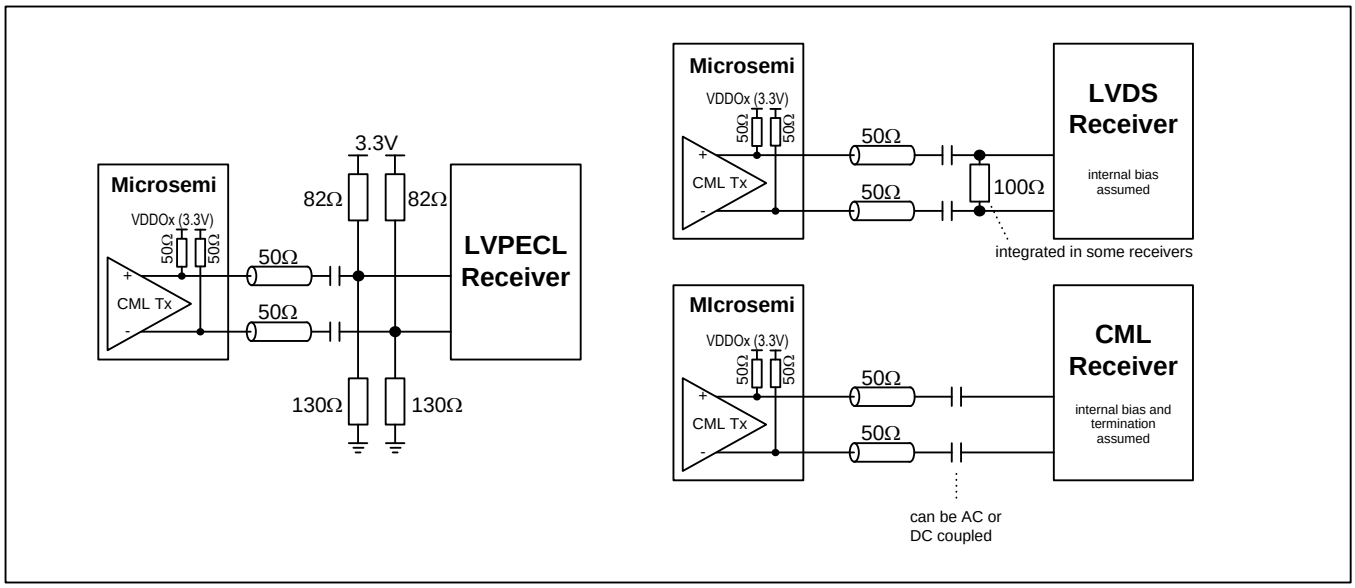


Figure 6 – Example External Components for CML Output Signals

Table 9 - Electrical Characteristics: Output Jitter Performance

Characteristics	Min.	Typ.	Max.	Units	Notes
125MHz output			1	ps rms	12kHz - 20MHz
156.25MHz output			1	ps rms	12kHz - 20MHz

6. Package and Thermal Information

Table 10 - 5x5mm QFN Package Thermal Properties

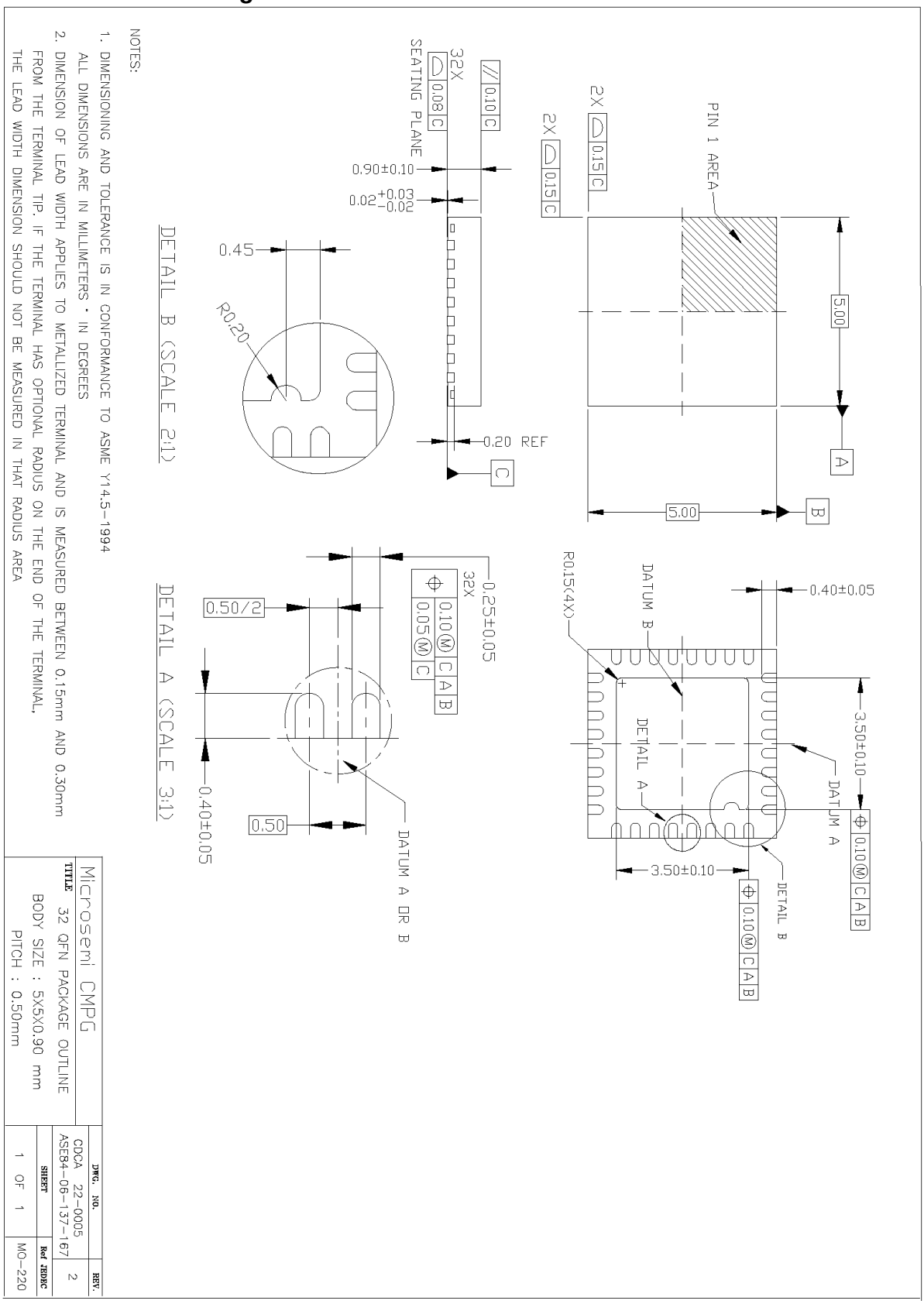
PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance (Note 1)	θ_{JA}	still air	29.6	°C/W
		1m/s airflow	23.3	
		2.5m/s airflow	20.6	
Junction to Board Thermal Resistance	θ_{JB}		9.8	°C/W
Junction to Case Thermal Resistance	θ_{JC}		17.5	°C/W
Junction to Pad Thermal Resistance (Note 2)	θ_{JP}	Still air	3.4	°C/W
Junction to Top-Center Thermal Characterization Parameter	ψ_{JT}	Still air	0.2	°C/W

Note 1: Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power.

Note 2: Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package.

Note 3: For all numbers in the table, the exposed pad is connected to the ground plane with a 5x5 array of thermal vias; via diameter 0.33mm; via pitch 0.76mm.

7. Mechanical Drawing



8. Data Sheet Revision History

Revision	Description
23-Jun-2013	First general release
23-Mar-2015	In Table 1 and section 4.6 changed the minium reset active time to 100ms. In Table 1 added requirement to AC[1:0] and TEST pins that any pullup or pulldown resistors used to set the values of these pins at reset should be 1kΩ. Changed the VDDO1 and VDDO2 descriptions in Table 1 to clearly indicate that VDDO1 is for output OC1 and VDDO2 is for output OC2. Modified Figure 6. In the LVDS diagram removed the 5kΩ resistors to ground, which are only appropriate for one type of LVDS receiver design. Added 100Ω differential termination and note about how it may be integrated in some receivers. Added note that internal bias and termination is assumed for the CML receiver diagram.
19-Apr-2016	Corrected Figure 3 to have square corners rather than chamfered corners to match the mechanical drawing in section 7. Added Note 3 to Table 10.