Ten LVCMOS Output Low Additive Jitter Fanout Buffer

Features

- 3 to 1 input Multiplexer: Two inputs accept any differential (LVPECL, HCSL, LVDS, SSTL, CML, LVCMOS) or a single ended signal and the third input accepts a crystal or a single ended signal
- Ten 1.5V/1.8V/2.5V/3.3V LVCMOS outputs
- Supports frequencies from 0 to 200MHz
- Supports crystals from 8MHz to 60MHz
- Ultra-low additive jitter: 17fs (12kHz to 20MHz)
- Ultra-low noise floor of -170dBc/Hz
- Supports 2.5V or 3.3V power supplies
- Output to output skew of 30ps (typical)
- Input to output delay of 2ns (typical)

Ordering Information

ZL40241LDG1	32 Pin QFN	Trays
ZL40241LDF1	32 pin QFN	Tape and Reel

Package size: 5 x 5 mm

-40°C to +85°C

Applications

- General purpose clock distribution
- Low jitter clock trees
- Logic translation
- Clock and data signal restoration
- Wired and Wireless communications
- High performance microprocessor clock distribution
- Medical Imaging
- Test equipment

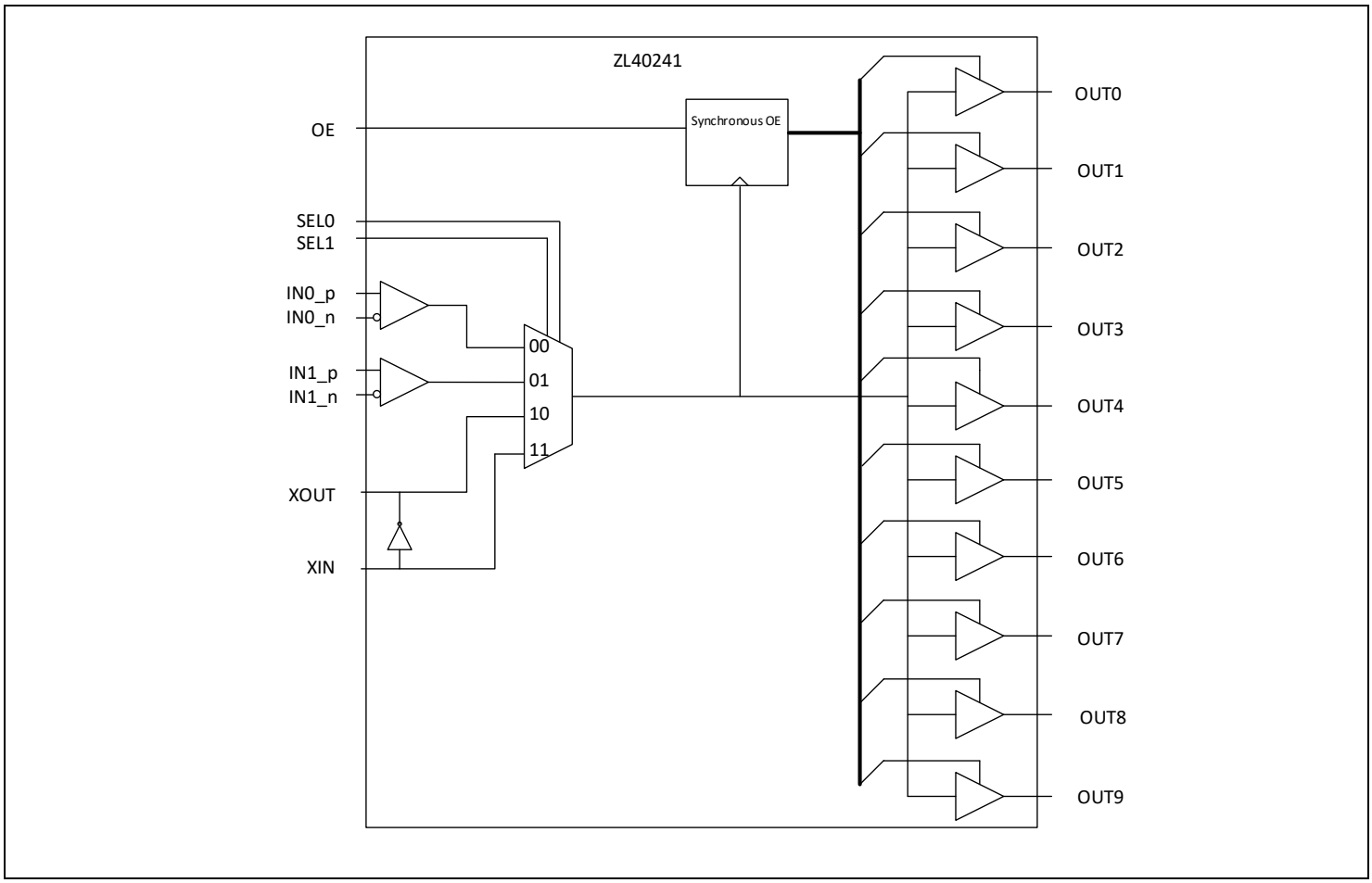

Figure 1. Functional Block Diagram

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Pin Diagram

The device is packaged in a 5x5mm 32-pin QFN.

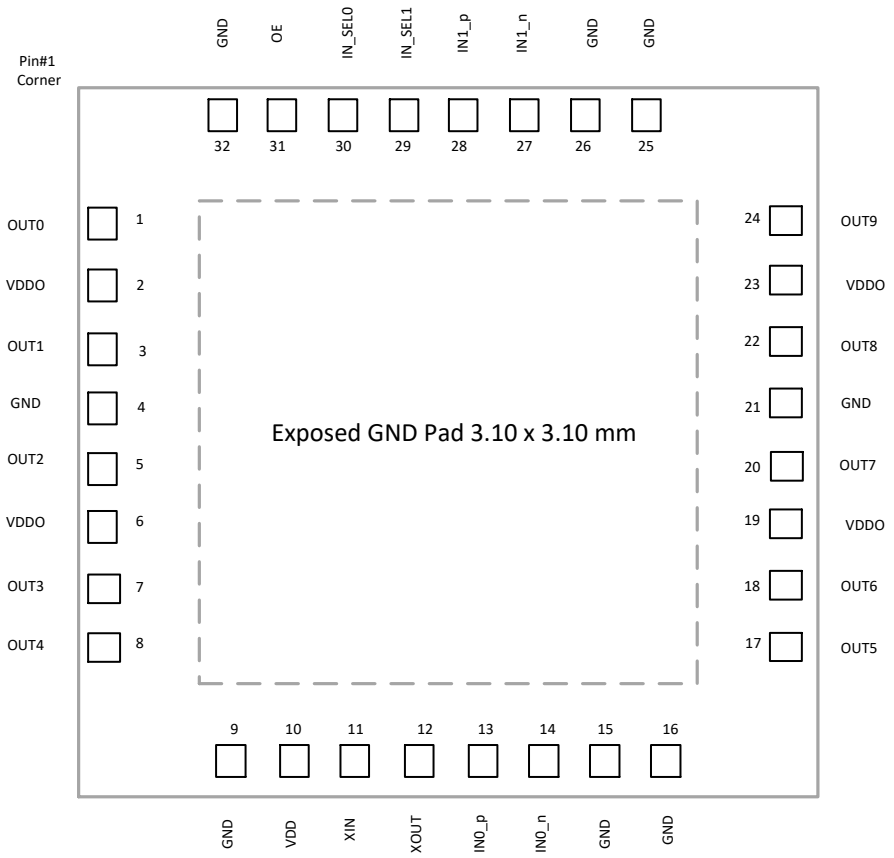


Figure 2. Pin Diagram

Pin Descriptions

All device inputs and outputs are LVPECL unless described otherwise. The I/O column uses the following symbols: I – input, I_{PU} – input with 300kΩ internal pull-up resistor, I_{PD} – input with 300kΩ internal pull-down resistor, I_{APU} – input with 30kΩ internal pull-up resistor, I_{APD} – input with 30kΩ internal pull-down resistor, $I_{APU/APD}$ – input biased at VDD/2 with 60kΩ internal pull-up and 60kΩ pull-down resistors, O – output, I/O – Input/Output pin, P – power supply pin.

Table 1 · Pin Descriptions

<table>
<tr><th>#</th><th>Name</th><th>I/O</th><th>Description</th></tr>
<tr><td colspan="4">Input Reference</td></tr>
<tr><td>13
14
28
27</td><td>IN0_p
IN0_n
IN1_p
IN1_n</td><td>I_{APD}
$I_{APU/APD}$
I_{APD}
$I_{APU/APD}$</td><td>Input Differential or Single Ended References 0 and 1

Input frequency range 0Hz to 200MHz.

Non-inverting inputs (_p) are pulled down with internal 30kΩ pull-down resistors. Inverting inputs (_n) are biased at VDD/2 with 60kΩ pull-up and pull-down resistors to keep inverting input voltages at VDD/2 when inverting inputs are left floating (device fed with a single ended reference).</td></tr>
<tr><td colspan="4">Output Clocks</td></tr>
<tr><td>1
3
5
7
8
17
18
20
22
24</td><td>OUT0
OUT1
OUT2
OUT3
OUT4
OUT5
OUT6
OUT7
OUT8
OUT9</td><td>O</td><td>Ultra-Low Additive Jitter LVCMOS Outputs 0 to 9

Output frequency range 0 to 200MHz</td></tr>
<tr><td colspan="4">Control</td></tr>
<tr><td>30
29</td><td>IN_SEL0
IN_SEL1</td><td>I_{PD}</td><td>Input select pins. Logic level on these pins selects which input will be passed to the output.

<table>
<tr><th>IN_SEL1</th><th>IN_SEL0</th><th>OUTN</th></tr>
<tr><td>0</td><td>0</td><td>Input 0 (IN0)</td></tr>
<tr><td>0</td><td>1</td><td>Input 1 (IN1)</td></tr>
<tr><td>1</td><td>0</td><td>Crystal Oscillator or overdrive</td></tr>
<tr><td>1</td><td>1</td><td>Crystal Bypass</td></tr>
</table>
</td></tr>
</table>

31	OE	I_{PD}	**Output Enable** When high outputs are enabled. When low outputs are high-Z.
Crystal Oscillator			
11	XIN	I	**Crystal Oscillator Input or crystal bypass mode or crystal overdrive mode** If crystal oscillator is not used pull down this pin or connect it to ground.
12	XOUT	O	**Crystal Oscillator Output**
Power and Ground			
10	VDD	P	**Positive Supply Voltage.** Connect to 3.3V or 2.5V supply. VDD voltage must be higher or equal to VDDO.
2 6 19 23	VDDO	P	**Positive Supply Voltage for LVCMOS Outputs** Connect 3.3V, 2.5V, 1.8V or 1.5V power supply
4 9 15 16 21 25 26 32	GND	P	**Ground** Connect to ground
E-Pad	GND	P	**Ground.** Connect to ground

Functional Description

The ZL40241 is a pin controlled low additive jitter, low power 3 x 10 LVCMOS fanout buffer.

Two inputs can accept signal in differential (LVPECL, SSTL, LVDS, HSTL, CML) or single ended (LVPECL or LVCMOS) format and the third input can accept a single ended signal or it can be used to build a crystal oscillator by connecting an external crystal resonator between its XIN and XOUT pins.

The ZL40241 has ten LVCMOS outputs which can be powered from 3.3V, 2.5V, 1.8V or 1.5V supply. Output can be synchronously enabled/disabled via OE pin.

The device operates from 2.5V+/-5% or 3.3V+/-5% supply. Its operation is guaranteed over the industrial temperature range -40°C to +85°C.

Clock Inputs

The following blocks diagram shows how to terminate different signals fed to the ZL40241 inputs.

Figure 3 shows how to terminate a single ended output such as LVCMOS. Ideally, resistors R1 and R2 should be 100Ω each so that the transmission line is terminated with matched impedance (50Ω). However, if the driving strength of the output driver is not sufficient resistor values should be increased

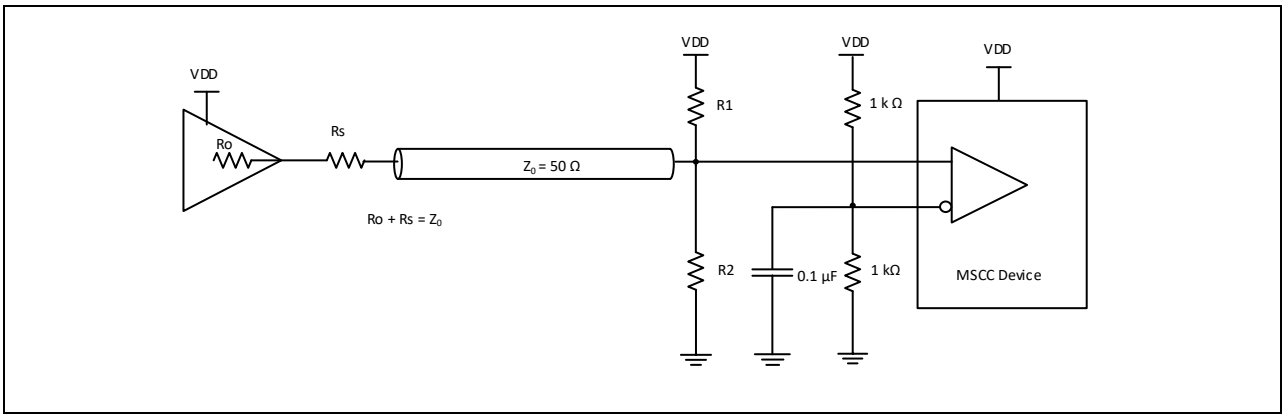


Figure 3. Input driven by a single ended output

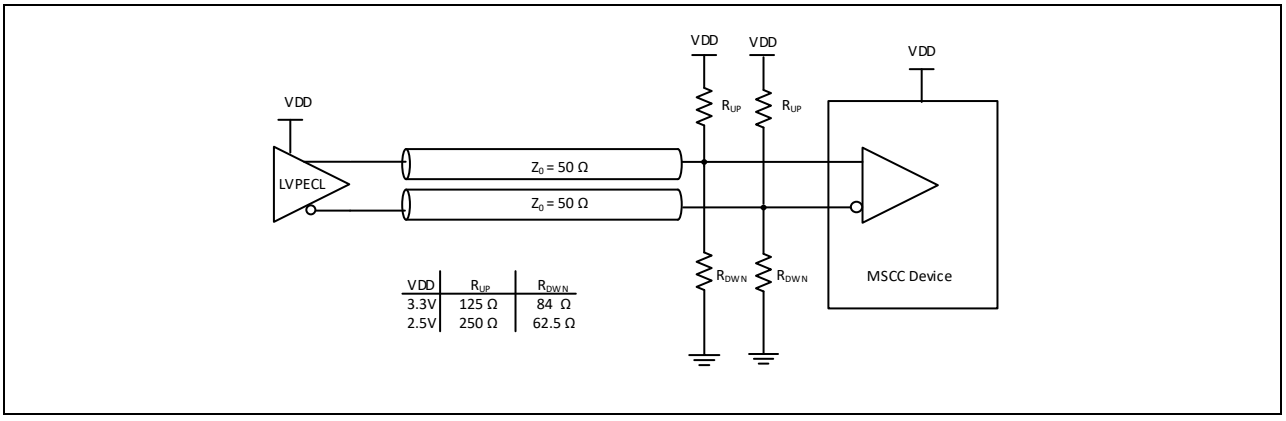


Figure 4. Input driven by DC coupled LVPEVCL output

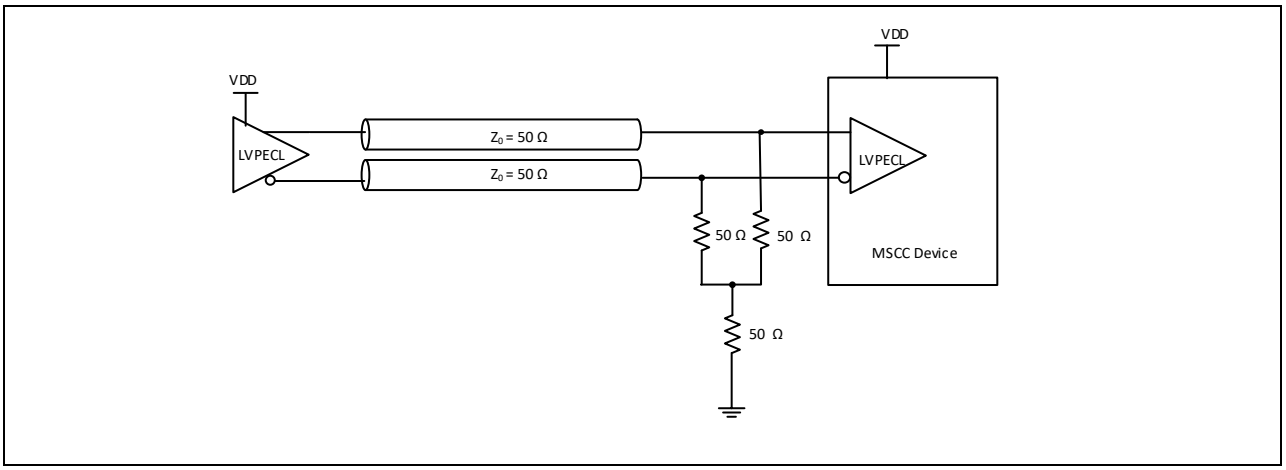


Figure 5. Input driven by DC coupled LVPEVCL output (alternative termination)

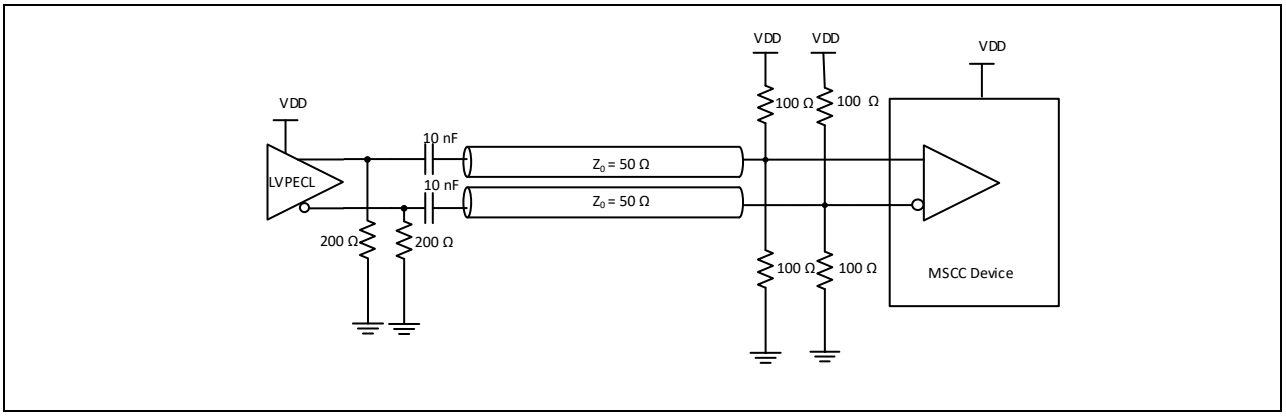


Figure 6. Input driven by AC coupled LVPECL output

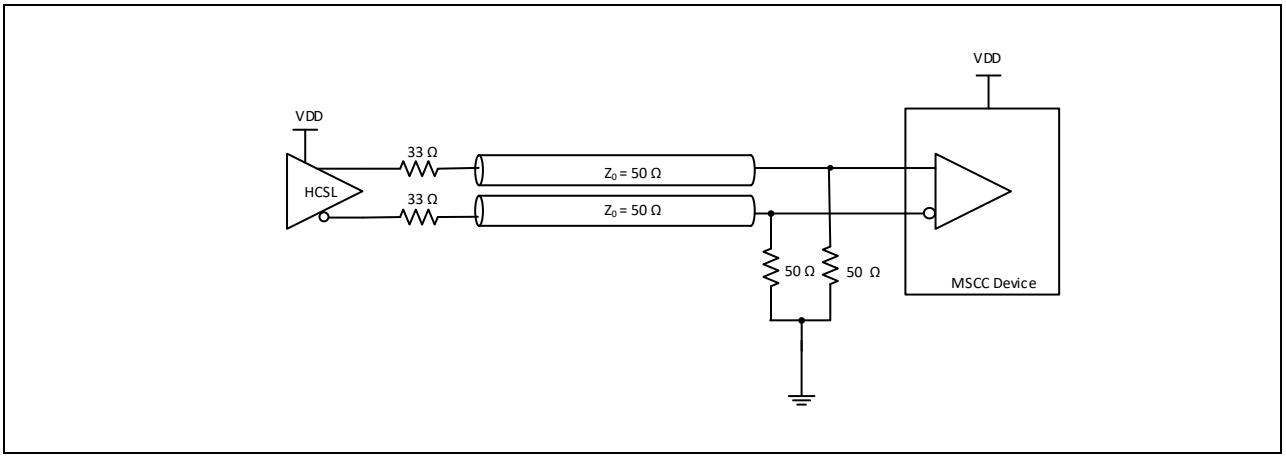


Figure 7. Input driven by HCSL output

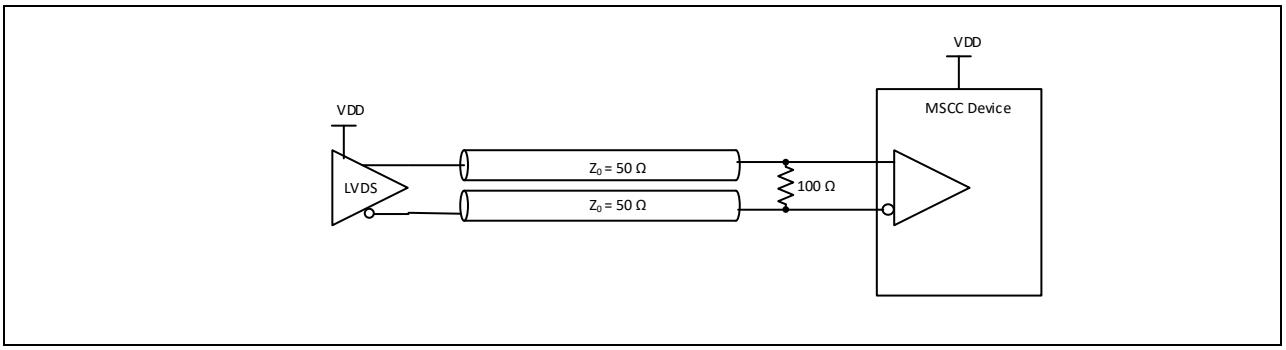


Figure 8. Input driven by LVDS output

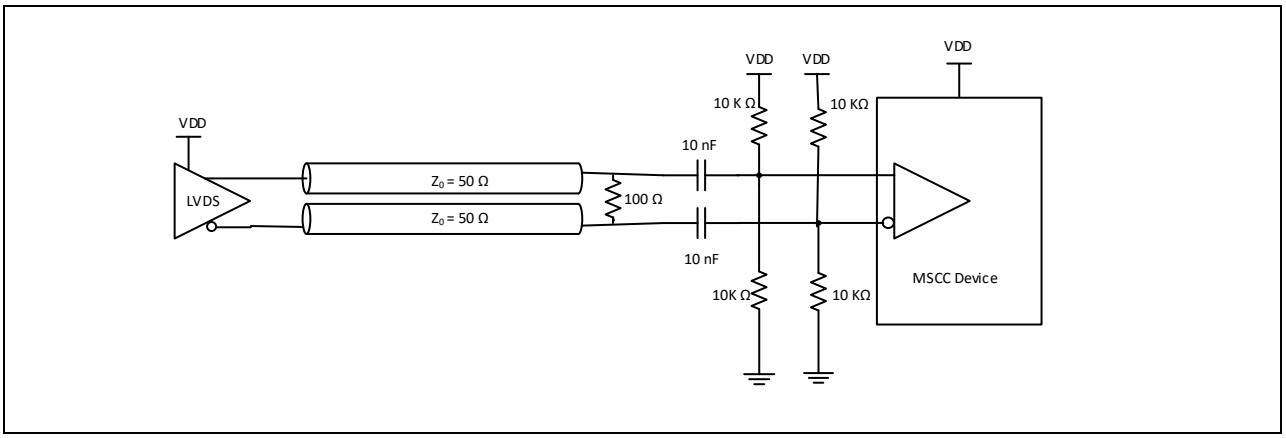


Figure 9. Input driven by AC coupled LVDS

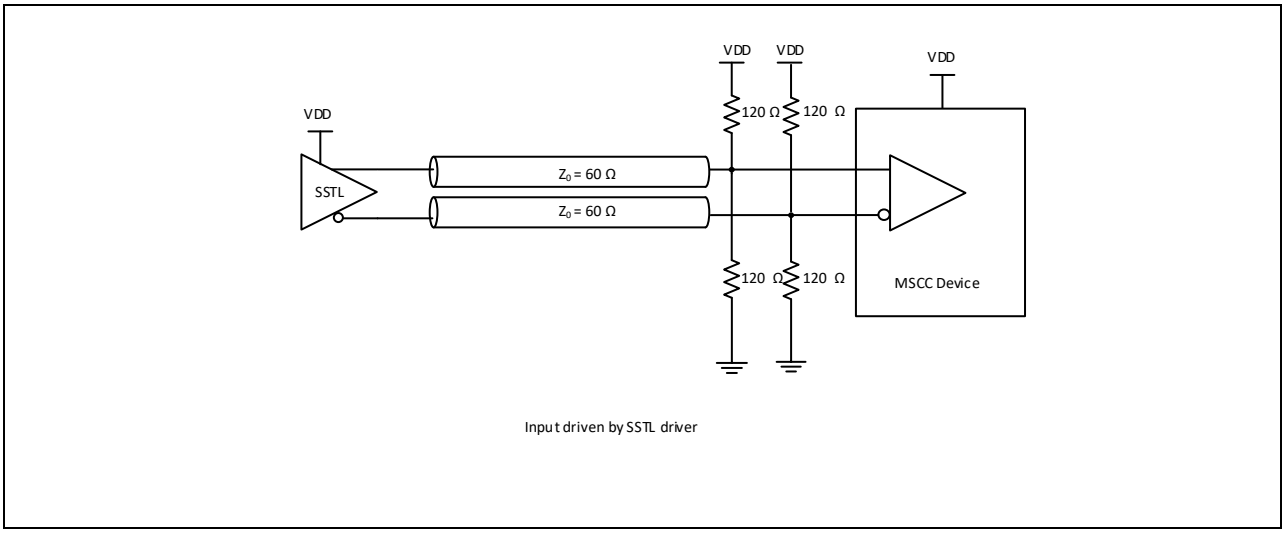


Figure 10. Input driven by an SSTL output

Clock Outputs

LVCMOS outputs require only series termination resistor whose value is depending on LVCMOS output voltage as shown in Figure 11.

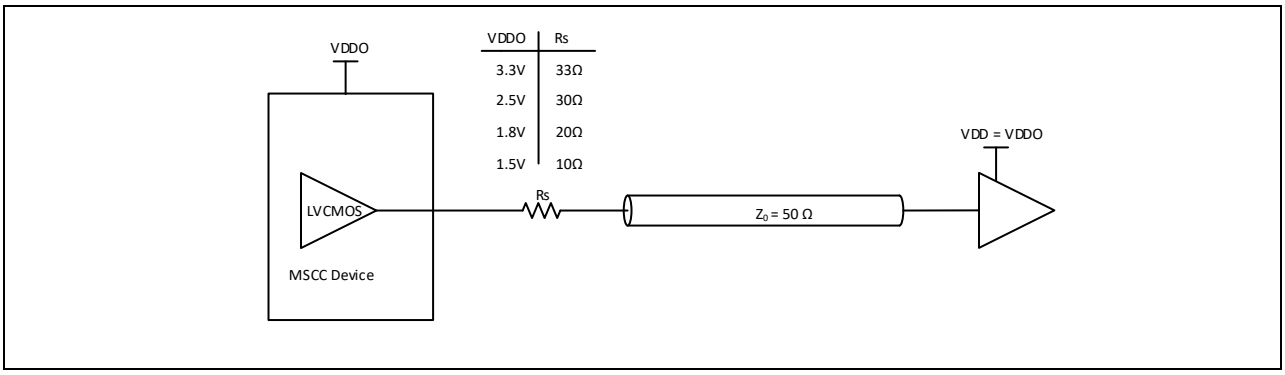


Figure 11. Termination for 3.3V LVPECL outputs

Crystal Oscillator Input

The crystal oscillator circuit can work with crystal resonators from 8MHz to 60MHz. Load capacitors C1 and C2 shall be selected as per crystal vendor recommendation. Shunt resistor is implemented inside the device. If the crystal is not used, connect XIN pin to ground.

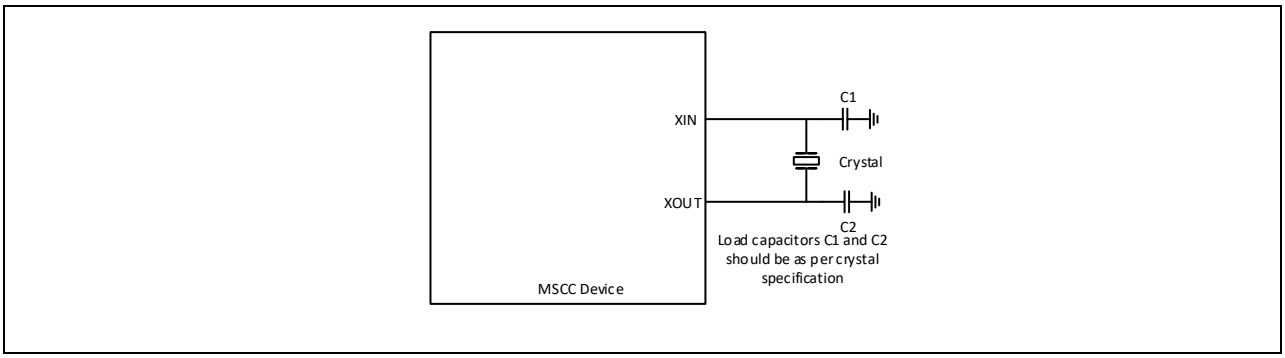


Figure 12. Crystal Oscillator Circuit

The phase noise plot for 25MHz crystal is shown in Figure 13. The phase noise floor of the device is below -170dBc/Hz as can be seen on the figure.

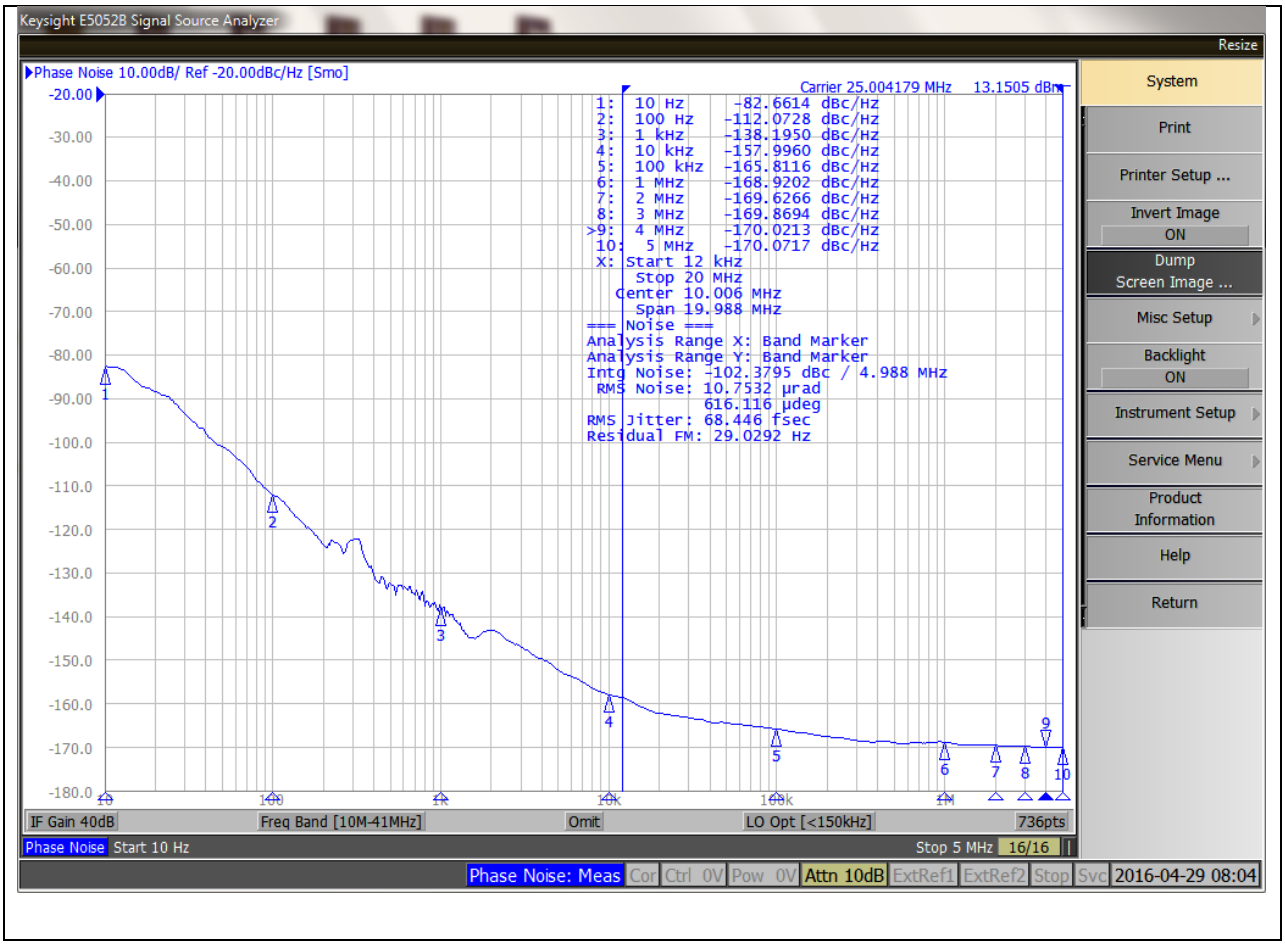


Figure 13. Phase Noise Plot with 25MHz Crystal

Termination of unused inputs and outputs

Unused inputs can be left unconnected or alternatively IN_0/1 can be pulled-down by 1kΩ resistor. Unused outputs should be left unconnected.

Power Consumption

The total device power consumption can be calculated as:

$$P_T = P_S + P_{XTAL} + P_C + P_D$$

Where:

$P_S = V_{DD} \times I_S$ is static power consumed by input buffers. If XTAL is running this power should be set to zero. where the static current (I_S) is specified in Table 4 ·

$P_{XTAL} = V_{DD} \times I_{DD\_XTAL}$ is power consumption of XTAL circuit. The current of the XTAL circuit is provided in Table 4 · If XTAL is not used the power consumption is equal to zero.

$P_C = V_{DDO} \times I_{DDC}$ Common output power shared among all ten outputs. The current (I_{DDC} is specified in Table 4 · ,

$P_D = V_{DDO} \times (I_{DD} \times n \times f / 100MHz + V_{DDO} \times C_{LOAD} \times f \times n)$ Dynamic power where dynamic current (I_{DD}) is specified in Table 4 · , C_{LOAD} is capacitive load driven by an output, f is frequency of the output clock and n is number of active outputs.

The power consumption for different clock frequencies and power supply voltages can be quickly estimated from Figure 14, Figure 15 and Figure 15.

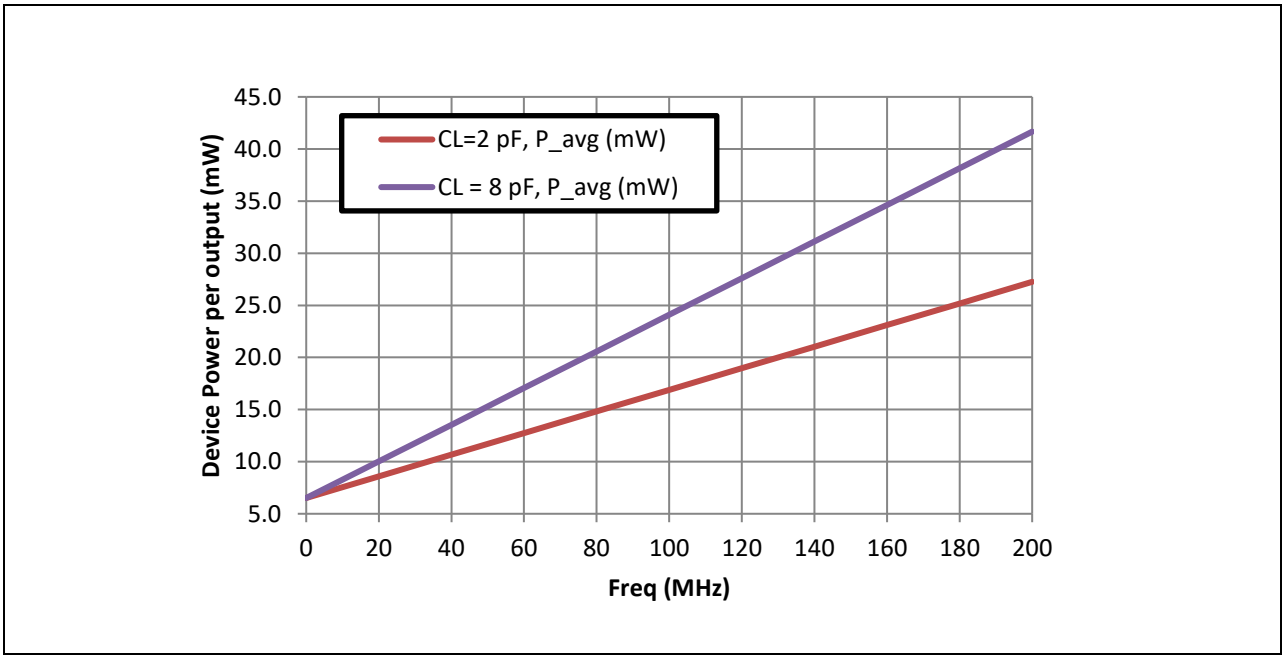


Figure 14. Device power consumption per output for V_{DD} = V_{DDO} = 3.465V

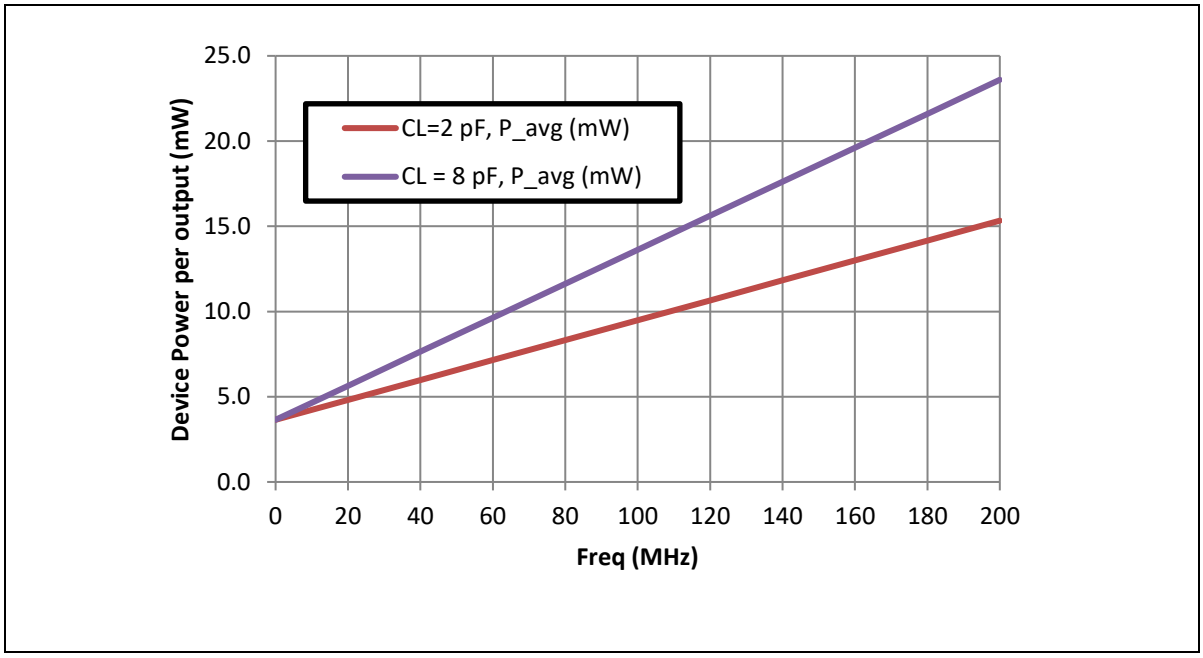


Figure 15. Device power consumption per output for V_{DD} = V_{DDO} = 2.625V

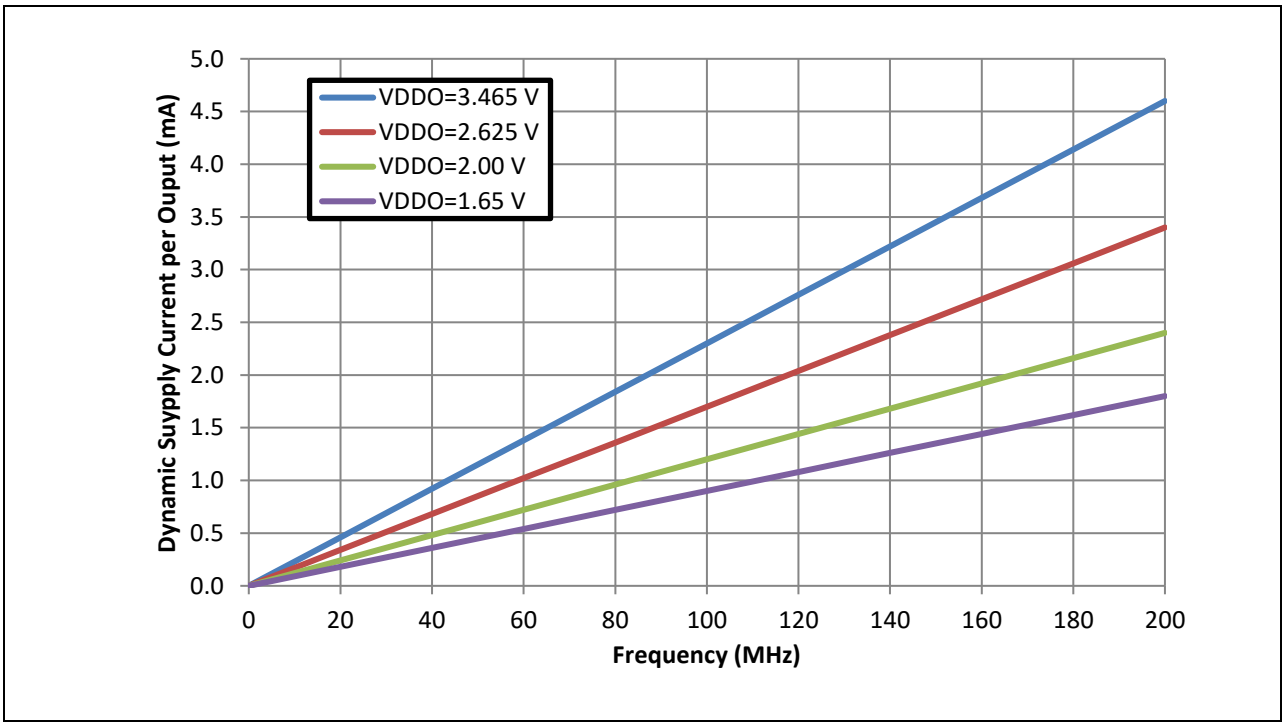


Figure 16. Dynamic supply current per output for different output supply voltages

Power Supply Filtering

Each power pin (VDD and VDDO) should be decoupled with 0.1µF capacitor with minimum equivalent series resistance (ESR) and minimum series inductance (ESL). For example, 0402 X5R Ceramic Capacitors with 6.3V minimum rating could be used. These capacitors should be placed as close as possible to the power pins. To reduce the power noise from adjacent digital components on the board each power supply could be further insulted with low resistance ferrite bead with two capacitors. The ferrite bead will also insulate adjacent component from the noise generated from the device. Following figure shows recommended decoupling for each power pin.

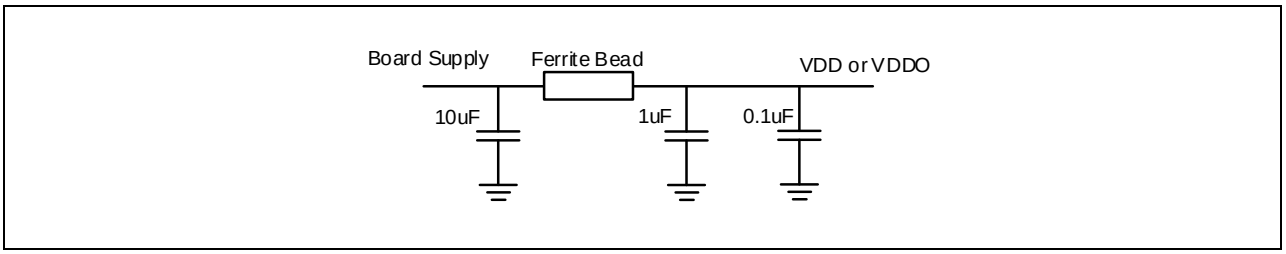


Figure 17. Power Supply Filtering

Device Control

ZL40241 is controlled via Output Enable (OE) and Input Select (SEL0/1) input pins

AC and DC Electrical Characteristics

Absolute Maximum Ratings

Table 2 · Absolute Maximum Ratings*

	Parameter	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage (3.3V)	V_{DD} /V_{DDO}	-0.5		4.6	V	
2	Supply voltage (2.5V)	V_{DD} /V_{DDO}	-0.5		4.6	V	
3	Supply voltage (1.8V)	V_{DDO}	-0.5		2.5	V	
4	Supply voltage (1.5V)	V_{DDO}	-0.5		2.0	V	
5	Storage temperature	T_{ST}	-55		125	°C	

* Exceeding these values may cause permanent damage
* Functional operation under these conditions is not implied
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions

Table 3 · Recommended Operating Conditions*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Supply voltage 3.3V	V_{DD} /V_{DDO}	3.135	3.30	3.465	V	
2	Supply voltage 2.5V	V_{DD} /V_{DDO}	2.375	2.50	2.625	V	
3	Supply voltage 1.8V	V_{DDO}	1.6	1.8V	2	V	
4	Supply voltage 1.5V	V_{DDO}	1.35	1.5	1.65		
5	Operating temperature	T_A	-40	25	85	°C	
6	Input voltage	V_{DD-IN}	- 0.3		V_{DD} + 0.3	V	

* Voltages are with respect to ground (GND) unless otherwise stated
* The device supports two power supply modes (3.3V and 2.5V)

Table 4 · Current consumption

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Static device current	$I_{s\_3.3V}$		15	18	mA	VDD= 3.465V
		$I_{s\_2.5V}$		12	15	mA	VDD = 2.625V
2	Device current with 25MHz XTAL input	$I_{DD\_XTAL\_3.3V}$		24	27	mA	VDD= 3.465V
		$I_{DD\_XTAL\_2.5V}$		18	20	mA	VDD= 2.625V
3	Dynamic current per output (f = 100MHz) (1)(2) Needs to be scaled for different frequencies by f/100MHz, Driving Strength = 1 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$		4.2	4.7	mA	VDDO= 3.465V
		$I_{DD\_2.5V}$		3.0	3.5	mA	VDDO= 2.625V
		$I_{DD\_1.8V}$		2.1	2.4	mA	VDDO= 2V
		$I_{DD\_1.5V}$		1.6	1.8	mA	VDDO= 1.65V
4	Dynamic current per output (f = 100MHz) (1)(2) Needs to be scaled for different frequencies by f/100MHz, Driving Strength = 0 (registers 0x09, 0x0A)	$I_{DD\_3.3V}$		2.3	3.0	mA	VDDO= 3.465V
		$I_{DD\_2.5V}$		1.7	1.8	mA	VDDO= 2.625V
		$I_{DD\_1.8V}$		1.2	1.3	mA	VDDO= 2V
		$I_{DD\_1.5V}$		0.9	1.0	mA	VDDO= 1.65V
5	Common output current(3)	$I_{DDC\_3.3V}$		3.8	8.0	mA	VDDO= 3.465V
		$I_{DDC\_2.5V}$		1.9	3.3	mA	VDDO= 2.625V
		$I_{DDC\_1.8V}$		1.2	1.7	mA	VDDO= 2V
		$I_{DDC\_1.5V}$		1	1.4	mA	VDDO= 1.65V

(1) Needs to be scaled for different frequencies by f/100MHz
(2) To calculate total power consumption use following formula: P = (I_s + I_{DD_XTAL}) * VDD + (I_{DDC} + I_{DD} * n * f/100MHz + VDDO * C_{LOAD} * f * n) * VDDO, where I_{DD_XTAL}: should be set to zero if XTAL is not used or I_s should be set to zero if XTAL is used.
n: number of active outputs
f: frequency of the clock
C_{LOAD}: is capacitive load driven by an output.
(3) This current is consumed by device whenever one or more outputs are enabled. It is independent of the number of active outputs

Table 5 · Input Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage for SEL0/1 and OE	V_{CIH}	1.20			V	
2	CMOS low-level input voltage for SEL0/1 and OE	V_{CIL}			0.45	V	
3	CMOS input leakage current for SEL0/1 and OE(1)	I_{IL}	-40		10	µA	V_I = V_{DD} or 0 V
4	Differential input common mode voltage for IN0_p/n and IN1_p/n	V_{CM}	0.5		VDD – 0.85	V	
5	Differential input voltage difference for IN0_p/n and IN1_p/n	V_{ID}	0.15		1.3	V	
6	Differential input leakage current for IN0_p/n and IN1_p/n(2)	I_{IL}	-200		100	µA	V_I = V_{DD} or 0 V
7	Single ended input high voltage for IN_0_p and IN_1_p	V_{SIH}	2		VDD + 0.3V	V	VDD = 3.3V+/- 5%
		V_{SIH}	1.6		VDD + 0.3V	V	VDD = 2.5V+/- 5%
8	Single ended input high voltage for IN_0_p and IN_1_p	V_{SIL}	-0.3		1.3	V	VDD = 3.3V+/- 5%
		V_{SIL}	-0.3		0.9	V	VDD = 2.5V+/- 5%
9	Input frequency	f_{IN}	0		200	MHz	
10	Input duty cycle	dc	35%		65%		@200MHz; for lower frequencies duty cycle can be scaled proportionally
11	Input slew rate	slew		2		V/ns	
12	Input pull-up/ pull-down resistance (INx_n)	R_{PU}/R_{PD}		60kΩ			
13	Input pull-down resistance (INx_p)	R_{PD}		30kΩ			

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
(1) CMOS input leakage is due to 300kΩ pull-up/pull-down resistors
(2) Differential Input leakage is due to 60kΩ pull-up/pull-down resistors INx_n and due to 30kΩ pull-down resistor for INx_p

Table 6 · Crystal Oscillator Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Mode of oscillation	mode	Fundamental				
2	Frequency	f	8		60	MHz	
3	On chip shunt resistor	R		0.5		MΩ	
4	On chip capacitance	C		12		pF	
5	Frequency in overdrive mode(1)	f_{OV}	0.1		200	MHz	Functional but may not meet AC parameters Minimum depends on AC coupling Capacitor (0.1uF assumed)
6	Frequency in bypass mode(2)	f_{BP}			200	MHz	Functional but may not meet AC parameters

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
(1) Maximum input level is 2V
(2) Maximum output level is VDD

Table 7 · LVCMOS Output Characteristics*

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Output high voltage	V_{OH}	0.8*VDDO			V	VDDO = 3.3V±5%
		V_{OH}	0.8*VDDO			V	VDDO = 2.5V±5%
		V_{OH}	0.7*VDDO			V	VDDO = 1.8V±10%
		V_{OH}	0.7*VDDO			V	VDDO = 1.5V±10%
2	Output low voltage	V_{OL}			0.2*VDDO	V	VDDO = 3.3V±5%
		V_{OL}			0.2*VDDO	V	VDDO = 2.5V±5%
		V_{OL}			0.3*VDDO	V	VDDO = 1.8V±10%
		V_{OL}			0.3*VDDO	V	VDDO = 1.5V±10%
3	Output impedance	R_O		17		Ω	VDDO = 3.3V
		R_O		21		Ω	VDDO = 2.5V
		R_O		30		Ω	VDDO = 1.8V
		R_O		42		Ω	VDDO = 1.5V
4	Output slew rate-- rise or fall (20% to 80%)	t_r, t_f	3.19	5.14	6.33	V/ns	VDDO = 3.3V±5%
		t_r, t_f	1.72	3.74	4.61	V/ns	VDDO = 2.5V±5%
		t_r, t_f	1.64	2.52	3.32	V/ns	VDDO = 1.8V±10%
		t_r, t_f	1.20	1.96	2.54	V/ns	VDDO = 1.5V±10%
5	Output frequency	F_O	0		200	MHz	
6	Output Duty Cycle		50.26%		53.18%		Input. duty-cycle 50%
7	Output enable or disable time				2	Cycle	
8	Output to output skew	t_{OOSK}			27	ps	
9	Device to device output skew	t_{DOOSK}			1.6	ns	
10	Input to output delay	t_{IOD}	1.15	2.09	2.54	ns	VDD = 3.3V
		t_{IOD}	1.57	2.27	2.77	ns	VDD = 2.5V
11	Input multiplexer isolation	iso	75			dB	tested with 125MHz clocks

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Load 50 Ohm to VDDO/2

Table 8 · LVCMOS Output Additive Jitter and Phase Noise*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	System level additive jitter(1)		17		fs-RMS	VDD = 3.3V, VDDO = 3.3V f_{in} = 125MHz, single ended input
			31		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f_{in} = 125MHz, single ended input
			22		fs-RMS	VDD = 3.3V, VDDO = 3.3V f_{in} = 125MHz, differential input
			37		fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f_{in} = 125MHz, differential input
2	Additive jitter(2) (3)		45.18	93.11	fs-RMS	VDD = 3.3V, VDDO = 3.3V f_{in} = 125MHz, single ended input
			80.46	126.92	fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f_{in} = 125MHz, single ended input
			39.95	68.98	fs-RMS	VDD = 3.3V, VDDO = 3.3V f_{in} = 125MHz, differential input
			67.18	117.26	fs-RMS	VDD = 2.5V, VDDO = 1.5V to 2.5V f_{in} = 125MHz, differential input
3	Phase Noise floor (VDD = 3.3V, VDDO = 3.3V)		-145.08	-138.67	dBc/Hz	@10kHz, f_{in} = 125MHz, single ended input
			-152.46	-145.82	dBc/Hz	@100kHz, f_{in} = 125MHz, single ended input
			-160.67	-155.66	dBc/Hz	@1MHz, f_{in} = 125MHz, single ended input
			-162.66	-160.55	dBc/Hz	@10MHz, f_{in} = 125MHz, single ended input
			-162.71	-160.19	dBc/Hz	@20MHz, f_{in} = 125MHz, single ended input
			-145.34	-137.83	dBc/Hz	@10kHz, f_{in} = 125MHz, differential input
			-152.60	-146.93	dBc/Hz	@100kHz, f_{in} = 125MHz, differential input
			-161.06	-156.99	dBc/Hz	@1MHz, f_{in} = 125MHz, differential input
			-163.22	-160.84	dBc/Hz	@10MHz, f_{in} = 125MHz, differential input
			-163.38	-161.42	dBc/Hz	@20MHz, f_{in} = 125MHz, differential input
4	Phase Noise floor (VDD = 2.5V, VDDO = 2.5V)		-139.93	-134.59	dBc/Hz	@10kHz, fin = 125MHz, single ended input
			-147.22	-144.21	dBc/Hz	@100kHz, fin = 125MHz, single ended input
			-157.11	-154.78	dBc/Hz	@1MHz, fin = 125MHz, single ended input
			-160.58	-158.21	dBc/Hz	@10MHz, fin = 125MHz, single ended input
			-160.78	-158.19	dBc/Hz	@20MHz, fin = 125MHz, single ended input
			-141.69	-134.26	dBc/Hz	@10kHz, fin = 125MHz, differential input
			-149.19	-144.73	dBc/Hz	@100kHz, fin = 125MHz, differential input
			-158.66	-156.22	dBc/Hz	@1MHz, fin = 125MHz, differential input
			-161.60	-159.32	dBc/Hz	@10MHz, fin = 125MHz, differential input
			-161.85	-159.36	dBc/Hz	@20MHz, fin = 125MHz, differential input

* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)

(1) System level additive jitter is calculated as $J_{RMS\_SYS\_AJ} = J_{RMS\_OUT} - J_{RMS\_IN}$
(2) Additive jitter is calculated as $J_{RMS\_AJ} = \text{sqrt}(J_{RMS\_OUT}^2 - J_{RMS\_IN}^2)$ where jitter is integrated in 12 kHz to 20 MHz band
Tester measures jitter at 156.25MHz. Since this freq won't appear in the data sheet, it should be removed from the PPGT. Data sheet jitter is guaranteed by lab char. The ATE jitter measurement will be used to screen outliers only, with limits based on ATE distribution

Table 9 · LVCMOS Output Jitter Phase Noise with 25MHz XTAL*

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Jitter RMS in 12kHz to 20MHz band		72.63		fs	VDD = 3.3V, VDDO = 3.3V
			87.59		fs	VDD = 2.5V; VDDO = 2.5V
2	Phase Noise floor		-75.96		dBc/Hz	@10Hz , VDD = 3.3V, VDDO = 3.3V
			-107.50		dBc/Hz	@100Hz, VDD = 3.3V, VDDO = 3.3V
			-132.34		dBc/Hz	@1kHz, VDD = 3.3V, VDDO = 3.3V
			-157.36		dBc/Hz	@10kHz, VDD = 3.3V, VDDO = 3.3V
			-165.82		dBc/Hz	@100kHz, VDD = 3.3V, VDDO = 3.3V
			-168.85		dBc/Hz	@1MHz, VDD = 3.3V, VDDO = 3.3V
			-168.88		dBc/Hz	@5MHz, VDD = 3.3V, VDDO = 3.3V
			-70.52		dBc/Hz	@10Hz, VDD = 2.5V; VDDO = 2.5V
			-102.60		dBc/Hz	@100Hz, VDD = 2.5V; VDDO = 2.5V
			-129.14		dBc/Hz	@1kHz, VDD = 2.5V; VDDO = 2.5V
			-153.93		dBc/Hz	@10kHz, VDD = 2.5V; VDDO = 2.5V
			-164.00		dBc/Hz	@100kHz, VDD = 2.5V; VDDO = 2.5V
			-167.34		dBc/Hz	@1MHz, VDD = 2.5V; VDDO = 2.5V
			-167.41		dBc/Hz	@5MHz, VDD = 2.5V; VDDO = 2.5V

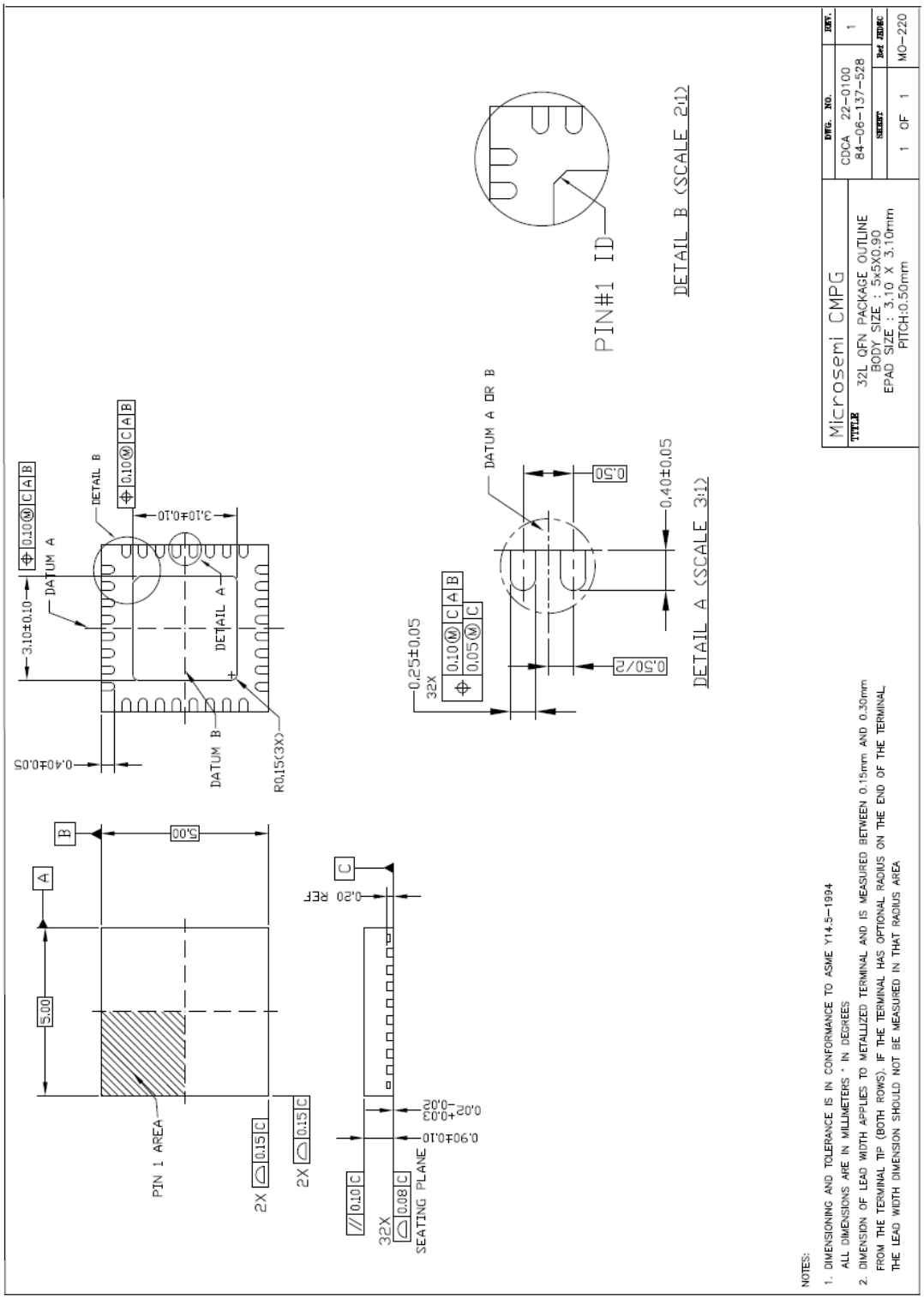
* Values are over Recommended Operating Conditions
* Values are over all two power supply modes (V_{DD} = 3.3V and V_{DD} = 2.5V)
* Xtal frequency is 25 MHz

Table 10 · 5x5mm QFN Package Thermal Properties

Parameter	Symbol	Conditions	Value	Units
Maximum Ambient Temperature	T_A		85	°C
Maximum Junction Temperature	T_{JMAX}		125	°C
Junction to Ambient Thermal Resistance(1) (Note 1)	θ_{JA}	still air	26.8	°C/W
		1m/s airflow	21.8	
		2.5m/s airflow	19.9	
Junction to Board Thermal Resistance	θ_{JB}		10.8	°C/W
Junction to Case Thermal Resistance	θ_{JC}		19.5	°C/W
Junction to Pad Thermal Resistance(2)	θ_{JP}	Still air	6.5	°C/W
Junction to Top-Center Thermal Characterization Parameter	Ψ_{JT}	Still air	0.6	°C/W

(1) Theta-JA (θ_{JA}) is the thermal resistance from junction to ambient when the package is mounted on an 4-layer JEDEC standard test board and dissipating maximum power
(2) Theta-JP (θ_{JP}) is the thermal resistance from junction to the center exposed pad on the bottom of the package)

Package Outline



Revision History

February 2017: Initial Release

July 2018: Release changes:

- Added note in pinout to tie XIN pin when crystal circuit is not used
- Fixed several typographical errors.

October 2018: Release changes:

- Removed Figures 18, and 19 due to inaccuracy