

## Brief Description

The ZSSC3036 is a sensor signal conditioner (SSC) integrated circuit for high-accuracy amplification and analog-to-digital conversion of a differential input signal. Designed for high-resolution altimeter module applications, the ZSSC3036 can perform offset, span, and 1<sup>st</sup> and 2<sup>nd</sup> order temperature compensation of the measured signal. Developed for correction of resistive bridge sensors, it can also provide a corrected temperature output measured with an internal sensor.

The measured and corrected bridge values are provided at the digital output pins, which can be configured as I<sup>2</sup>C™\* (≤ 3.4MHz) or SPI (≤ 20MHz). Digital compensation of signal offset, sensitivity, temperature, and non-linearity is accomplished via an 18-bit internal digital signal processor (DSP) running a correction algorithm. Calibration coefficients are stored on-chip in a highly reliable, non-volatile, multiple-time programmable (MTP) memory. Programming the ZSSC3036 is simple via the serial interface. The IC-internal charge pump provides the MTP programming voltage. The interface is used for the PC-controlled calibration procedure, which programs the set of calibration coefficients in memory. The ZSSC3036 provides accelerated signal processing in order to support high-speed control, safety, and real-time sensing applications. It complements IDT's additional ZSSC30x6 products.

## Features

- Flexible, programmable analog front-end design; up to 16-bit scalable, charge-balancing two-segment analog-to-digital converter (ADC)
- Fully programmable gain amplifier accepting sensors from 14 to 72 (linear factor)
- Internal auto-compensated temperature sensor
- Digital compensation of individual sensor offset; 1<sup>st</sup> and 2<sup>nd</sup> order digital compensation of sensor gain as well as of 1<sup>st</sup> and 2<sup>nd</sup> order temperature gain and offset drift
- Fast sensing: 16-bit conditioned sensor signal measurement rate at more than 200s<sup>-1</sup>
- Typical sensor elements can achieve accuracy of less than ±0.10% FSO\*\* @ -40 to 110°C

## Benefits

- Integrated 18-bit calibration math DSP
- Fully corrected signal at digital output
- Layout customized for die-die bonding with sensor for high-density chip-on-board assembly
- Single-pass calibration minimizes calibration costs
- No external trimming, filter, or buffering components required
- Highly integrated CMOS design
- Excellent for low-voltage and low-power battery applications
- Optimized for operation in calibrated resistive sensor modules

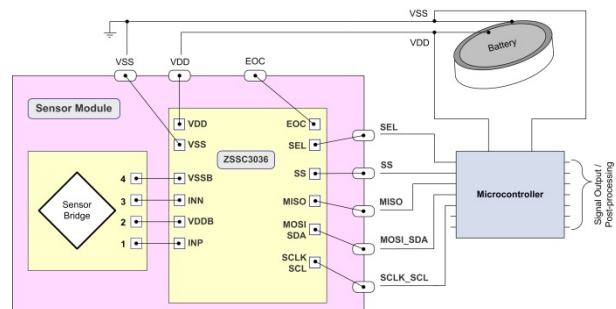
## Physical Characteristics

- Supply voltage range: 1.8 to 3.6V
- Current consumption: 1mA (operating mode)
- Sleep State current: 50nA (typical)
- Temperature resolution: <0.003K/LSB
- Operation temperatures: -40°C to +85°C  
-40°C to +110°C
- Small die size
- Delivery options: die for wafer bonding

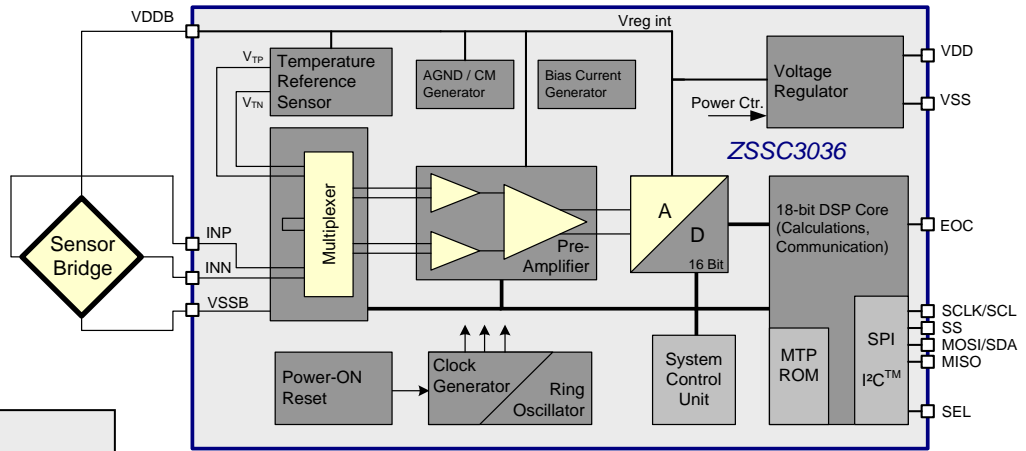
\* I<sup>2</sup>C™ is a trademark of NXP.

\*\* FSO = Full Scale Output.

## ZSSC3036 Application Example



**ZSSC3036  
Block Diagram**



- Applications**
- ❖ Barometric altitude measurement for portable navigation or emergency call systems
  - ❖ Altitude measurement for car navigation
  - ❖ Inside hard disk pressure measurement
  - ❖ Weather forecast
  - ❖ Fan control
  - ❖ Industrial, pneumatic, and liquid pressure

**Ordering Information** (See section 6 in the data sheet for additional options for delivery package and wafer thickness of 725µm.)

Sales Code	Description	Delivery Package
ZSSC3036CC1B	Die—temperature range: -40°C to +85 °C	Wafer (304µm) unsawn, tested
ZSSC3036CI1B	Die—temperature range: -40°C to +85 °C, extended qualification	Wafer (304µm) unsawn, tested
ZSSC3036CC1C	Die—temperature range: -40°C to +85°C	Dice on frame (304µm), tested
ZSSC3036CI1BH	Die—temperature range: -40°C to +110 °C, extended qualification	Wafer (304µm) unsawn, tested
ZSSC3036CI1CH	Die—temperature range: -40°C to +110 °C, extended qualification	Dice on frame (304µm), tested
ZSSC30x6-KIT	Evaluation Kit for ZSSC30x6 Product Family, including boards, cable, software, and 1 sample	

## Table of Contents

1	IC Characteristics .....	6
1.1.	Absolute Maximum Ratings .....	6
1.2.	Operating Conditions .....	6
1.3.	Electrical Parameters .....	7
1.4.	Power Supply Rejection Ratio (RSRR) vs. Frequency.....	9
2	Circuit Description .....	10
2.1.	Brief Description .....	10
2.2.	Signal Flow and Block Diagram.....	10
2.3.	Analog Front End.....	11
2.3.1.	Amplifier .....	11
2.3.2.	Analog-to-Digital Converter.....	13
2.3.3.	Temperature Measurement .....	17
2.3.4.	Bridge Supply.....	17
2.4.	Digital Section.....	17
2.4.1.	Digital Signal Processor (DSP) Core .....	17
2.4.2.	MTP Memory.....	17
2.4.3.	Clock Generator .....	18
2.4.4.	Power Supervision .....	18
2.4.5.	Interface .....	18
3	Functional Description.....	19
3.1.	Power Up .....	19
3.2.	Measurements .....	19
3.3.	Operational Modes .....	19
3.4.	Command Interpretation.....	22
3.4.1.	SPI/I <sup>2</sup> C™ Commands .....	22
3.5.	Communication Interface.....	25
3.5.1.	Common Functionality .....	25
3.5.2.	SPI .....	26
3.5.3.	I <sup>2</sup> C™.....	29
3.6.	Memory.....	30
3.6.1.	Programming Memory .....	30
3.6.2.	Memory Status Commands .....	31
3.6.3.	Memory Contents.....	32
3.7.	Calibration Sequence .....	38
3.7.1.	Calibration Step 1 – Assigning Unique Identification.....	39
3.7.2.	Calibration Step 2 – Data Collection.....	39
3.7.3.	Calibration Step 3 – Coefficient Calculations.....	40
3.8.	The Calibration Math .....	40
3.8.1.	Bridge Signal Compensation .....	40
3.8.2.	Temperature Signal Compensation .....	43

4	Die Pad Assignments .....	44
5	Quality and Reliability .....	45
6	Ordering Sales Codes .....	45
7	Related Documents .....	45
8	Glossary .....	46
9	Document Revision History .....	48

## Table of Figures

Figure 2.1	ZSSC3036 Functional Block Diagram .....	10
Figure 2.2	ADC Offset.....	16
Figure 3.1	Operational Flow Chart: Power Up .....	21
Figure 3.2	Operational Flow Chart: Command Mode and Normal Mode .....	22
Figure 3.3	SPI Configuration CPHA=0 .....	26
Figure 3.4	SPI Configuration CPHA=1 .....	27
Figure 3.5	SPI Command Request .....	27
Figure 3.6	SPI Read Status .....	28
Figure 3.7	SPI Read Data .....	28
Figure 3.8	I <sup>2</sup> C™ Command Request .....	29
Figure 3.9	I <sup>2</sup> C™ Read Status.....	29
Figure 3.10	I <sup>2</sup> C™ Read Data .....	30
Figure 3.11	Memory Program Operation .....	31
Figure 4.1	ZSSC3036 Pad Assignments .....	44

## List of Tables

Table 1.1	Maximum Ratings .....	6
Table 1.2	Operating Conditions .....	6
Table 1.3	Requirements for VDD Power-on Reset.....	7
Table 1.4	Electrical Parameters.....	7
Table 2.1	Amplifier Gain: Stage 1 .....	11
Table 2.2	Amplifier Gain: Stage 2.....	12
Table 2.3	Gain Polarity .....	12
Table 2.4	MSB/LSB Segmentation Settings for Bridge Measurement.....	13
Table 2.5	MSB/LSB Segmentation Settings for Temperature Measurement.....	13
Table 2.6	ADC Conversion Times for a Single A2D Conversion.....	14
Table 2.7	Typical Conversion Times vs. Noise Performance for 16-Bit Results with Full Sensor Signal Conditioning for AZBM, BM, AZTM, and TM .....	15
Table 2.8	ADC Offset Settings.....	16
Table 3.1	SPI/I <sup>2</sup> C™ Commands .....	23
Table 3.2	Get_Raw Commands .....	24
Table 3.3	General Status Byte.....	25

Table 3.4	Status Byte for Read Operations .....	25
Table 3.5	Status Byte for Write Operations .....	25
Table 3.6	Mode Status .....	26
Table 3.7	Memory Status Word .....	31
Table 3.8	MTP Memory Content Assignments .....	32
Table 4.2	Pad Assignments .....	44

# 1 IC Characteristics

## 1.1. Absolute Maximum Ratings

Note: The absolute maximum ratings are stress ratings only. The ZSSC3036 might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

**Table 1.1 Maximum Ratings**

PARAMETER	SYMBOL	Min	TYP	MAX	UNITS
Voltage Reference	V <sub>SS</sub>	0		0	V
Analog Supply Voltage	V <sub>DD</sub>	-0.4		3.63	V
Voltage at all Analog and Digital IO Pins	V <sub>A_IO</sub> , V <sub>D_IO</sub>	-0.5		V <sub>DD</sub> +0.5	V
Input Current into any Pin Except SDA, CLK <sup>1)</sup> and Supply Pins <sup>2)</sup>	I <sub>IN</sub>	-100		100	mA
Electrostatic Discharge Tolerance – Human Body Model (HBM1) <sup>3)</sup>	V <sub>HBM1</sub>	4000		-	V
Storage Temperature	T <sub>STOR</sub>	-50		125	°C
1) Latch-up current limit for CLK/SCLK and MOSI/SDA: ±70mA. 2) Latch-up resistance; reference for pin is 0V. 3) HBM1: C = 100pF charged to V <sub>HBM1</sub> with resistor R = 1.5kΩ in series based on MIL 883, Method 3015.7. ESD protection referring to the Human Body Model is tested with devices in ceramic dual in-line packages (CDIP) during product qualification.					

## 1.2. Operating Conditions

The reference for all voltages is V<sub>SS</sub>.

**Table 1.2 Operating Conditions**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V <sub>DD</sub>	1.8	-	3.6	V
VDD Rise Time	t <sub>VDD</sub>			200	μs
Bridge Current <sup>1)</sup>	I <sub>VDDB</sub>			1.8	mA
				16.5	
Operation Temperature Range—Standard	T <sub>AMB</sub>	-40	-	85	°C
Operation Temperature Range--Extended <sup>2)</sup>		-40	-	110	°C
External capacitance between VDDDB and VSS	CL	0.01		50	nF
1) Power supply rejection is reduced if a current in the range of 16.5mA > I <sub>VDDB</sub> > 1.8mA is drawn out of VDDDB. 2) Extended temperature range is indicated by the addition of H to the part number.					

A dynamic power-on-reset circuit is implemented in order to achieve minimum current consumption in idle mode. The VDD low level and the subsequent rise time and VDD rising slope must meet the requirements in Table 1.1 to guarantee an overall IC reset; lower VDD low levels allow slower rising of the subsequent on-ramp of VDD. Other combinations might also be possible. For example, the reset trigger can be influenced by increasing the power-down time and lowering the VDD rising slope requirement.

**Table 1.3 Requirements for VDD Power-on Reset**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Power Down Time (duration of VDD Low Level)	$t_{\text{SPIKE}}$	3	-	-	$\mu\text{s}$
VDD Low Level	$V_{\text{DDlow}}$	0	-	0.2	V
VDD Rising Slope	$SR_{\text{VDD}}$	10	-	-	V/ms

### 1.3. Electrical Parameters

All parameter values are valid only under the specified operating conditions. All voltages are referenced to Vss.

**Table 1.4 Electrical Parameters**

Note: See important table notes at the end of the table.

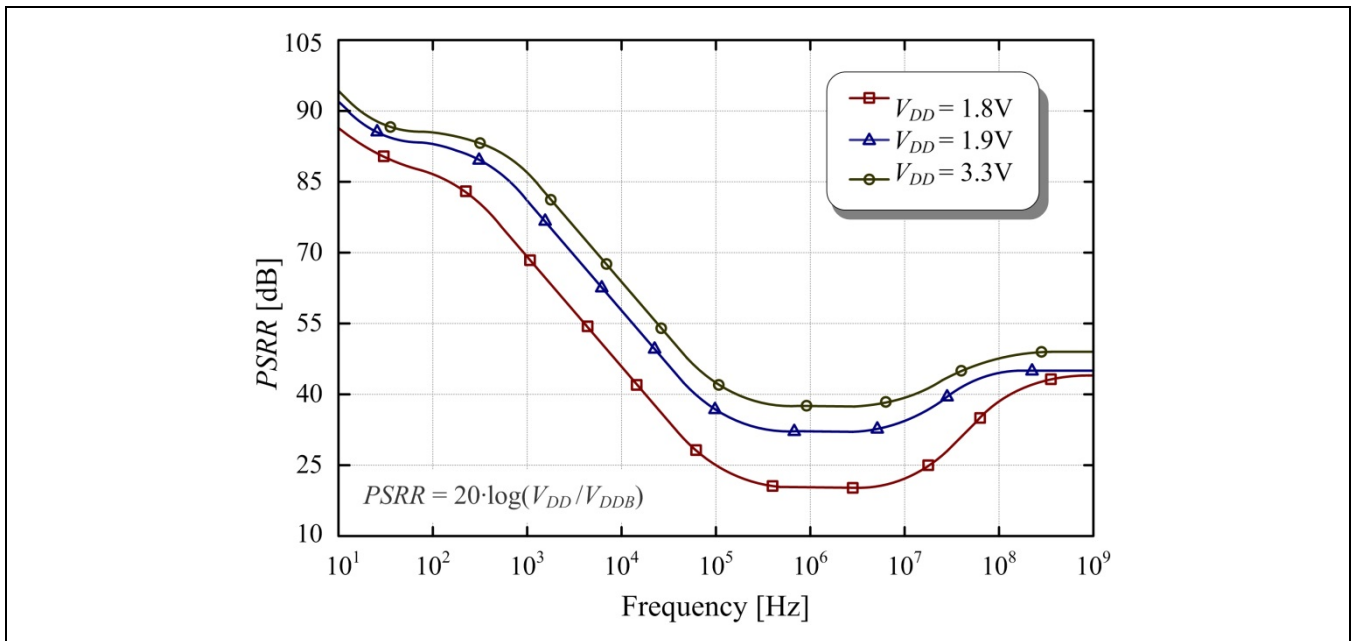
Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
<b>Supply</b>						
Bridge Supply Voltage, ADC Reference Voltage	$V_{\text{DDB}}$	Internally generated	1.60	1.67	1.74	V
Current Consumption	$I_{\text{VDD}}$	Active State, average		900	1500	$\mu\text{A}$
		Sleep State, idle current, $\leq 85^{\circ}\text{C}$		20	250	nA
		Sleep State, idle current, $\leq 110^{\circ}\text{C}$		50	950	nA
Power Supply Rejection $20 \cdot \log_{10}(V_{\text{DD}}/V_{\text{DDB}})$ (see section 1.4)	$PSR_{\text{VDD}}$	$V_{\text{DD}} = 1.8\text{V}$	17			dB
		$V_{\text{DD}} = 2\text{V}$	32			dB
Memory Program Voltage	$V_{\text{DD,prog}}$	Required voltage level at VDD pin	2.9		3.6	V
Mean Program Current	$I_{\text{VDD,prog}}$	Mean current consumption during MTP programming cycle at VDD	6			mA
Peak Program Current	$I_{\text{prog,max}}$	MTP programming at VDD pin, dynamic switch-on current draw			20	mA

Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
<b>Analog-to-Digital Converter (ADC, A2D)</b>						
Resolution	$r_{ADC}$		10		16	Bit
ADC Clock Frequency	$f_{ADC}$	Internal ADC clock	1.3	1.5	1.7	MHz
Reference Voltage n	$V_{refn}$			$V_{DDB} * 0.03$		
Reference Voltage p	$V_{refp}$			$V_{DDB} * 0.97$		
Offset	A2D_Offset	8-step programmable offset	1/16		8/16	
Integral Nonlinearity (INL)	INL <sub>ADC</sub>	Based on ideal slope	-4	-	+4	LSB
Differential Nonlinearity	DNL <sub>ADC</sub>	Tested / verified within design	-1	-	+1	LSB
Conversion Rate, 16-Bit Single	$f_{s,raw}$	Conversions per second for single 16-bit A2D conversion	15	-	1015	Hz
<b>Amplifier</b>						
Gain	$G_{amp}$	32 steps	13.2		72	
Gain Error	$G_{err}$	Referenced to nominal gain	-1.5	-	1.5	%
<b>Sensor Signal Conditioning Performance</b>						
IC Accuracy Error <sup>1)</sup>	Err <sub>A,IC</sub>	Accuracy error for ideally linear (in temperature and measurand) sensor			0.01	%FSO
Conversion Rate, 16-Bit SSC	$f_{s,SSC}$	Conversion per second for fully corrected 16-bit measurement	3.7		245	Hz
<b>Input</b>						
Input Voltage Range	$V_{INP}, V_{INN}$	Input voltage range at INP and INN	0.65		1.05	V
Bridge Resistance	$R_{BR}$	Full power supply disturbance rejection (PSRR) capabilities	1	10	50	k $\Omega$
		Reduced PSRR, but full functionality	100		999	$\Omega$
<b>Power-Up</b>						
Start-up Time	$t_{STA1}$	$V_{DD}$ ramp up to interface communication (see section 3.1)			1.3	ms
	$t_{STA2}$	$V_{DD}$ ramp up to analog operation			3.3	ms
Wake-up Time	$t_{WUP1}$	Sleep to Active State interface communication			0.7	ms
	$t_{WUP2}$	Sleep to Active State analog operation			2.7	ms



Parameter	Symbol	Conditions/Comments	Min	Typ	Max	Unit
<b>Oscillator</b>						
Internal Oscillator Frequency	$f_{CLK}$		2.6	3	3.4	MHz
<b>Internal Temperature Sensor</b>						
Temperature Resolution		For both temperature ranges: -40°C to +85°C -40°C to +110°C		0.003		K/LSB
<b>Interface and Memory</b>						
SPI Clock Frequency	$f_{C,SPI}$	Maximum capacitance at MISO line: 40pF @ $V_{DD}=1.8V$			20	MHz
I <sup>2</sup> C™ Clock Frequency	$f_{C,I2C}$				3.4	MHz
Program Time	$t_{prog}$	MTP programming time per 16-bit register	500		600	μs
Data Retention <sup>2)</sup>	$t_{RET\_MTP}$	1000h @ 125°C	10			a
1) Percentage referred to maximum full-scale output (FSO); e.g. for 16-bit measurements: $Err_{A,IC} [\%FSO] = 100 \cdot \text{MAX}\{  ADC_{meas} - ADC_{ideal}  \} / 2^{16}$ . 2) With maximum ambient temperature of 125°C.						

#### 1.4. Power Supply Rejection Ratio (RSRR) vs. Frequency



## 2 Circuit Description

### 2.1. Brief Description

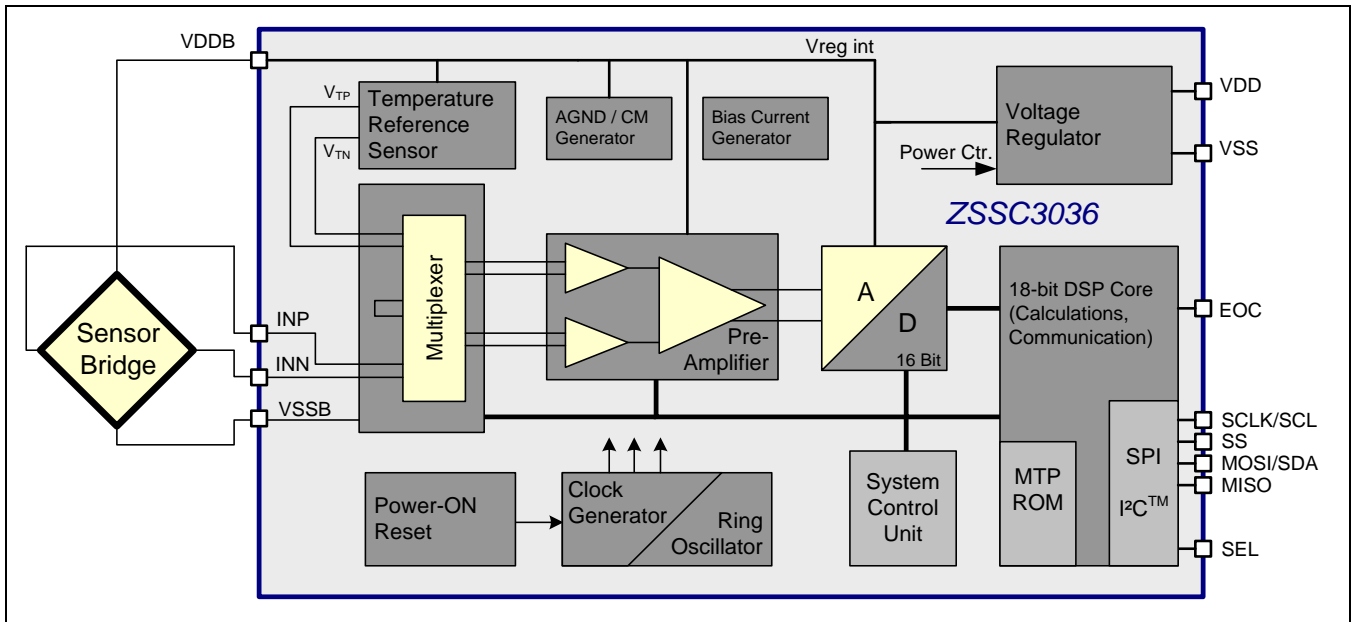
The ZSSC3036 provides a highly accurate amplification of bridge sensor signals. The compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an 18-bit DSP core running a correction algorithm with calibration coefficients stored in an MTP memory. The ZSSC3036 can be configured for a wide range of resistive bridge sensor types. A digital interface (SPI or I<sup>2</sup>C™) enables communication. The ZSSC3036 supports two operational modes: Normal Mode and Command Mode. Normal Mode is the standard operating mode. Typically in Normal Mode, the ZSSC3036 wakes up from a Sleep State (low power), runs a measurement in Active State, and automatically returns to the Sleep State. (See section 3.3 for details on operational modes.)

### 2.2. Signal Flow and Block Diagram

See Figure 2.1 for the ZSSC3036 block diagram. The sensor bridge supply  $V_{DDB}$  and the power supply for analog circuitry are provided by a voltage regulator, which is optimized for power supply disturbance rejection (PSRR). See section 1.4 for a graph of PSRR versus frequency. To improve noise suppression, the digital blocks are powered by a separate voltage regulator. A power supervision circuit monitors all supply voltages and generates appropriate reset signals for initializing the digital blocks.

The state machine controls the analog circuitry to perform the three measurement types: bridge, temperature, and offset measurement. The multiplexer selects the signal input to the amplifier, which can be the external signals from the input pins INP and INN, the internal temperature reference sensor signals, or an input short for measuring offset. A full measurement request will trigger an automatic sequence of all measurement types and all input signals. The Temperature Reference Sensor block is based on a resistive sensing element.

**Figure 2.1 ZSSC3036 Functional Block Diagram**



The amplifier consists of two stages with programmable gain values. The 1/f noise and inherent offset are suppressed by auto-zero and chopper stabilizer techniques. This auto-zero sequence is performed before each bridge sensor and temperature measurement to compensate for the inherent offset of the amplifier.

The ZSSC3036 employs a 2-stage analog-to-digital converter (ADC) based on switched-capacitor technique with inherent low-pass behavior and noise suppression. The programmable resolution from 10 to 16 bits provides flexibility for adapting the conversion characteristics. To improve power supply noise suppression, the ADC uses the bridge supply  $V_{DDB}$  as its reference voltage.

The remaining IC-internal offset and the sensor element offset, i.e., the overall system offset for the amplifier and ADC, can be canceled by an offset and auto-zero measurement, respectively.

The DSP accomplishes the auto-zero, span, and 1<sup>st</sup> and 2<sup>nd</sup> order temperature compensation of the measured bridge signal. The correction coefficients are stored in the MTP memory.

The ZSSC3036 supports SPI and I<sup>2</sup>C™ interface communication for controlling the ZSSC3036, configuration, and measurement result output.

## 2.3. Analog Front End

### 2.3.1. Amplifier

The amplifier has a differential architecture and consists of two stages. The amplification of each stage and the sensor bridge gain polarity are programmable via settings in the Measurement Configuration Register *BM\_config* (address 10<sub>HEX</sub>; see section 3.6.3) in the MTP memory (see section 2.4.2).

The first five bits of *BM\_config* are the programmable gain settings *Gain\_stage1* and *Gain\_stage2*. The options for the programmable gain settings are listed in Table 2.1 and Table 2.2.

**Table 2.1 Amplifier Gain: Stage 1**

<i>Gain_stage1</i>		
<i>BM_config</i> Bit G1	<i>BM_config</i> Bit G0	Stage 1 Gain Setting
0	0	12
0	1	20
1	0	30
1	1	40

**Table 2.2 Amplifier Gain: Stage 2**

<b>Gain_stage2</b>			
<b>BM_config Bit G4</b>	<b>BM_config Bit G3</b>	<b>BM_config Bit G2</b>	<b>Stage 2 Gain Setting</b>
0	0	0	1.1
0	0	1	1.2
0	1	0	1.3
0	1	1	1.4
1	0	0	1.5
1	0	1	1.6
1	1	0	1.7
1	1	1	1.8

If needed, the polarity of the sensor bridge gain can be reversed by setting the *Gain\_polarity* bit, which is bit 5 in the *BM\_config* register (see section 3.6.3). Changing the gain polarity is achieved by inverting the chopper clock. Table 2.3 gives the settings for the *Gain\_polarity* bit. This feature enables applying a sensor to the ZSSC3036 with swapped input signals at INN and INP; e.g., to avoid crossing wires for the final sensor module’s assembly.

**Table 2.3 Gain Polarity**

<b>Gain_polarity (BM_config Bit 5)</b>	<b>Gain</b>	<b>Setting Description</b>
0	+1	No polarity change.
1	-1	Gain polarity is inverted.

The inherent amplifier offset is suppressed by means of auto-zero and chopper techniques.

The optimal gain (and offset) setup for a specific sensor element can be determined by these steps:

- 1) Collect sensor elements’ characteristic, statistical data (over temperature, ambient sensor parameter, and over production tolerances):
  - a. Minimum differential output voltage:  $V_{min}$
  - b. Maximum differential output voltage:  $V_{max}$

*Note: The best possible setup can only be determined if the absolute value of  $V_{max}$  is bigger than the absolute value of  $V_{min}$ . If this is not the case, the gain polarity should be reversed.*

- 2) If  $V_{min}$  and  $V_{max}$  have different signs (normally:  $V_{max}$  is positive and  $V_{min}$  is negative), then the required ADC offset shift can be selected using this ratio:  $Ratio_{Offset} = |V_{min}| / (V_{max} - V_{min})$ .

In this case, the respective offset setup (A2D\_offset) is the nearest integer of multiples of 1/16 in the range of 1/16 to 8/16 (see Table 2.8):  $A2D\_offset = Round\_to\_x16^{th}\{Ratio_{Offset}\}$ .

3) Determine which of the two following cases is valid.

a. If  $\text{Ratio}_{\text{Offset}} - \text{A2D\_offset} \leq 0$  then calculate

$$\text{Theoretical optimum gain: } \text{Gain}_{\text{opt}} = (1 - \text{A2D\_offset}) * V_{\text{ref}} / V_{\text{max}}$$

b. If  $\text{Ratio}_{\text{Offset}} - \text{A2D\_offset} > 0$  then calculate

$$\text{Theoretical optimum gain: } \text{Gain}_{\text{opt}} = \text{A2D\_offset} * V_{\text{ref}} / |V_{\text{min}}|$$

$$\text{with: } V_{\text{ref}} = V_{\text{refp}} - V_{\text{refn}} = 0.94 * V_{\text{DDB,min}} \approx 1.5\text{V}$$

Finally, select the setup gain ( $\text{Gain}_{\text{setup}}$ ) as the nearest gain to  $\text{Gain}_{\text{opt}}$ , where  $\text{Gain}_{\text{setup}} \leq \text{Gain}_{\text{opt}}$ .

### 2.3.2. Analog-to-Digital Converter

A second-order charge-balancing analog-to-digital converter (ADC) is used to convert the amplifier signal. To allow optimizing the trade-off between conversion time and resolution, the conversion is split into a MSB coarse conversion and an LSB fine conversion. The final ADC resolution is determined by MSB + LSB. For the bridge measurement, the MSB-LSB segmentation is programmable via the *Msb* and *Lsb* settings in the *BM\_config* register (10<sub>HEX</sub>; see section 3.6.3) stored in the MTP memory (see section 2.4.2). For the temperature measurement, the MSB-LSB segmentation is programmable via the *Temp\_ADC* settings in the *BM\_config* register.

The conversion time is proportional to  $2^{\text{MSB}} + 2^{\text{LSB}}$ . During the MSB coarse conversion, the ADC input signal is sampled and integrated  $2^{\text{MSB}}$  times, resulting in inherit low-pass behavior and noise suppression. The longer the MSB coarse conversion is, the better the noise suppression is. Possible settings are listed below in Table 2.4 and Table 2.5.

**Table 2.4 MSB/LSB Segmentation Settings for Bridge Measurement**

<i>Msb</i> Setup Bits [7:6] in <i>BM_config</i>	Number of MSB Coarse Conversion Bits	<i>Lsb</i> Setup Bits [9:8] in <i>BM_config</i>	Number of LSB Fine Conversion Bits
00 <sub>BIN</sub>	10	00 <sub>BIN</sub>	0
01 <sub>BIN</sub>	12	01 <sub>BIN</sub>	2
10 <sub>BIN</sub>	14	10 <sub>BIN</sub>	4
11 <sub>BIN</sub>	16	11 <sub>BIN</sub>	6

**Table 2.5 MSB/LSB Segmentation Settings for Temperature Measurement**

<i>Temp_ADC</i> Setup Bits [14:13] in <i>BM_config</i>	Number of MSB Coarse Conversion Bits	Number of LSB Fine Conversion Bits
00 <sub>BIN</sub>	Setup according to IDT configuration in reserved memory (recommended setup for best performance and speed trade-off)	
01 <sub>BIN</sub>	16	0
10 <sub>BIN</sub>	10	6
11 <sub>BIN</sub>	12	4

Useful MSB/LSB setups are with  $LSB = 0$  (MSB-only conversions) or combinations that result in  $MSB + LSB \leq 16$ . Resolutions beyond 16-bit mainly digitize the collected front-end noise and typically do not improve the system performance.

The ADC conversion times for different MSB/LSB settings are listed in Table 2.6.

**Table 2.6 ADC Conversion Times for a Single A2D Conversion**

MSB [Bits]	LSB [Bits]	Bridge or Temperature Measurement Conversion Time in $\mu s$ (typical)
10	0	785
12	0	3200
14	0	12660
<b>16</b>	<b>0</b>	<b>49470</b>
10	2	830
12	2	3240
<b>14</b>	<b>2</b>	<b>12710</b>
10	4	870
<b>12</b>	<b>4</b>	<b>3280</b>
<b>10</b>	<b>6</b>	<b>940</b>

Table 2.7 shows the trade-off between noise performance and typical conversion time for 16-bit results for a signal that has been fully conditioned using 4 single measurements: the auto-zero bridge measurement (AZBM), the bridge measurement (BM), auto-zero temperature measurement (AZTM), and temperature measurement (TM).

**Table 2.7 Typical Conversion Times vs. Noise Performance for 16-Bit Results with Full Sensor Signal Conditioning for AZBM, BM, AZTM, and TM**

Note: The pink shading indicates IDT's recommended ADC segmentation for temperature sensor measurement.

ADC Segmentation: Temperature Sensor [MSB/LSB]	ADC Segmentation: Bridge Sensor [MSB/LSB]	Typical Measurement Duration, MEASURE, (AC <sub>HEX</sub> ) [ms]	Typical 3-Sigma Noise for SSC-Corrected Output <sup>1)</sup> [counts]
10 / 6	10 / 6	4.7	11.0
10 / 6	12 / 4	10.5	7.2
10 / 6	14 / 2	34.3	5.7
10 / 6	16 / 0	129.5	5.6
12 / 4	10 / 6	10.5	10.3
12 / 4	12 / 4	15.9	6.9
12 / 4	14 / 2	39.2	5.5
12 / 4	16 / 0	136.5	5.2
16 / 0	10 / 6	129.5	9.7
16 / 0	12 / 4	136.5	6.5
16 / 0	14 / 2	160.7	5.3
16 / 0	16 / 0	258.9	4.8

1) Reference noise values obtained with this setup: 13.7kΩ sensor bridge, 25°C, Gain=64, ADC shift=-1/16 through 15/16 (see below), VDD=1.8V.

The ADC offset is programmable in 8 steps so that the ADC input voltage range can be adapted to the voltage range at the input pins INP and INN. Possible ADC input voltages are shown in Figure 2.2, where  $V_{AGND} \approx V_{DDB}/2$ . The ADC offset is controlled by the *A2D\_Offset* setting bits [12:10] in the Measurement Configuration Register *BM\_config* (10<sub>HEX</sub>; see section 3.6.3) in the MTP memory (see section 2.4.2). The ADC offset settings are listed in Table 2.8. See section 1.4 for typical values for  $V_{refn}$  and  $V_{refp}$ .

Figure 2.2 ADC Offset

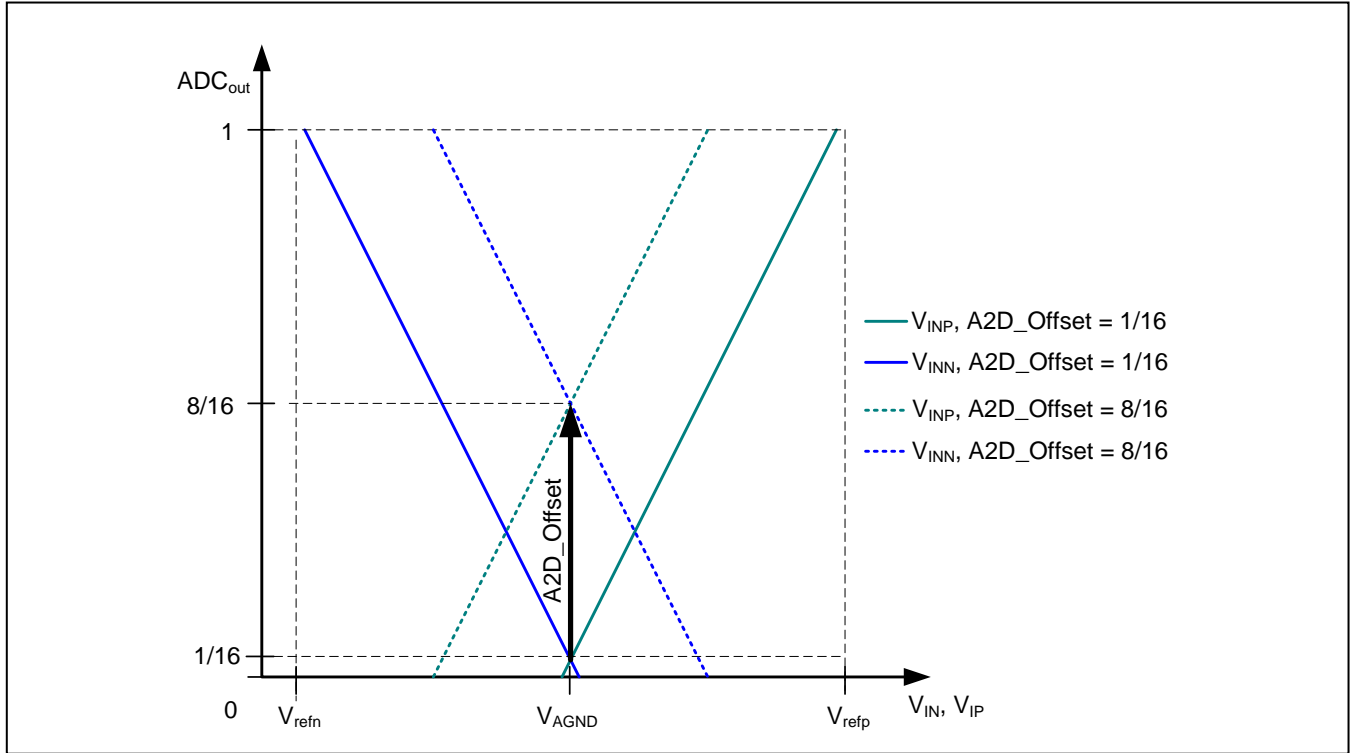


Table 2.8 ADC Offset Settings

Z2	Z1	Z0	ADC Differential Input Range/ $V_{ref}$ Where $V_{ref} = V_{refp} - V_{refn}$	A2D_Offset
0	0	0	-1/16 to 15/16	1/16
0	0	1	-2/16 to 14/16	2/16
0	1	0	-3/16 to 13/16	3/16
0	1	1	-4/16 to 12/16	4/16
1	0	0	-5/16 to 11/16	5/16
1	0	1	-6/16 to 10/16	6/16
1	1	0	-7/16 to 9/16	7/16
1	1	1	-8/16 to 8/16	8/16



### 2.3.3. Temperature Measurement

The ZSSC3036 provides an internal temperature sensor measurement to allow compensation for temperature effects. See section 1.3 for the temperature sensor resolution. The temperature sensor uses bipolar transistors. Any transistor circuitry mismatch is suppressed by dynamic element matching technique. The temperature output signal is a differential voltage that is adapted by the amplifier for the ADC input.

For temperature measurements, the ADC offset and amplifier gain setting are defined by IDT. The ADC MSB/LSB segmentation is programmable by the user for optimizing noise immunity or conversion time (see section 2.3.2).

### 2.3.4. Bridge Supply

The ZSSC3036 provides dedicated bridge supply pins V<sub>DDB</sub> and V<sub>SSB</sub>. The ADC reference voltages for the sensor bridge measurement are derived from these internal voltages so that bridge supply disturbances are suppressed. The current drive ability of V<sub>DDB</sub> is limited (see I<sub>V<sub>DDB</sub></sub> in section 1.2).

## 2.4. Digital Section

### 2.4.1. Digital Signal Processor (DSP) Core

The DSP Core block performs the algorithm for correcting the sensor signal. The resulting coefficients are stored in the MTP memory. When the measurement results are available, the "end of conversion" signal is set at the EOC pin. The internal EOC information is valid only if both the measurement and calculation have been completed.

### 2.4.2. MTP Memory

The ZSSC3036's memory is designed with an OTP (one-time programmable) structure. The memory is organized in 4 one-time programmable pages. When data in the currently valid memory page needs to be updated, normally a new page must be selected by increasing the page counter and the whole memory content must be written in its updated version. The user has access to a 24 x 16 bit storage area for values such as calibration coefficients. Dedicated calibration values are stored in an area not accessible to the user. The required programming voltage is generated internally in the ZSSC3036 whereas increased ZSSC3036 power supply requirements must be fulfilled during programming (see Memory Programming Voltage in section 1.3). There is no over-write or erase function for the MTP memory.

The physical memory function is such that each single bit that has not yet been set to 1 (i.e., remains 0) can still be changed to 1, so it is possible to (partially) re-program an MTP register as shown in the following example:

- Assume MTP address 11<sub>HEX</sub> was written with 8421<sub>HEX</sub> which is 1000 0100 0010 0001<sub>BIN</sub>.
- Changing the register contents to A6A7<sub>HEX</sub> (i.e., 1010 0110 1010 0111<sub>binary</sub>) can be achieved by either writing A6A7<sub>HEX</sub> (any already written bit will be ignored automatically) or just writing the difference compared to 8421<sub>HEX</sub>, which is 2286<sub>HEX</sub>.

The content of a re-written register can generally be determined by

$$\text{content}_{\text{Register}} = \text{content}_{\text{old}} (\text{BITWISE\_OR}) \text{content}_{\text{new}}.$$

If  $\text{content}_{\text{Register}}$  equals  $\text{content}_{\text{new}}$ , a re-write is possible; e.g., this is not the case for  $\text{content}_{\text{old}} = \text{FFFF}_{\text{HEX}}$  and  $\text{content}_{\text{new}} \neq \text{FFFF}_{\text{HEX}}$ . Depending on the former and the newly intended MTP addresses and register contents a re-programming could be possible.

#### **2.4.3. Clock Generator**

The clock generator, implemented as a ring oscillator, provides a 3MHz clock signal. The frequency is trimmed during production test.

#### **2.4.4. Power Supervision**

The power supervision block as a part of the voltage regulator combined with the digital section monitors all power supplies to ensure a defined reset of all digital blocks during power-up or power supply interruptions.

#### **2.4.5. Interface**

The ZSSC3036 can communicate with the user's PC via an SPI or I<sup>2</sup>C™ interface \*. The interface type is selectable via the voltage level on the SEL pin:

- SEL = 0 -> SPI Mode
- SEL = 1 -> I<sup>2</sup>C™ Mode

If the SEL pin is not connected, I<sup>2</sup>C™ communication will be selected (IC-internal pull-up at SEL pin). The SPI-specific pins (SS, MISO) do not need to be connected for I<sup>2</sup>C™ operation.

To also provide interface accessibility in Sleep State (all features inactive except for the digital interface logic), the interface circuitry is directly supplied by VDD.

---

\* Functional I<sup>2</sup>C™ interface properties correspond to the NXP I<sup>2</sup>C™ bus specification Rev. 0.3 (June 2009).

## 3 Functional Description

### 3.1. Power Up

Specifications for this section are given in sections 1.2 and 1.3. On power-up, the ZSSC3036 communication interface is able to receive the first command after a time  $t_{STA1}$  from when the VDD supply is within operating specifications. The ZSSC3036 can begin the first measurement after a time of  $t_{STA2}$  from when the VDD supply is operational.

The wake up time from Sleep State to Active State (see section 3.3) after receiving the activating command is defined as  $t_{WUP1}$  and  $t_{WUP2}$ . In Command Mode, subsequent commands can be sent after  $t_{WUP1}$ . The first measurement starts after  $t_{WUP2}$  if a measurement request was sent.

### 3.2. Measurements

Available measurement procedures are

- AZBM: auto-zero bridge measurement
- BM: bridge measurement
- AZTM: auto-zero temperature measurement
- TM: temperature measurement

**AZBM:** The configuration for bridge measurements is loaded. The Multiplexer block connects the amplifier input to the AGND analog ground reference. An analog-to-digital conversion is performed so that the inherent system offset for the bridge configuration is converted by the ADC to a 16-bit digital word.

**BM:** The configuration for bridge measurements is loaded. The Multiplexer connects the amplifier input to the bridge pins INP and INN. An analog-to-digital conversion is performed. The result is a 16-bit digital word.

**AZTM:** The configuration for temperature measurements is loaded. The Multiplexer connects the amplifier input to AGND. An analog-to-digital conversion is performed so that the inherent system offset for the temperature configuration is converted by the ADC to a 16-bit digital word.

**TM:** The configuration for temperature measurements is loaded. The Multiplexer connects the Amplifier input to the internal temperature sensor. An analog-to-digital conversion is performed. The result is a 16-bit digital word.

The typical application's measurement cycle is a complete SSC measurement (using the command  $AC_{HEX}$ ) with AZBM, BM, AZTM, and TM followed by a signal correction calculation.

### 3.3. Operational Modes

Figure 3.1 illustrates the ZSSC3036 power-up sequence and subsequent operation depending on the selected interface communication mode ( $I^2C^{TM}$  or SPI) as determined by the SEL pin voltage level (see section 2.4.5). With either interface, after the voltage regulators are switched on, the ZSSC3036's low voltage section (LV) is active while the related interface configuration information is read from memory. Then the LV section is switched off, the ZSSC3036 goes into Sleep State, and the interface is ready to receive commands. Since the interface is always powered by  $V_{DD}$ , it is referred to as the high voltage section (HV).

See Table 3.1 for definitions of the commands.

Figure 3.2 shows the ZSSC3036 operation in Normal Mode and Command Mode including when the LV and HV sections are active as indicated by the color legend. The Normal Mode automatically returns to Sleep State after executing the requested measurements. In Command Mode, the ZSSC3036 remains active if a dedicated command (Start\_NOM) was sent, which is helpful during calibration. Command Mode can only be entered if Start\_CM is the first command received after POR.

Figure 3.1 Operational Flow Chart: Power Up

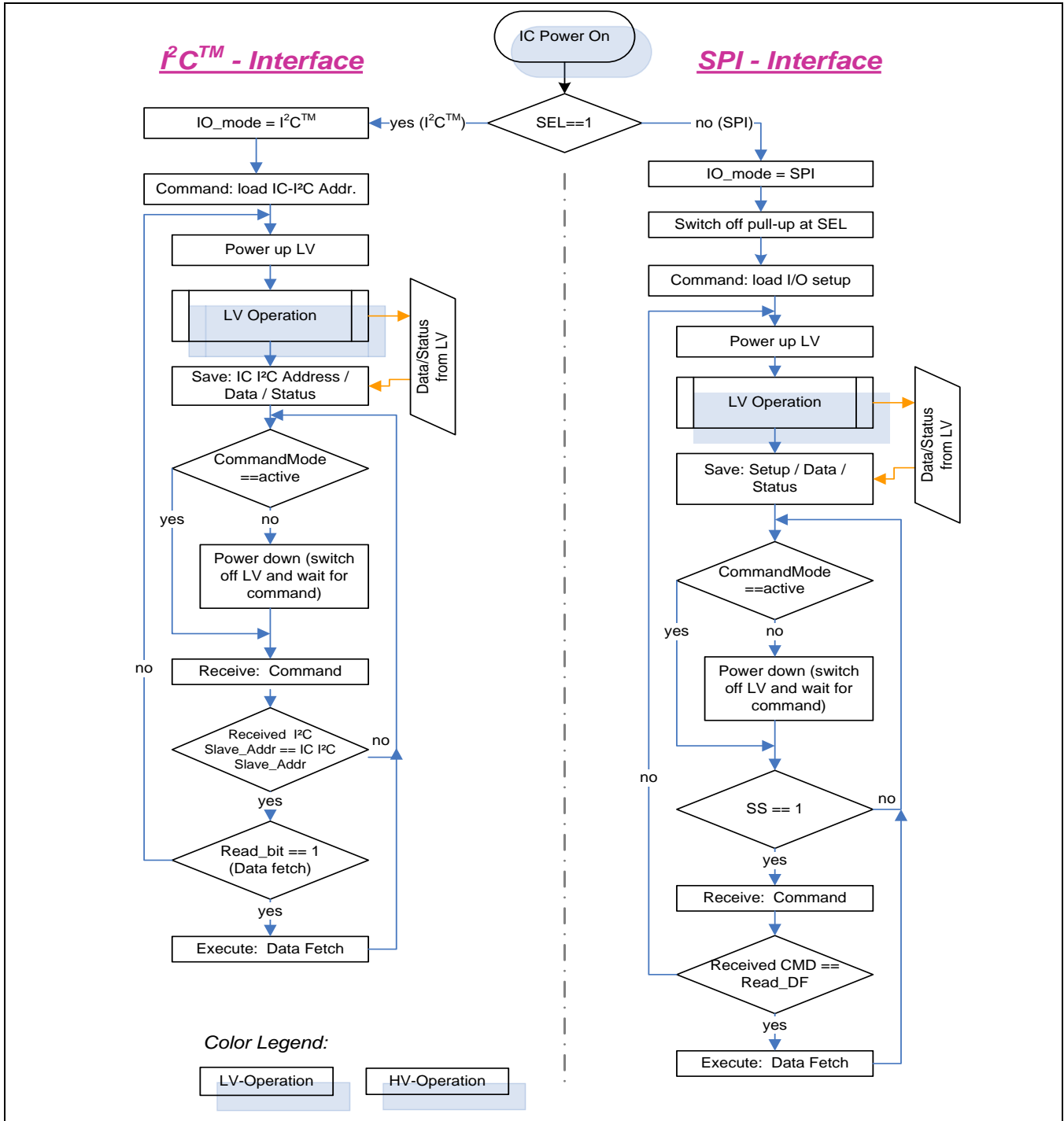
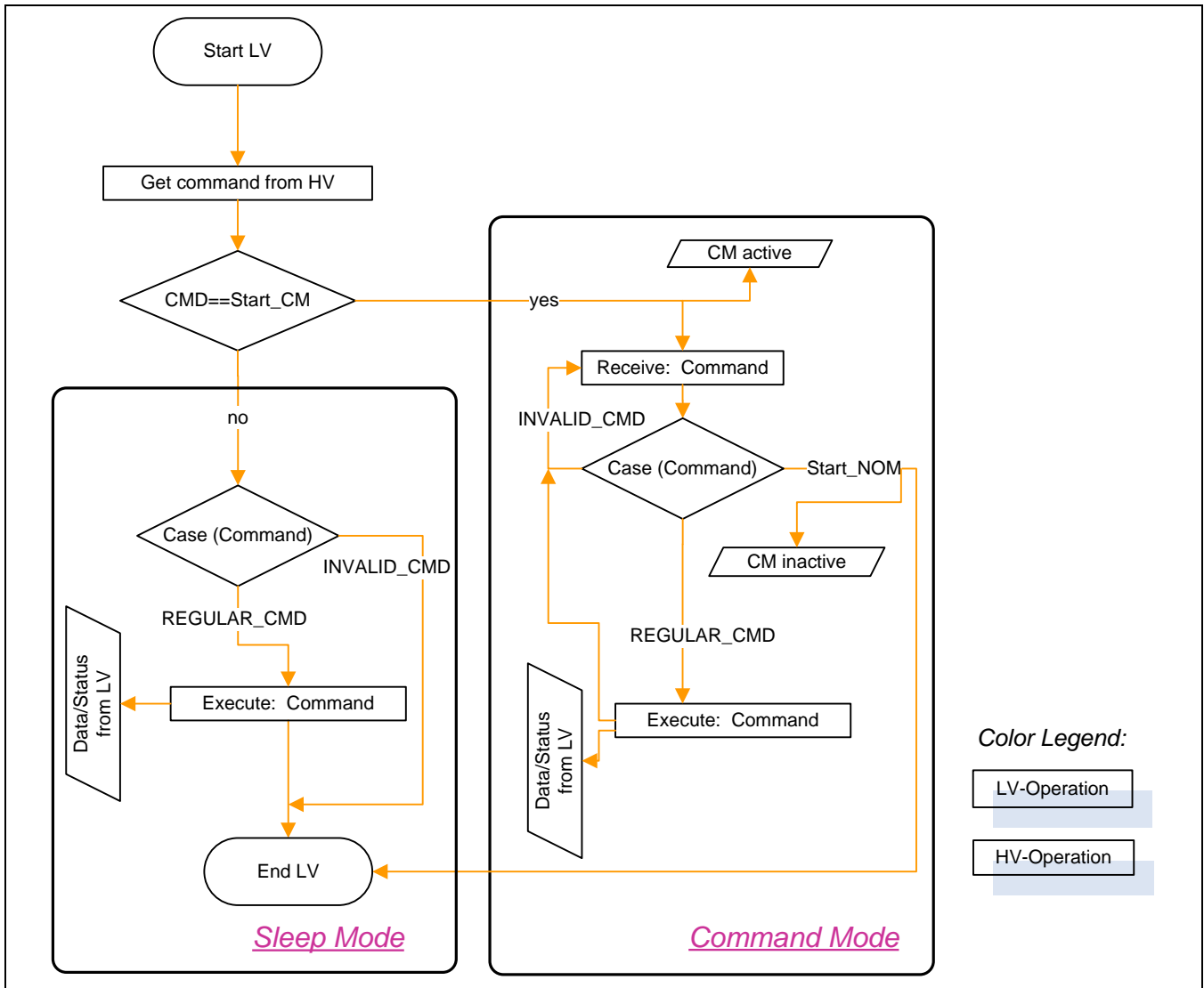


Figure 3.2 Operational Flow Chart: Command Mode and Normal Mode



### 3.4. Command Interpretation

#### 3.4.1. SPI/I<sup>2</sup>C™ Commands

The user-accessible section of memory includes addresses 00<sub>HEX</sub> through 17<sub>HEX</sub> in the OTP memory that is designated by the user memory page pointer. Because each of the four OTP memory pages cannot be rewritten or erased, the memory page pointer must be incremented to the next OTP memory page in order to write to memory again (see Table 3.1 for the command). After all four user-accessible OTP memory pages have been used, further write operations are not possible and the “Memory Full” bit is returned as set in the status byte after write operations (see section 3.5.1).

The SPI/I<sup>2</sup>C™ commands supported by the ZSSC3036 are listed in Table 3.1. The command to read an address in the user memory is the same as its address. The command to read the 16-bit memory status of the data at an address in user memory is the address plus 20<sub>HEX</sub>. The command to write to an address in user memory is the address plus 40<sub>HEX</sub>.

There is an IDT-reserved section of memory that can be read but not over-written by the user.

**Table 3.1 SPI/I<sup>2</sup>C™ Commands**

Note: Every return starts with a status byte followed by the data word as described in section 3.5.1.

Command (Byte)	Return	Description	Normal Mode	Command Mode
00 <sub>HEX</sub> to 17 <sub>HEX</sub>	16-bit user data	Read data in the user memory address (00 <sub>HEX</sub> to 17 <sub>HEX</sub> ) matching the command (might not be using all addresses).	yes	yes
20 <sub>HEX</sub> to 37 <sub>HEX</sub>	16-bit user memory status	Read memory status for address specified by command minus 20 <sub>HEX</sub> (addresses 00 <sub>HEX</sub> to 17 <sub>HEX</sub> respectively; see section 3.6.2 for a description of the memory status).	yes	yes
40 <sub>HEX</sub> to 57 <sub>HEX</sub> followed by data (0000 <sub>HEX</sub> to FFFF <sub>HEX</sub> )	—	Write data to user memory at address specified by command minus 40 <sub>HEX</sub> (addresses 00 <sub>HEX</sub> to 17 <sub>HEX</sub> respectively; might not be using all addresses).	no	yes
70 <sub>HEX</sub> to 7E <sub>HEX</sub>	16-bit IDT-reserved memory data	Read data in IDT-reserved memory at address specified by command minus 70 <sub>HEX</sub> (second set of addresses 00 <sub>HEX</sub> to 0E <sub>HEX</sub> respectively).	no	yes
80 <sub>HEX</sub> to 8E <sub>HEX</sub>	16-bit IDT-reserved memory status	Read memory status bytes for IDT-reserved memory data at address specified by command minus 80 <sub>HEX</sub> (second set of addresses 00 <sub>HEX</sub> to 0E <sub>HEX</sub> respectively; see section 3.6.2 for a description of the memory status bytes).	no	yes
5E <sub>HEX</sub>	—	Increment user memory page pointer.	no	yes
A0 <sub>HEX</sub> to A7 <sub>HEX</sub> followed by XXXX <sub>HEX</sub> (see Table 3.2)	16-bit wide raw data	<b>Get_Raw</b> This command can be used to perform a measurement and write the raw ADC data into the output register. The LSB of the command determines how the AFE configuration register is loaded for the Get_Raw measurement (see Table 3.2).	yes	yes
A8 <sub>HEX</sub>	—	<b>Start_NOM</b> Exit Command Mode and transition to Normal Mode.	no	yes
A9 <sub>HEX</sub>	—	<b>Start_CM</b> Exit Normal Mode and transition to Command Mode.	yes	no

Command (Byte)	Return	Description	Normal Mode	Command Mode
AA <sub>HEX</sub>	—	<b>Write_ChecksumC</b> If not yet written, the checksum for the valid user MTP page is calculated and written to MTP.	no	yes
AC <sub>HEX</sub>	16-bit fully corrected bridge measurement data + 16-bit corrected internal temperature	<b>Measure</b> Triggers full measurement cycle (AZBM, BM, AZTM, and TM, as described in section 3.2) and calculation and storage of data in interface (configurations from MTP).	yes	yes
FX <sub>HEX</sub>	Status followed by last data	<b>NOP</b> Only valid for SPI (see 3.5.1 and 3.5.2).	yes	yes

**Table 3.2 Get\_Raw Commands**

Command	Measurement	AFE Configuration Register
A0 <sub>HEX</sub> followed by 0000 <sub>HEX</sub>	BM – Bridge Measurement	<i>BM_Config</i>
A1 <sub>HEX</sub> followed by ssss <sub>HEX</sub>	BM – Bridge Measurement	sss is the user's configuration setting for the measurement provided via the interface. The format and purpose of configuration bits must be according to the definitions for <i>BM_Config</i> .
A2 <sub>HEX</sub> followed by 0000 <sub>HEX</sub>	BM-AZBM – Auto-Zero Corrected Bridge Measurement <sup>1)</sup>	<i>BM_Config</i>
A3 <sub>HEX</sub> followed by ssss <sub>HEX</sub>	BM-AZBM – Auto-Zero Corrected Bridge Measurement <sup>2)</sup>	sss is the user's configuration setting for the measurement provided via the interface. The format and purpose of configuration bits must be according to the definitions for <i>BM_Config</i> .
A4 <sub>HEX</sub> followed by 0000 <sub>HEX</sub>	TM – Temperature Measurement	IDT-defined register
A5 <sub>HEX</sub> followed by ssss <sub>HEX</sub>	TM – Temperature Measurement	sss is the user's configuration setting for the measurement provided via the interface. The format and purpose of configuration bits must be according to the definitions for <i>BM_Config</i> being valid for temperature measurement in this case (bits [15:13] will be ignored).
A6 <sub>HEX</sub> followed by 0000 <sub>HEX</sub>	TM-AZTM – Auto-Zero Corrected Temperature Measurement <sup>1)</sup>	IDT-defined register
A7 <sub>HEX</sub> followed by ssss <sub>HEX</sub>	TM-AZTM – Auto-Zero Corrected Temperature Measurement <sup>2)</sup>	sss is the user's configuration setting for the measurement provided via the interface. The format and purpose of configuration bits must be according to the definitions for <i>BM_Config</i> being valid for temperature measurement in this case (bits [15:13] will be ignored).

1) Recommended for raw data collection during calibration coefficient determination using pre-programmed (in MTP) measurement setups.  
2) Recommended for raw data collection during calibration coefficient determination using un-programmed (not in MTP), external measurement setups; e.g., for evaluation purposes.



### 3.5. Communication Interface

#### 3.5.1. Common Functionality

Commands are handled by the command interpreter in the LV section. Commands that need additional data are not treated differently than other commands because the HV interface is able to buffer the command and all the data that belongs to the command and the command interpreter is activated as soon as a command byte is received.

Every response starts with a status byte followed by the data word. The data word depends on the previous command. It is possible to read the same data more than once if the read request is repeated (I<sup>2</sup>C™) or a NOP command is sent (SPI). If the next command is not a read request (I<sup>2</sup>C™) or a NOP (SPI), it invalidates any previous data.

The status byte contains the following bits (see Table 3.3, Table 3.4, and Table 3.5 for sequence):

- Power indication (bit 6): 1 if the device is powered (V<sub>DDB</sub> on); 0 if not powered. This is needed for SPI Mode where the master reads all zeros if the device is not powered or in power-on reset (POR).
- Busy indication (bit 5): 1 if the device is busy, which indicates that the data for the last command is not available yet. No new commands are processed if the device is busy.
- Actual ZSSC3036 mode (bits 4:3): 00 = Normal Mode; 01 = Command Mode; 1X = IDT-reserved.
- Memory integrity/error flag (bit 2): 0 if integrity test passed, 1 if test failed. This bit indicates whether the checksum-based integrity check passed or failed. Correctable errors are not reported but can be queried with the memory status commands (see section 3.6.2). The memory error status bit is calculated only during the power-up sequence, so a newly written CRC will only be used for memory verification and status update after a subsequent ZSSC3036 power-on reset (POR).
- Data transfer/correction (bit 1): If the last command was a memory write, this bit is 0 if the last memory write was successful (memory not full yet); otherwise it is 1 (e.g., page increase but already on last MTP page). If the last command was a memory read, this bit is 1 if the data was corrected.

**Table 3.3 General Status Byte**

Bit	7	6	5	4	3	2	1	0
Meaning	0	Powered?	Busy?	Mode		Memory error?	Internal data transfer	Special

**Table 3.4 Status Byte for Read Operations**

Bit	7	6	5	4	3	2	1	0
Meaning	0	Powered?	Busy?	Mode		Memory error?	Data corrected?	ALU saturation?

**Table 3.5 Status Byte for Write Operations**

Bit	7	6	5	4	3	2	1	0
Meaning	0	Powered?	Busy?	Mode		Memory error?	Memory full? ⇔ MTP write reject?	Don't care

**Table 3.6 Mode Status**

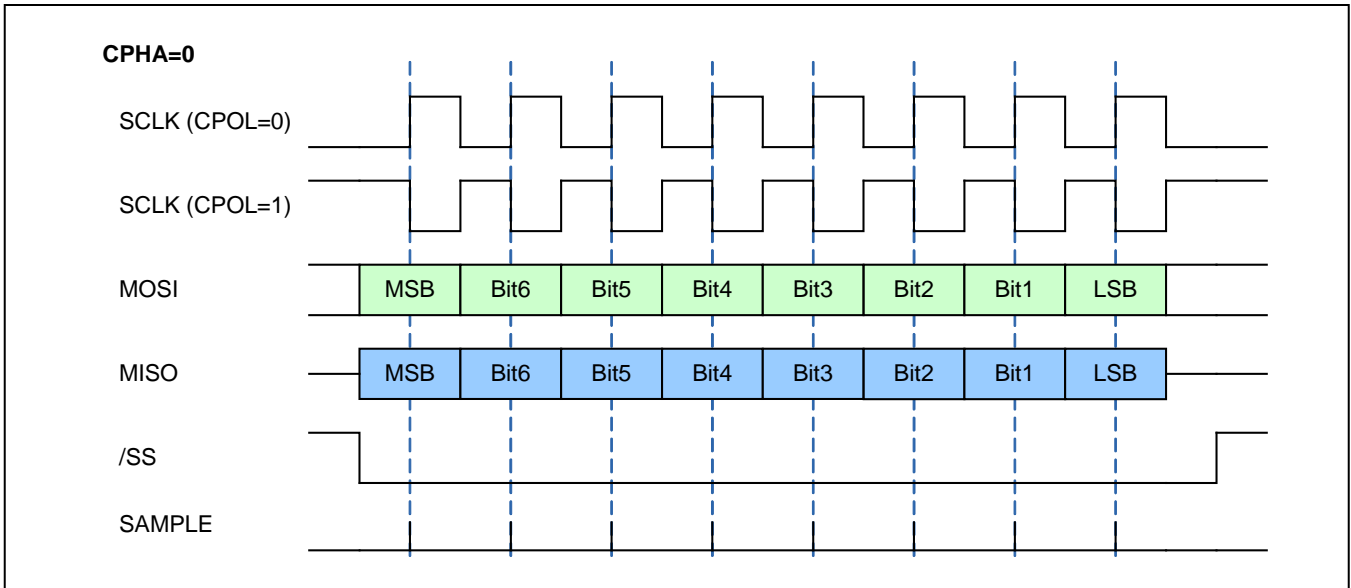
Status[4:3]	Mode
00	Normal Mode
01	Command Mode
10	IDT-Reserved
11	Command Mode and Reserved

Further status information is provided by the EOC pin. The EOC pin is set high when a measurement and calculation have been completed.

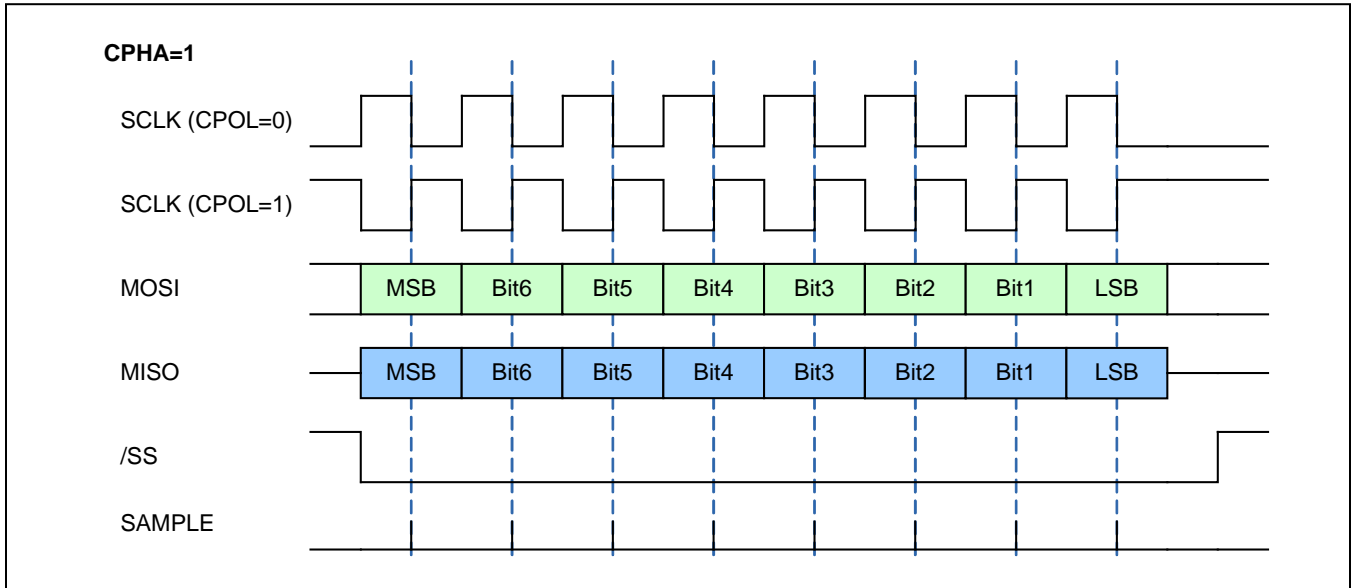
**3.5.2. SPI**

The SPI Mode is available when the SEL pin = 0. The polarity and phase of the SPI clock are programmable via the CKP\_CKE setting in address 02<sub>HEX</sub> as described in Table 3.8. CKP\_CKE is two bits: CPHA (bit 10), which selects which edge of SCLK latches data, and CPOL (bit 11), which indicates whether SCLK is high or low when it is idle. The polarity of the SS signal and pin are programmable via the SS\_polarity setting (bit 9). The different combinations of polarity and phase are illustrated in the figures below.

**Figure 3.3 SPI Configuration CPHA=0**

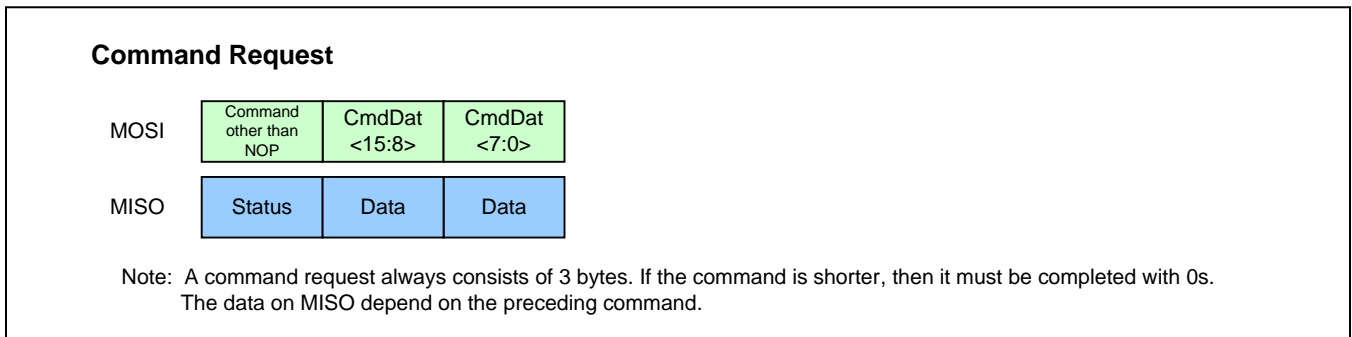


**Figure 3.4 SPI Configuration CPHA=1**



In SPI mode, each command except NOP is started as shown in Figure 3.5. After the execution of a command (busy = 0), the expected data can be read as illustrated in Figure 3.6 or if no data are returned by the command, the next command can be sent. The status can be read at any time with the NOP command (see Figure 3.7).

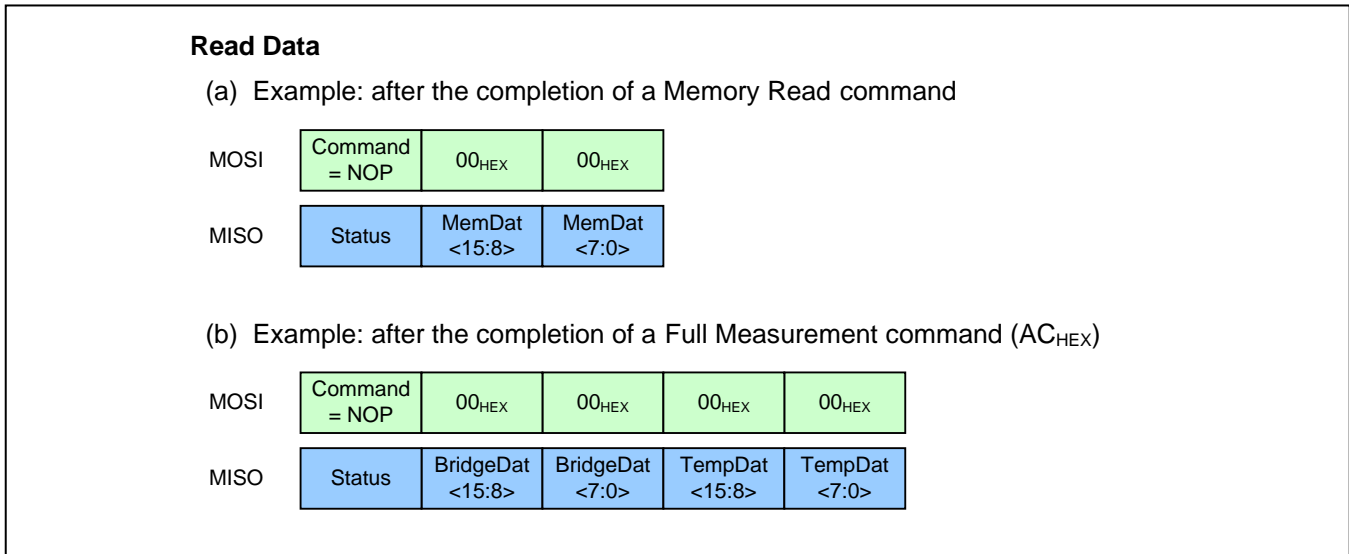
**Figure 3.5 SPI Command Request**



**Figure 3.6 SPI Read Status**



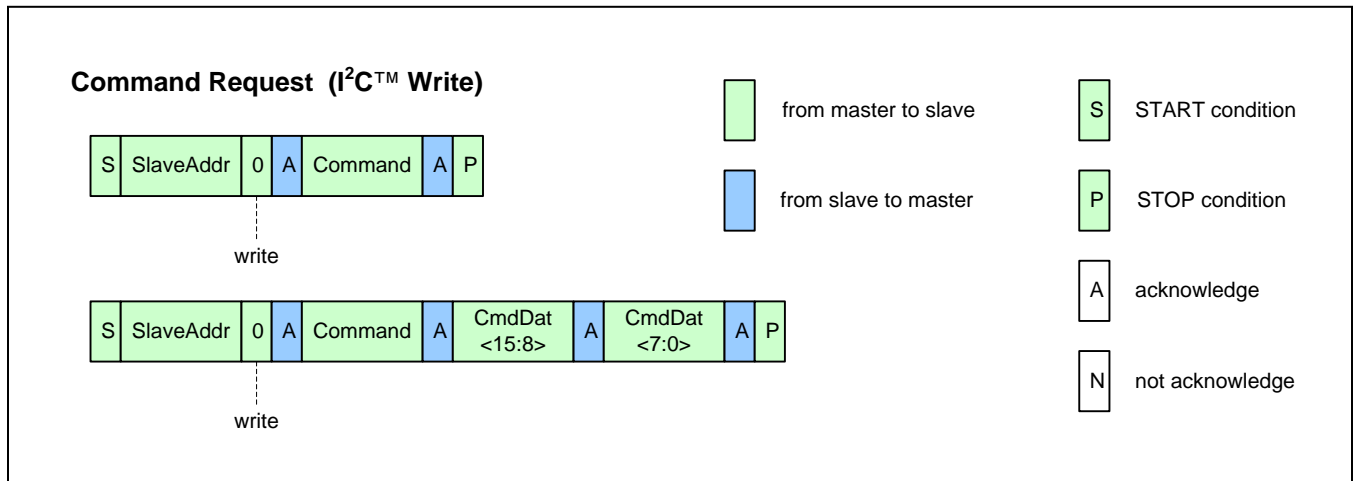
**Figure 3.7 SPI Read Data**



### 3.5.3. I<sup>2</sup>C™

I<sup>2</sup>C Mode is selected by the SEL pin = 1. In I<sup>2</sup>C Mode, each command is started as shown in Figure 3.8. Only the number of bytes that is needed for the command must be sent. An exception is the HS-mode where 3 bytes must always be sent as in SPI Mode. After the execution of a command (busy = 0), the expected data can be read as illustrated in Figure 3.10 or if no data are returned by the command, the next command can be sent. The status can be read at any time as described in Figure 3.9.

**Figure 3.8 I<sup>2</sup>C™ Command Request**



**Figure 3.9 I<sup>2</sup>C™ Read Status**

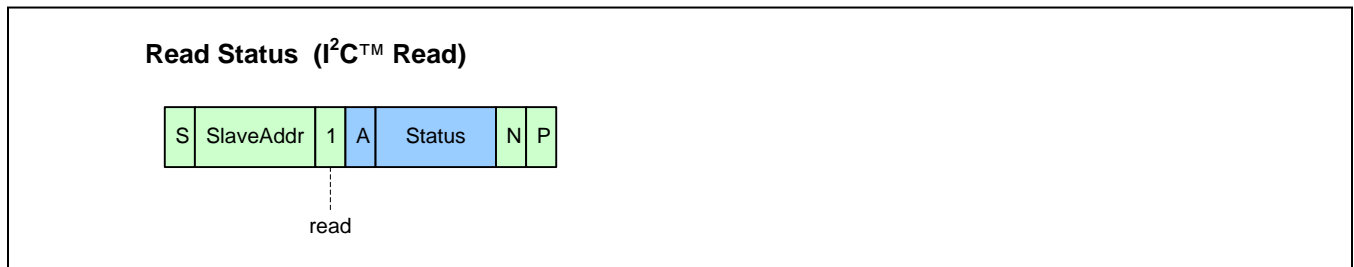
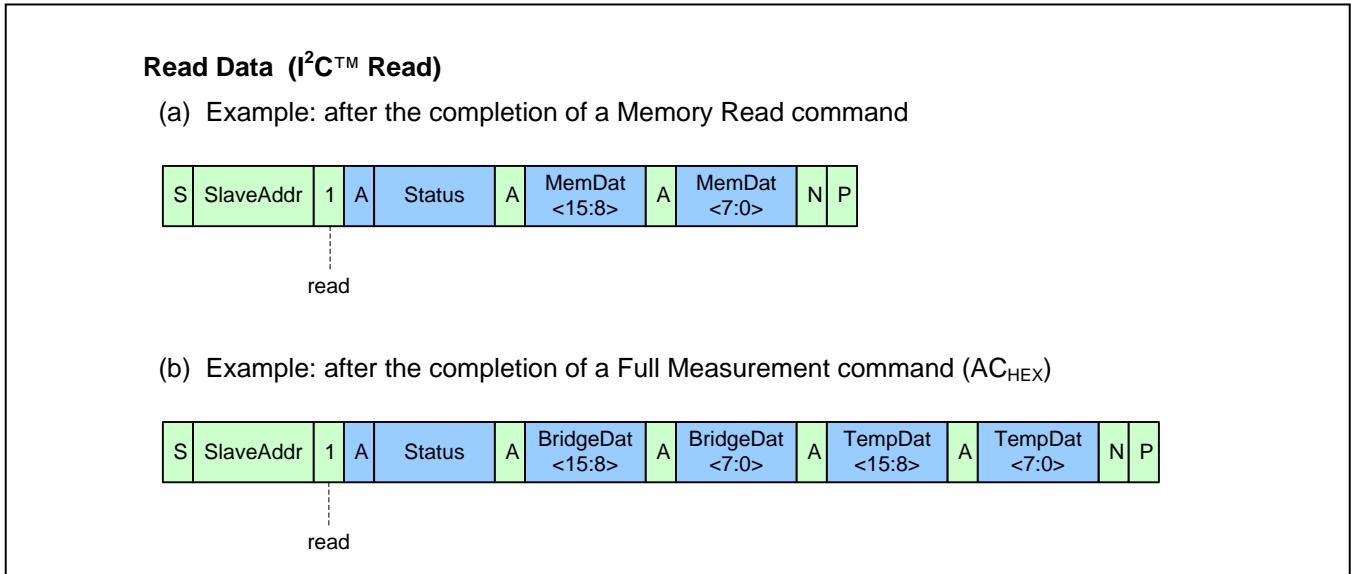


Figure 3.10 I<sup>2</sup>C™ Read Data



All mandatory I<sup>2</sup>C-bus protocol features are implemented. Optional features like clock stretching, 10-bit slave address, etc., are not supported by the ZSSC3036's interface. In I<sup>2</sup>C-High-Speed Mode, a command consists of a fixed length of three bytes.

### 3.6. Memory

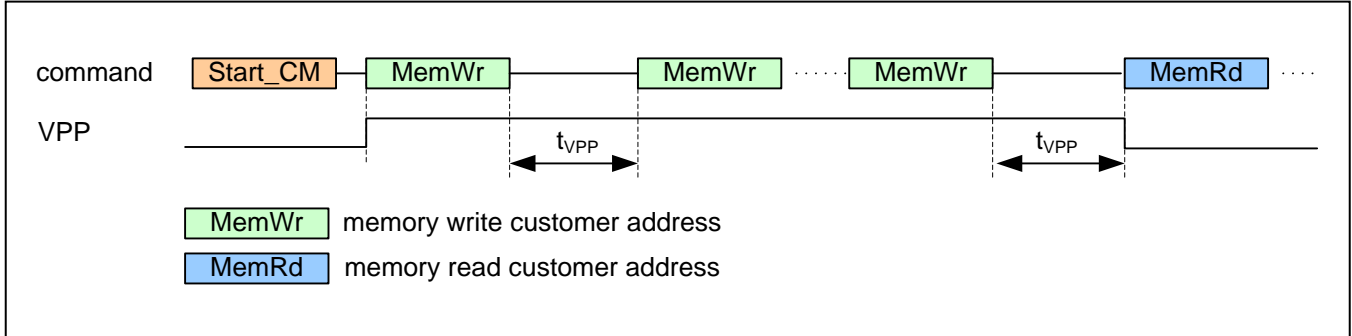
In the ZSSC3036, the memory is organized page-wise and can be programmed multiple (4) times (MTP). Each register can only be programmed once per page. The valid page is determined by the page counter which can be incremented with the command 5E<sub>HEX</sub> – this leads to a “reset” of all registers and a re-programming is necessary. Increasing the customer page counter will disable all old register contents of the former page. It is possible to (re-)program a total of 4 pages. Resetting the page counter is not possible. The page counter starts with 0 and can be incremented to a maximum of 3. If the 4<sup>th</sup> memory page has been used, no further changes in the memory are possible – careful writing and page incrementing is strongly recommended. There are two MTP page types:

- Customer Page: accessible by means of regular write operations (40<sub>HEX</sub> to 57<sub>HEX</sub>). It contains: the customer ID, interface setup data, measurement setup information, calibration coefficients, etc.
- IDT Page: only accessible for write operations by IDT. The IDT page contains specific trim information and is programmed during manufacturing test by IDT.

#### 3.6.1. Programming Memory

Programming memory requires a specific supply voltage level (>2.9V) at the VDD pin (see section 1.3 for specifications). The MTP programming voltage itself is generated by means of an implemented charge pump, generating an internal memory programming voltage (VPP); no additional, external voltage, other than VDD needed. The program timing is shown in Figure 3.11. Supplying the ZSSC3036 with VDD>2.9V during memory programming is required. After the memory is programmed, it must be read again to verify the validity of the memory contents.

**Figure 3.11 Memory Program Operation**



**3.6.2. Memory Status Commands**

The 16-bit memory status answer for the commands: 20<sub>HEX</sub> to 37<sub>HEX</sub> and 80<sub>HEX</sub> to 8E<sub>HEX</sub> contains the following information:

- One bit indicating if the data read was corrected.
- Two bits indicating the current page in use.

**Table 3.7 Memory Status Word**

Bit	Description
15 (MSB)	Data was corrected (0: no, 1: yes)
14	Current page
13	
12:0	Undefined – do not use

### 3.6.3. Memory Contents

**Table 3.8 MTP Memory Content Assignments**

MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
00 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	Cust_ID0	Customer ID byte 0 (combines with memory word 01 <sub>HEX</sub> to form customer ID)
01 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	Cust_ID1	Customer ID byte 1 (combines with memory word 00 <sub>HEX</sub> to form customer ID)
<b>Interface Configuration</b>				
02 <sub>HEX</sub>	6:0	000 0000 <sub>BIN</sub>	Slave_Addr	I <sup>2</sup> C™ slave address; valid range: 00 <sub>HEX</sub> to 7F <sub>HEX</sub> (default: 00 <sub>HEX</sub> ), Remark: address codes 04 <sub>HEX</sub> to 07 <sub>HEX</sub> are reserved for entering the I <sup>2</sup> C™ High Speed Mode
	8:7	00 <sub>BIN</sub>	-	Reserved
	9	0 <sub>BIN</sub>	SS_polarity	Determines the polarity of the Slave Select pin (SS) for SPI operation: <ul style="list-style-type: none"> <li>0 ⇔ Slave Select is active low (SPI and ZSSC3036 are active if SS==0)</li> <li>1 ⇔ Slave Select is active high (SPI and ZSSC3036 are active if SS==1)</li> </ul>
	11:10	00 <sub>BIN</sub>	CKP_CKE	Clock polarity and clock-edge select—determines polarity and phase of SPI interface clock with the following modes: <ul style="list-style-type: none"> <li>00 ⇔ SCLK is low in idle state, data latch with rising edge and data output with falling edge</li> <li>01 ⇔ SCLK is low in idle state, data latch with falling edge and data output with rising edge</li> <li>10 ⇔ SCLK is high in idle state, data latch with falling edge and data output with rising edge</li> <li>11 ⇔ SCLK is high in idle state, data latch with rising edge and data output with falling edge</li> </ul>
	15:12		-	Not assigned



MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
<b>Signal Conditioning Parameters</b>				
03 <sub>HEX</sub>	0	0 <sub>BIN</sub>	Offset_B[16]	Bridge offset, bit[16]—functions as the MSB and combines with Offset_B[15:0] in 05 <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	1	0 <sub>BIN</sub>	Offset_B_sign	Sign for sensor bridge offset (Offset_B): 0 => a positive value or 1 => a negative value
	2	0 <sub>BIN</sub>	Gain_B[16]	Bridge gain, bit[16] —functions as the MSB and combines with Gain_B[15:0] in 06 <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	3	0 <sub>BIN</sub>	Gain_B_sign	Sign of the sensor bridge gain (Gain_B): 0 => a positive value or 1 => a negative value
	4	0 <sub>BIN</sub>	Tcg[16]	1 <sup>st</sup> -order temperature coefficient of the bridge gain, bit[16] —functions as the MSB and combines with Tcg[15:0] in 07 <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	5	0 <sub>BIN</sub>	Tcg_sign	Sign of 1 <sup>st</sup> -order temperature coefficient (Tcg): 0 => a positive value or 1 => a negative value
	6	0 <sub>BIN</sub>	Tco[16]	1 <sup>st</sup> -order temperature coefficient of the bridge offset, bit[16] —functions as the MSB and combines with Tco[15:0] in 08 <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	7	0 <sub>BIN</sub>	Tco_sign	Sign of 1 <sup>st</sup> -order temperature coefficient (Tco): 0 => a positive value or 1 => a negative value
	8	0 <sub>BIN</sub>	SOT_tco[16]	2 <sup>nd</sup> -order temperature coefficient of the bridge offset, bit[16] —functions as the MSB and combines with SOT_tco[15:0] in 09 <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	9	0 <sub>BIN</sub>	SOT_tco_sign	Separate sign setting for 2 <sup>nd</sup> -order temperature coefficient (SOT_tco): 0 => a positive value or 1 => a negative value
	10	0 <sub>BIN</sub>	SOT_tcg[16]	2 <sup>nd</sup> -order temperature coefficient of the bridge gain, bit[16] —functions as the MSB and combines with SOT_tcg[15:0] in 0A <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	11	0 <sub>BIN</sub>	SOT_tcg_sign	Separate sign setting for 2 <sup>nd</sup> -order temperature coefficient (SOT_tcg): 0 => a positive value or 1 => a negative value

MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
	12	0 <sub>BIN</sub>	SOT_bridge[16]	2 <sup>nd</sup> -order coefficient of the bridge signal, bit[16] — functions as the MSB and combines with SOT_bridge[15:0] in 0B <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	13	0 <sub>BIN</sub>	SOT_bridge_sign	Separate sign setting for 2 <sup>nd</sup> -order bridge coefficient (SOT_bridge): 0 => a positive value or 1 => a negative value
	14	0 <sub>BIN</sub>	SOT_curve	Type of second-order curve correction for the bridge sensor signal. 0 ⇔ parabolic curve 1 ⇔ s-shaped curve
	15	0 <sub>BIN</sub>	TSETL_sign	Separate sign setting for T_SETL: 0 => a positive value or 1 => a negative value
04 <sub>HEX</sub>	0	0 <sub>BIN</sub>	Gain_T[16]	Temperature gain of temperature sensor, bit[16] — functions as the MSB and combines with Gain_T[15:0] in 0D <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	1	0 <sub>BIN</sub>	Gain_T_sign	Separate sign setting for the temperature gain (Gain_T): 0 => a positive value or 1 => a negative value
	2	0 <sub>BIN</sub>	SOT_T[16]	2 <sup>nd</sup> -order temperature coefficient of temperature sensor, bit[16] — functions as the MSB and combines with SOT_T[15:0] in 0E <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	3	0 <sub>BIN</sub>	SOT_T_sign	Separate sign setting for 2 <sup>nd</sup> -order temperature coefficient (SOT_T): 0 => a positive value or 1 => a negative value
	4	0 <sub>BIN</sub>	Offset_T[16]	Temperature offset of temperature sensor, bit[16] — functions as the MSB and combines with Offset_T[15:0] in 0C <sub>HEX</sub> to form the 17-bit coefficient's absolute value
	5	0 <sub>BIN</sub>	Offset_T_sign	Separate sign setting for the temperature offset (Offset_T): 0 => a positive value or 1 => a negative value
	15:6	0 0000 000 0 <sub>BIN</sub>	-	Not assigned

MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
05 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub> (7000 <sub>HEX</sub> )	Offset_B[15:0]	<p>Bits [15:0] of the bridge offset correction coefficient, which is an 18-bit wide absolute value (the respective MSBs Offset_B[16] and sign, Offset_B_sign, are under bits[1:0] in 03<sub>HEX</sub>)</p> <p>[-1/16 to 15/16] = 7000<sub>HEX</sub> (default for volume)            [-2/16 to 14/16] = 6000<sub>HEX</sub>            [-3/16 to 13/16] = 5000<sub>HEX</sub>            [-4/16 to 12/16] = 4000<sub>HEX</sub>            [-5/16 to 11/16] = 3000<sub>HEX</sub>            [-6/16 to 10/16] = 2000<sub>HEX</sub>            [-7/16 to 9/16] = 1000<sub>HEX</sub>            [-8/16 to 8/16] = 0000<sub>HEX</sub> (default for prototypes)</p>
06 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub> (8000 <sub>HEX</sub> )	Gain_B[15:0]	<p>Bits[15:0] of 17-bit wide absolute value of the bridge gain coefficient (default for prototypes: 0000<sub>HEX</sub>; default for volume production: 8000<sub>HEX</sub>—the respective MSBs, Gain_B[16] and sign, Gain_B_sign, are under bits[3:2] in 03<sub>HEX</sub>)</p>
07 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	Tcg[15:0]	<p>Coefficient for temperature correction of the bridge gain term – the respective MSBs, Tcg[16] and sign, Tcg_sign, are under (bits[5:4] in 03<sub>HEX</sub>)</p>
08 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	Tco[15:0]	<p>Coefficient for temperature correction of the bridge offset term – the respective MSBs, Tco[16] and sign, Tco_sign, are under (bits[7:6] in 03<sub>HEX</sub>)</p>
09 <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	SOT_tco[15:0]	<p>2<sup>nd</sup> order term applied to Tco – the respective MSBs, SOT_tco[16] and sign, SOT_tco_sign, are under (bits[9:8] in 03<sub>HEX</sub>)</p>
0A <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	SOT_tcg[15:0]	<p>2<sup>nd</sup> order term applied to Tcg. – the respective MSBs, SOT_tcg[16] and sign, SOT_tcg_sign, are under (bits[11:10] in 03<sub>HEX</sub>)</p>
0B <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	SOT_bridge[15:0]	<p>2<sup>nd</sup> order term applied to the sensor bridge readout – the respective MSBs, SOT_bridge[16] and sign, SOT_bridge_sign are under (bits[13:12] in 03<sub>HEX</sub>)</p>
0C <sub>HEX</sub>	15:0	0000 <sub>HEX</sub> (7000 <sub>HEX</sub> )	Offset_T[15:0]	<p>Bits [15:0] of the temperature offset correction coefficient (the respective MSBs, Offset_T[16] and sign, Offset_T_sign, are under (bits[5:4] in 04<sub>HEX</sub>)</p> <p>[-1/16 to 15/16] = 7000<sub>HEX</sub> (default for volume)            [-2/16 to 14/16] = 6000<sub>HEX</sub>            [-3/16 to 13/16] = 5000<sub>HEX</sub>            [-4/16 to 12/16] = 4000<sub>HEX</sub>            [-5/16 to 11/16] = 3000<sub>HEX</sub>            [-6/16 to 10/16] = 2000<sub>HEX</sub>            [-7/16 to 9/16] = 1000<sub>HEX</sub>            [-8/16 to 8/16] = 0000<sub>HEX</sub> (default for prototypes)</p>

MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
0D <sub>HEX</sub>	15:0	0000 <sub>HEX</sub> (8000 <sub>HEX</sub> )	Gain_T[15:0]	Bits [15:0] of the absolute value of the temperature gain coefficient (default for prototypes: 0000 <sub>HEX</sub> ; default for volume production: 8000 <sub>HEX</sub> ); the respective MSBs, Gain_T[16] and sign, Gain_T_sign, are under bits[1:0] in 04 <sub>HEX</sub> )
0E <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	SOT_T[15:0]	2 <sup>nd</sup> order term applied to the temperature reading – the respective MSBs, SOT_T[16] and sign, SOT_T_sign, are under (bits[3:2] in 04 <sub>HEX</sub> )
0F <sub>HEX</sub>	15:0	0000 <sub>HEX</sub>	T_SETL	Stores raw temperature reading at the temperature at which low calibration points were taken
<b>Measurement Configuration Register (BM_config)</b>				
10 <sub>HEX</sub>	1:0	00 <sub>BIN</sub>	Gain_stage1	Gain setting for the 1 <sup>st</sup> PREAMP stage with Gain_stage1: <ul style="list-style-type: none"> <li>• 00 ⇔ 12</li> <li>• 01 ⇔ 20</li> <li>• 10 ⇔ 30</li> <li>• 11 ⇔ 40</li> </ul>
	4:2	000 <sub>BIN</sub>	Gain_stage2	Gain setting for the 2 <sup>nd</sup> PREAMP stage with Gain_stage2: <ul style="list-style-type: none"> <li>• 000 ⇔ 1.1</li> <li>• 001 ⇔ 1.2</li> <li>• 010 ⇔ 1.3</li> <li>• 011 ⇔ 1.4</li> <li>• 100 ⇔ 1.5</li> <li>• 101 ⇔ 1.6</li> <li>• 110 ⇔ 1.7</li> <li>• 111 ⇔ 1.8</li> </ul>
	5	0 <sub>BIN</sub>	Gain_polarity	Set up the polarity of the sensor bridge's gain (inverting of the chopper) with <ul style="list-style-type: none"> <li>• 0 ⇔ positive (no polarity change)</li> <li>• 1 ⇔ negative (180° polarity change)</li> </ul>
	7:6	00 <sub>BIN</sub> (11 <sub>BIN</sub> )	Msb	Absolute number of bits for the MSB conversion in the ADC with Msb: <ul style="list-style-type: none"> <li>• 00 ⇔ 10-bit</li> <li>• 01 ⇔ 12-bit</li> <li>• 10 ⇔ 14-bit</li> <li>• 11 ⇔ 16-bit</li> </ul>

MTP Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
	9:8	00 <sub>BIN</sub>	Lsb	Absolute number of bits for the LSB conversion in the ADC with Lsb: <ul style="list-style-type: none"> <li>• 00 ⇔ 0-bit (single stage ADC)</li> <li>• 01 ⇔ 2-bit</li> <li>• 10 ⇔ 4-bit</li> <li>• 11 ⇔ 6-bit</li> </ul>
	12:10	000 <sub>BIN</sub>	A2D_Offset	ADC offset and resulting A2D input range [Vref] with A2D_Offset: <ul style="list-style-type: none"> <li>• 000 ⇔ 1/16 results in range [-1/16, 15/16]</li> <li>• 001 ⇔ 2/16 results in range [-2/16, 14/16]</li> <li>• 010 ⇔ 3/16 results in range [-3/16, 13/16]</li> <li>• 011 ⇔ 4/16 results in range [-4/16, 12/16]</li> <li>• 100 ⇔ 5/16 results in range [-5/16, 11/16]</li> <li>• 101 ⇔ 6/16 results in range [-6/16, 10/16]</li> <li>• 110 ⇔ 7/16 results in range [-7/16, 9/16]</li> <li>• 111 ⇔ 8/16 results in range [-8/16, 8/16]</li> </ul>
	14:13	00 <sub>BIN</sub>	Temp_ADC	Selection between fixed ADC segmentations for temperature measurements: <ul style="list-style-type: none"> <li>• 00 ⇔ setup according to IDT-reserved memory (recommended setup for best performance and speed trade-off)</li> <li>• 01 ⇔ MSB=16, LSB=0 (16-bit)</li> <li>• 10 ⇔ MSB=10, LSB=6 (16-bit)</li> <li>• 11 ⇔ MSB=12, LSB=4 (16-bit)</li> </ul>
	15	0 <sub>BIN</sub>	-	Reserved
11 <sub>HEX</sub>				Not assigned
12 <sub>HEX</sub>				Not assigned
13 <sub>HEX</sub>				Not assigned
14 <sub>HEX</sub>				Not assigned
15 <sub>HEX</sub>				Not assigned
16 <sub>HEX</sub>				Not assigned
17 <sub>HEX</sub>	15:0	-	ChecksumC	Generated (checksum) for user page through a linear feedback shift register (LFSR); signature is checked with power-up to ensure memory content integrity

The memory integrity checksum (referred to as *CRC*) is generated through a linear feedback shift register with the polynomial:

$$g(x) = x^{16} + x^{15} + x^2 + 1 \quad \text{with the initialization value: FFFF}_{\text{HEX}}$$

### 3.7. Calibration Sequence

Calibration essentially involves collecting raw signal and temperature data from the sensor-IC system for different known bridge values and temperatures. This raw data can then be processed by the calibration master (assumed to be a PC), and the calculated calibration coefficients can then be written to MTP memory. Below is a brief overview of the steps involved in calibrating the ZSSC3036.

There are three main steps to calibration:

1. *Assigning a unique identification to the ZSSC3036.* This identification is written to shadow RAM and later programmed in MTP memory. This unique identification can be stored in the two 16-bit registers dedicated to customer ID. It can be used as an index into a database stored on the calibration PC. This database will contain all the raw values of bridge readings and temperature readings for that part, as well as the known bridge measurand conditions and temperature to which the bridge was exposed.
2. *Data collection.* Data collection involves getting uncorrected or raw data from the bridge at different known measurand values and temperatures. Then this data is stored on the calibration PC using the unique identification of the device as the index to the database.
3. *Coefficient calculation and storage in MTP memory.* After enough data points have been collected to calculate all the desired coefficients, the coefficients can be calculated by the calibrating PC and written to the shadow RAM. After that, MTP memory is programmed with the contents of the shadow RAM.
4. *Result.* The sensor signal and the characteristic temperature effect on output will be linearized according to the setup-dependent maximum output range.

It is essential to perform the calibration with a fixed programming setup during the data collection phase. In order to prevent any accidental misprocessing, it is further recommended to keep the MTP memory setup stable during the whole calibration process as well as in the subsequent operation. A ZSSC3036 calibration only fits the single setup used during its calibration. Changes of functional parameters after a successful calibration can decrease the precision and accuracy performance of the ZSSC3036 as well as of the whole application.

### 3.7.1. Calibration Step 1 – Assigning Unique Identification

Assign a unique identification number to the ZSSC3036 by using the memory write command ( $40_{\text{HEX}} + \text{data}$  and  $41_{\text{HEX}} + \text{data}$ ; see Table 3.1 and Table 3.8) to write the identification number to Cust\_ID0 at memory address  $00_{\text{HEX}}$  and Cust\_ID1 at address  $01_{\text{HEX}}$  as described in section 3.6.1. These two 16-bit registers allow for more than 4 trillion unique devices.

### 3.7.2. Calibration Step 2 – Data Collection

The number of unique points (measurand and/or temperature) at which calibration must be performed generally depends on the requirements of the application and the behavior of the resistive bridge in use. The minimum number of points required is equal to the number of bridge coefficients to be corrected with a minimum of three different temperatures at three different bridge values. For a full calibration resulting in values for all 7 possible bridge coefficients and 3 possible temperature coefficients, a minimum of 7 pairs of bridge with temperature measurements must be collected.

Within this minimum 3x3 measurements field, data must be collected for the specific value pairs (at known conditions) and then processed to calculate the coefficients. In order to obtain the potentially best and most robust coefficients, it is recommended that measurement pairs (temperature vs. measurand) be collected at the outer corners of the intended operation range or at least at points that are located far from each other. It is also essential to provide highly precise reference values as nominal, expected values. The measurement precision of the external calibration-measurement equipment should be ten times more accurate than the expected ZSSC3036 output precision after calibration in order to avoid precision losses caused by the nominal reference values (e.g., measurand signal and temperature deviations).

*Note: An appropriate selection of measurement pairs can significantly improve the overall system performance.*

The determination of the measurand-related coefficients will use all of the measurement pairs. For the temperature-related correction coefficients, 3 (at three different temperatures) of the measurement pairs will be used.

*Note: There is an inherent redundancy in the 7 bridge-related and 3 temperature-related coefficients. Since the temperature is a necessary output (which also needs correction), the temperature-related information is mathematically separated, which supports faster and more efficient DSP calculations during the normal usage of the sensor-IC system.*

The recommended approach for data collection is to make use of the raw-measurement commands:

- For bridge sensor values:
  - $A2_{\text{HEX}} + 0000_{\text{HEX}}$ : single bridge measurement for which the configuration register will be loaded from the *BM\_Config* register ( $10_{\text{HEX}}$  in MTP); preprogramming the measurement setup in the MTP is required.
  - $A3_{\text{HEX}} + \text{ssss}_{\text{HEX}}$ : single bridge measurement for which the *BM\_Config* configuration register (Gain, ADC, Offset, etc.) will be loaded as  $\text{ssss}_{\text{HEX}}$  and must be provided externally via the interface.

- For temperature values:
  - $A6_{\text{HEX}} + 0000_{\text{HEX}}$ : single temperature measurement for which the configuration register will be loaded from an internal temperature configuration register (preprogrammed by IDT in MTP); preprogramming of the respective configuration is done by IDT prior to IC delivery. This is the recommended approach for temperature data collection.
  - $A7_{\text{HEX}} + \text{ssss}_{\text{HEX}}$ : single temperature measurement for which the configuration register (Gain, ADC, Offset, etc.) will be loaded as  $\text{ssss}_{\text{HEX}}$  and must be provided externally via the interface. The data composition of the temperature configuration register is similar to the *BM\_config* (address  $10_{\text{HEX}}$ ) register for the bridge sensor.

### 3.7.3. Calibration Step 3 – Coefficient Calculations

The math to perform the coefficient calculation is complicated and will not be discussed in detail. There is a brief overview in the next section. IDT will provide software (DLLs) to perform the coefficient calculation (external to the sensor-IC system) based on auto-zero corrected values. After the coefficients are calculated, the final step is to write them to the MTP memory of the ZSSC3036.

## 3.8. The Calibration Math

### 3.8.1. Bridge Signal Compensation

The saturation check in the ZSSC3036 is enhanced compared with older SSCs from IDT. Even saturation effects of the internal calculation steps are detected, allowing the final correction output to still be determined. It is possible to get potentially useful signal conditioning results which have had an intermediate saturation during the calculations – these cases are detectable by observing the status bit[0] for each measurement result. Details about the saturation limits and the valid ranges for values are provided in the following equations.

*SOT\_curve* selects whether second-order equations compensate for sensor nonlinearity with a parabolic or S-shaped curve. The parabolic compensation is recommended.



The correction formula for the differential signal reading is represented as a two-step process depending on the  $SOT\_curve$  setting.

**Equations for the parabolic  $SOT\_curve$  setting ( $SOT\_curve = 0$ ):**

*Simplified:*

$$\Delta T = T\_Raw - T_{SETL} \quad (5)$$

$$K_1 = 2^{15} + \frac{\Delta T}{2^{15}} \cdot \left( \frac{SOT\_tcg}{2^{15}} \cdot \Delta T + Tcg \right) \quad (6)$$

$$K_2 = Offset\_B + BR\_Raw + \frac{\Delta T}{2^{15}} \cdot \left( \frac{SOT\_tco}{2^{15}} \cdot \Delta T + Tco \right) \quad (7)$$

$$Z_{BP} = \frac{Gain\_B}{2^{15}} \cdot \frac{K_1}{2^{15}} \cdot K_2 + 2^{15} \quad (\text{delimited to positive number range}) \quad (8)$$

$$B = \frac{Z_{BP}}{2^{15}} \cdot \left( \frac{SOT\_bridge}{2^{15}} \cdot Z_{BP} + 2^{15} \right) \quad (\text{delimited to positive number range}) \quad (9)$$

*Complete:*

$$\Delta T = \left[ T\_Raw - T_{SETL} \right]_{-2^{17}}^{2^{17}-1} \quad (10)$$

$$K_1 = \left[ 2^{15} + \left[ \frac{\Delta T}{2^{15}} \cdot \left[ \left[ \frac{SOT\_tcg}{2^{15}} \cdot \Delta T \right]_{-2^{17}}^{2^{17}-1} + Tcg \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \quad (11)$$

$$K_2 = \left[ Offset\_B + \left[ BR\_Raw + \left[ \frac{\Delta T}{2^{15}} \cdot \left[ \left[ \frac{SOT\_tco}{2^{15}} \cdot \Delta T \right]_{-2^{17}}^{2^{17}-1} + Tco \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \quad (12)$$

$$Z_{BP} = \left[ \left[ \frac{Gain\_B}{2^{15}} \cdot \left[ \frac{K_1}{2^{15}} \cdot K_2 \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_{-2^{17}}^{2^{17}-1} \right]_0^{2^{17}-1} \quad (13)$$

$$B = \left[ \frac{Z_{BP}}{2^{15}} \cdot \left[ \left[ \frac{SOT\_bridge}{2^{15}} \cdot Z_{BP} \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_{-2^{17}}^{2^{17}-1} \right]_0^{2^{16}-1} \quad (14)$$

**Equations for the S-shaped SOT\_curve setting (SOT\_curve = 1):**

*Simplified:*

$$Z_{BS} = \frac{Gain\_B}{2^{15}} \cdot \frac{K_1}{2^{15}} \cdot K_2 \quad (15)$$

$$B = \frac{Z_{BS}}{2^{15}} \cdot \left( \frac{SOT\_bridge}{2^{15}} \cdot |Z_{BS}| + 2^{15} \right) \quad (\text{delimited to positive number range}) \quad (16)$$

*Complete:*

$$Z_{BS} = \left[ \frac{Gain\_B}{2^{15}} \cdot \left[ \frac{K_1}{2^{15}} \cdot K_2 \right]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} \quad (17)$$

$$B = \left[ \frac{Z_{BS}}{2^{15}} \cdot \left[ \left[ \frac{SOT\_bridge}{2^{15}} \cdot |Z_{BS}| \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_{0}^{2^{16}} \quad (18)$$

**Where**

- B** = Corrected bridge reading output via I<sup>2</sup>C™ or SPI; range [0<sub>HEX</sub> to FFFF<sub>HEX</sub>];
- BR\_Raw** = Raw bridge reading from ADC after AZ correction; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- Gain\_B** = Bridge gain term; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- Offset\_B** = Bridge offset term; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- Tcg** = Temperature coefficient gain term; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- Tco** = Temperature coefficient offset term; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- T\_Raw** = Raw temperature reading after AZ correction; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- T<sub>SETL</sub>** = T\_Raw reading at which low calibration was performed (e.g., 25°C); range [-FFFF<sub>HEX</sub> to FFFF<sub>HEX</sub>];
- SOT\_tcg** = Second-order term for Tcg non-linearity; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- SOT\_tco** = Second-order term for Tco non-linearity; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- SOT\_bridge** = Second-order term for bridge non-linearity; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- |...|** = absolute value
- [...]<sub>ll</sub><sup>ul</sup>** = bound/saturation number range from ll to ul, over/under-flow is reported as saturation in status byte.

### 3.8.2. Temperature Signal Compensation

Temperature is measured internally. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation for nonlinearity is always parabolic. Again, the correction formula is best represented as a two-step process as follows:

*Simplified:*

$$Z_T = \frac{Gain\_T}{2^{15}} \cdot (T\_Raw + Offset\_T) + 2^{15} \quad (\text{delimited to positive number range}) \quad (19)$$

$$T = \frac{Z_T}{2^{15}} \cdot \left( \frac{SOT\_T}{2^{15}} \cdot Z_T + 2^{15} \right) \quad (\text{delimited to positive number range}) \quad (20)$$

*Complete:*

$$Z_T = \left[ \left[ \frac{Gain\_T}{2^{15}} \cdot [T\_Raw + Offset\_T]_{-2^{17}}^{2^{17}-1} \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_0^{2^{17}-1} \quad (21)$$

$$T = \left[ \frac{Z_T}{2^{15}} \cdot \left[ \left[ \frac{SOT\_T}{2^{15}} \cdot Z_T \right]_{-2^{17}}^{2^{17}-1} + 2^{15} \right]_{-2^{17}}^{2^{16}-1} \right]_0^{2^{16}-1} \quad (22)$$

#### Where

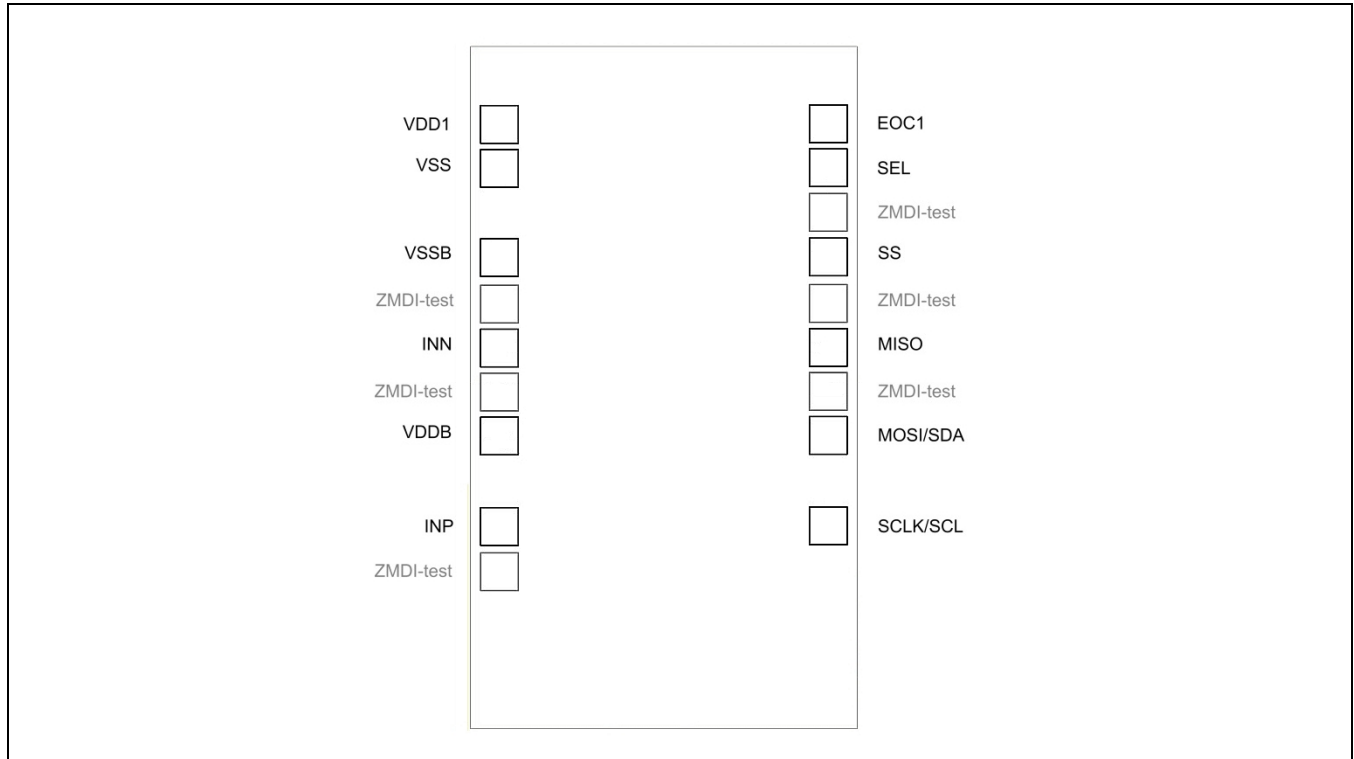
- Gain\_T* = Gain coefficient for temperature; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- T\_Raw* = Raw temperature reading after AZ correction; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- Offset\_T* = Offset coefficient for temperature; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>];
- SOT\_T* = Second-order term for temperature source non-linearity; range [-1FFFF<sub>HEX</sub> to 1FFFF<sub>HEX</sub>]

## 4 Die Pad Assignments

The ZSSC3036 is available in die form. See Figure 4.1 for pad assignments.

Note that the ZMDI-test pads are for IDT use only.

**Figure 4.1 ZSSC3036 Pad Assignments**



**Table 4.1 Pad Assignments**

Name	Direction	Type	Description
VDD1	IN	Supply	IC positive supply voltage for the IC, regular bond pad
VDD2			IC positive supply voltage for the IC, special pad (electrically connected to VDD1, also bondable)
VSS	IN	Supply	Ground reference voltage signal
VSSB	OUT	Analog	Negative bridge supply (bridge sensor ground)
VDDB	OUT	Analog	Positive bridge supply
INP	IN	Analog	Positive bridge signal
INN	IN	Analog	Negative bridge signal

Name	Direction	Type	Description
EOC1	OUT	Digital	End of conversion, regular bond pad
EOC2			End of conversion, special pad (electrically connected to EOC1, also bondable)
SEL	IN	Digital	I <sup>2</sup> C™ or SPI interface select
SCLK/SCL	IN	Digital	Clock input for SPI/I <sup>2</sup> C™
MOSI/SDA	IN/Out	Digital	Data input for SPI; data in/out for I <sup>2</sup> C™
MISO	OUT	Digital	Data output for SPI
SS	IN	Digital	Slave select for SPI
ZMDI-test	-	-	do not connect to these pads

## 5 Quality and Reliability

The ZSSC3036 is available in standard and extended qualification IC versions. For the standard version ZSSC3036CCxxx, all data specified parameters are guaranteed if not stated otherwise.

For the extended qualification version ZSSC3036Cxxx, there is also specific testing in order to sort for IC-specific (HTOL-qualified) early failures.

## 6 Ordering Sales Codes

Sales Code	Description	Package
ZSSC3036CC1B	Die—temperature range: –40°C to +85 °C	Wafer (304µm) unsawn, tested
ZSSC3036CC6B	Die—temperature range: –40°C to +85 °C	Wafer (725µm) unsawn, tested
ZSSC3036CI1B	Die—temperature range: –40°C to +85 °C, extended qualification	Wafer (304µm) unsawn, tested
ZSSC3036CI6B	Die—temperature range: –40°C to +85 °C, extended qualification	Wafer (725µm) unsawn, tested
ZSSC3036CC1C	Die—temperature range: –40°C to +85°C	Dice on frame (304µm), tested
ZSSC3036CI1C	Die—temperature range: –40°C to +85°C, extended qualification	Dice on frame (304µm), tested
ZSSC3036CI1BH	Die—temperature range: –40°C to +110 °C, 1 extended qualification	Wafer (304µm) unsawn, tested
ZSSC3036CI6BH	Die—temperature range: –40°C to +110 °C, extended qualification	Wafer (725µm) unsawn, tested
ZSSC3036CI1CH	Die—temperature range: –40°C to +110 °C, extended qualification	Dice on frame (304µm), tested
ZSSC30x6-KIT	Evaluation Kit for ZSSC30x6 Product Family, including boards, cable, software, and 1 sample	Kit

Contact IDT Sales for additional information.

## 7 Related Documents

Document
ZSSC3036 Feature Sheet
ZSSC3036 Application Note: Application Circuits
ZSSC30x6 Evaluation Kit Documentation
ZSSC30x6 Application Note: Calibration

Visit the ZSSC3036 product page [www.IDT.com/ZSSC3036](http://www.IDT.com/ZSSC3036) or contact your nearest sales office for the latest version of these documents.

## 8 Glossary

Term	Description
A2D	Analog-to-Digital
ACK	Acknowledge (interface's protocol indicator for successful data/command transfer)
ADC	Analog-to-Digital Converter Or Conversion
AZ	Auto-Zero (unspecific)
AZB	Auto-Zero Measurement for Sensor Bridge Path
AZT	Auto-Zero Measurement for Temperature Path
CLK	Clock
DAC	Digital-to-Analog Conversion or Converter
DF	Data Fetch (this is a command type)
DSP	Digital Signal Processor (digital configuration, calibration, calculation, communication unit)
EOC	End of Conversion
FSO	Full Scale Output (value in percent relative to the adc maximum output code; resolution dependent)
HTOL	High Temperature Operating Life
LSB	Least Significant Bit ("fine" portion of the converted signal)
LFSR	Linear Feedback Shift Register
MISO	Master Input, Slave Output (SPI)
MOSI	Master Output, Slave Input (SPI)
MR	Measurement Request (this is a command type)
MSB	Most Significant Bit ("coarse" portion of the converted signal)
MTP	Multiple-Time Programmable
NACK	Not Acknowledge (interface's protocol indicator for unsuccessful data/command transfer)
OTP	One Time Programmable
POR	Power-On Reset

Term	Description
PreAmp	Preamplifier
PSRR	Power Supply Disturbance Rejection
SCL	Serial Clock Line (I <sup>2</sup> C™)
SCLK	Serial Clock (SPI)
SDA	Serial Data Line (I <sup>2</sup> C™)
SM	Signal Measurement
SOT	Second-Order Term
SPI	Serial Peripheral Interface
SS	Slave Select (SPI)
TC	Temperature Coefficient (of a resistor or the equivalent bridge resistance)
TM	Temperature Measurement

## 9 Document Revision History

Revision	Date	Description
1.00	June 12, 2012	First release of data sheet.
1.10	January 22, 2013	Corrected measurement duration values; new contact information table.
1.20	May 28, 2013	Update for contact information and imagery for cover and headers.
2.00	March 13, 2014	Reduction of internal oscillator frequency, conversion rates, and ADC clock frequency; increase in ADC-conversion times; longer start-up and wake-up times.
2.01	August 24, 2014	Update for contact information. Minor edits for die information.
	April 20, 2016	Changed to IDT branding.