ZSSC3123

cLite™ Capacitive Sensor Signal Conditioner

Description

The ZSSC3123 is a CMOS integrated circuit for accurate capacitance-to-digital conversion and sensor-specific correction of capacitive sensor signals. Digital compensation of sensor offset, sensitivity, and temperature drift is accomplished via an internal digital signal processor running a correction algorithm with calibration coefficients stored in a non-volatile EEPROM.

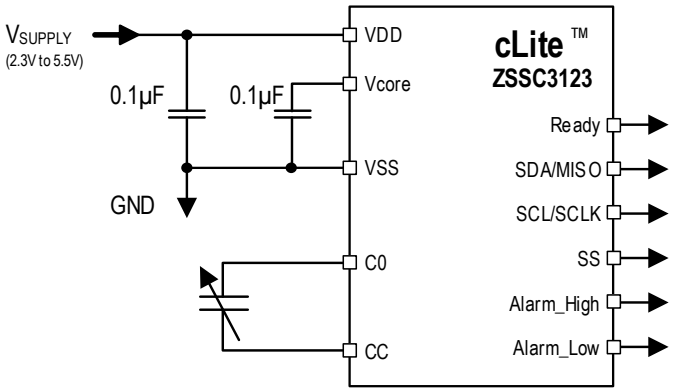
The ZSSC3123 is configurable for capacitive sensors with capacitances up to 260pF and a sensitivity of 125aF/LSB to 1pF/LSB depending on resolution, speed, and range settings. It is compatible with both single capacitive sensors (both terminals must be accessible) and differential capacitive sensors. Measured and corrected sensor values can be output as I2C, SPI, pulse density modulation (PDM), or alarms.

The I2C interface can be used for a simple PC-controlled calibration procedure to program a set of calibration coefficients into an on-chip EEPROM. The calibrated ZSSC3123 and a specific sensor are mated digitally: fast, precise, and without the cost overhead of trimming by external devices or laser.

Available Support

- ZSSC3123 SSC Evaluation Kit available: SSC Evaluation Board, samples, software, documentation.
- Support for industrial mass calibration available.
- Quick circuit customization option for large production volumes.

Application: Digital Output, Alarms



Features

- Maximum target input capacitance: 260pF
- Sampling rates as fast as 0.7ms at 8-bit resolution; 1.6ms at 10-bit; 5.0ms at 12-bit; 18.5ms at 14-bit
- Digital compensation of sensor: piece-wise 1st and 2nd order sensor compensation or up to 3rd order single-region sensor compensation
- Digital compensation of 1st and 2nd order temperature gain and offset drift
- Internal temperature compensation reference (no external components)
- Programmable capacitance span and offset
- Layout customized for die-die bonding with sensor for low-cost, high-density chip-on-board assembly
- Accuracy as high as ±0.25% FSO at -40°C to 125°C, 3V, 5V, Vsupply ±10% (see data sheet section 5 for restrictions)
- Minimized calibration costs: no laser trimming, one-pass calibration using a digital interface
- Wide capacitance range to support a broad portfolio of different sensor elements
- Excellent for low-power battery applications
- I2C or SPI interface—easy connection to a microcontroller
- PDM outputs (Filtered Analog Ratiometric) for both capacitance and temperature
- Up to two alarms that can act as full push-pull or open-drain switches
- Supply voltage: 2.3V to 5.5V
- Typical current consumption 750µA down to 60µA depending on configuration
- Typical Sleep Mode current: ≤ 1µA at 85°C
- Operation temperature: –40°C to +125°C depending on part code
- Die or 4.4 × 5.0 mm 14-TSSOP package

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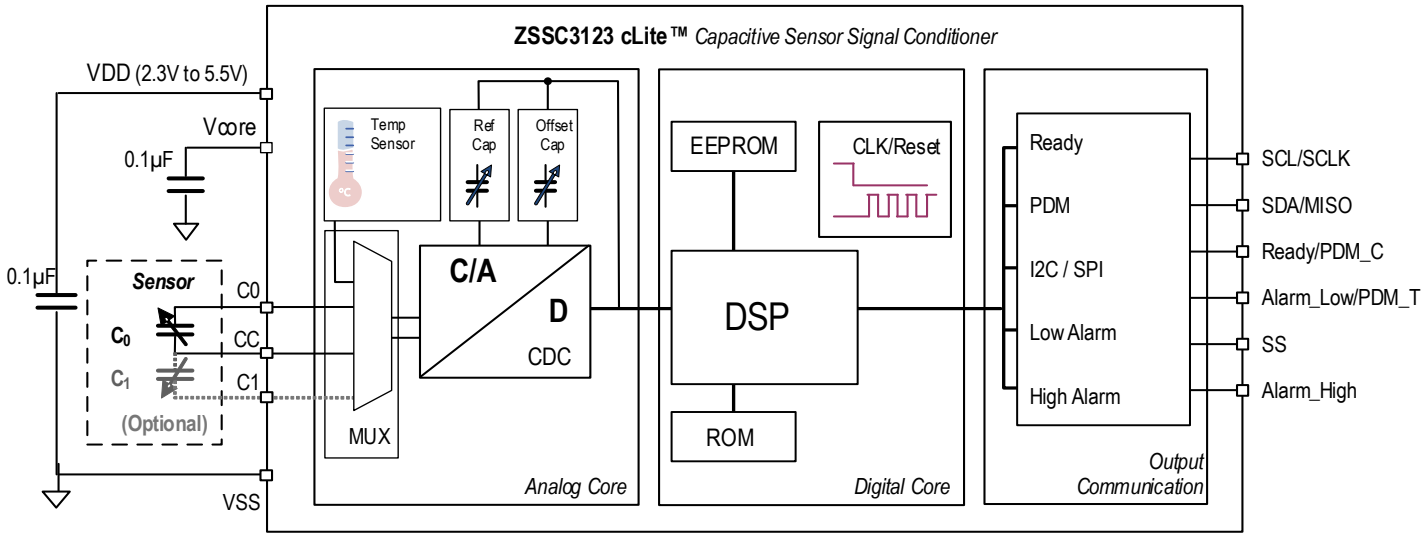
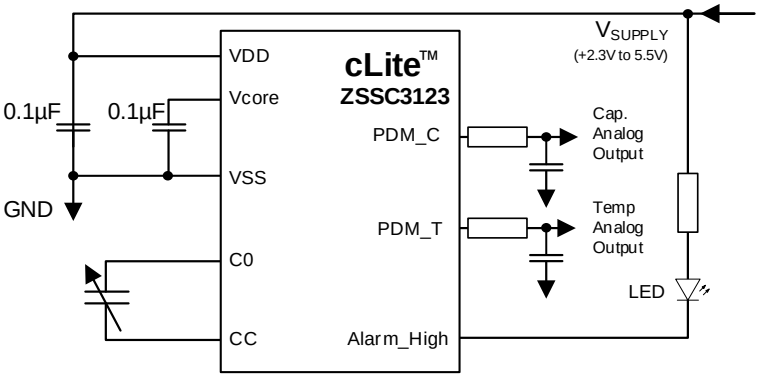
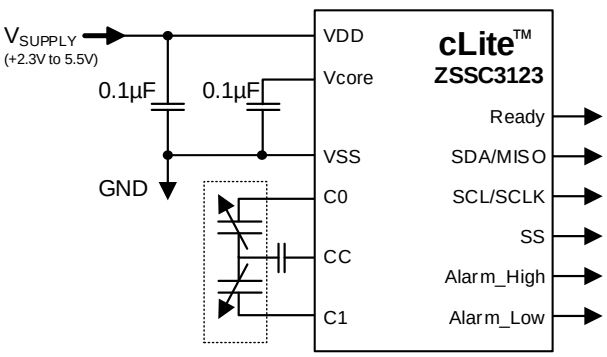
Block Diagram



Application: Analog Output



Application: Differential Capacitance Input



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1. Pin Assignments

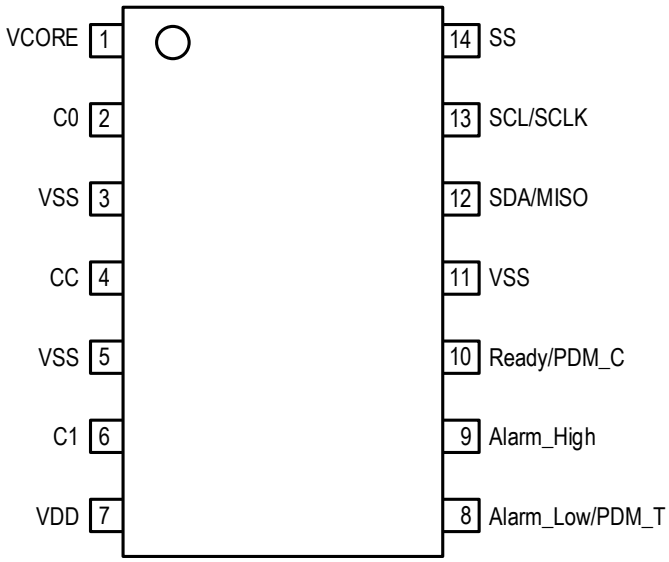

Figure 1. Pin Assignments for 4.4mm × 5.0mm 14-TSSOP – Top View

2. Pin Descriptions

Table 1. Pin Descriptions

Pin	Name	Description	Notes
1	VCORE	Core voltage	Always connect the VCORE pin to an external capacitor to ground that is within the specifications given in section 4 for C_{VCORE_SM} and C_{VCORE_UM}. This is the only internal module pin. For ESD details, see section 15.
2	C0	Capacitor input 0	
3	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.
4	CC	Common capacitor input	
5	VSS	Ground supply	Connecting to GND for shielding is strongly recommended.
6	C1	Capacitor input 1	If not used, must be unconnected.
7	VDD	Supply voltage (1.8V to 5.5V) 2.3V to 5.5V for ZSSC3123	VDD must be connected to V_{SUPPLY}. See section 4.
8	Alarm_Low/PDM_T	Low alarm output Temperature PDM (see Table 20)	If not used, must be unconnected.
9	Alarm_High	High alarm output	If not used, must be unconnected.
10	Ready/PDM_C	Ready signal (conversion complete output) Capacitance PDM (see Table 20)	If not used, must be unconnected.

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Pin	Name	Description	Notes
11	VSS	Ground supply	Must connect to GND.
12	SDA/MISO	I2C data if in I2C Mode Master-In-Slave-Out if in SPI Mode (see Table 20)	If not used, must connect to VDD.
13	SCL/SCLK	I2C clock if in I2C Mode Serial clock if in SPI Mode (see Table 20)	If not used, must connect to VDD.
14	SS	Slave Select (input) if in SPI Mode (see Table 20)	If not used, must be unconnected.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed in Table 2 can cause permanent damage to the device. Functional operation of the device at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Analog Supply Voltage	-0.3		6.0	V
V_{INA}	Voltages at Analog I/O – In Pin	-0.3		V_{DD}+0.3	V
V_{OUTA}	Voltages at Analog I/O – Out Pin	-0.3		V_{DD}+0.3	V
T_{STOR}	Storage Temperature Range	-55		150	°C

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4. Recommended Operating Conditions

Table 3. Recommend Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{SUPPLY}	Supply Voltage to Ground	2.3		5.5	V
T_{AMB}	Ambient Temperature Range[a]	-40		125	°C
I_{OUT}	Output Pads/Pins Drive Strength[b]	1.5		20	mA
$C_{VSUPPLY}$	External Capacitance between V_{DD} pin and Ground	100	220	470	nF
C_{VCORE_SM}	External Capacitance between Vcore and Ground – Sleep Mode	10		110	nF
C_{VCORE_UM}	External Capacitance between Vcore and Ground – Update Mode	90		330	nF
C_0	Input Capacitance Span (Full Scale Values)	2		260	pF
C_1	External Reference Capacitance	2		260	pF
C_{CC}	External Isolating Capacitance (Mult1) (CC pin to sensor common node) [c], [d]			16	pF
R_{PU}	I2C Pull-up Resistor	1	2.2		kΩ
C_{SDA}	SDA/MISO Load Capacitance			200	pF

[a]Caution: If buying die, select the proper package to ensure that the maximum junction temperature is not exceeded.

[b]See section 7 for full details on output pad drive strengths.

[c]An external isolating capacitor allows a non-galvanic connection to special differential or external reference sensor types. C_{CC} could also be used to lower the overall capacitance level to a value that is supported by the ZSSC3123 because it limits the maximum capacitance seen by the ZSSC3123 input to CC even if C0 and C1 have higher values. See section 9.2.1.3 for more details.

[d]The series combination of sensor and CC must not exceed the maximum capacitance allowed for the chosen Mult setting.

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5. Electrical Characteristics

Table 4. Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Supply Current						
I_{DD}	Update Mode Current (varies with part configuration) [a]	Best case settings: [b] Mult 1, 8-bit, 125ms Power Down		60	100	µA
		Worst case settings: Mult 1, 14-bit, 0ms Power Down		750	1100	
I_{PDM}	Extra Current with PDM enabled [b]			150		µA
I_{SLEEP}	Sleep Mode Current [a]	-40 to 85°C		0.6	1	µA
		-40 to 125°C		1	3	µA
Voltage Levels						
V_{POR}	Power-On-Reset Level		1.6	1.7	2.2	V
V_{REG}	Active Regulated Voltage	Note: Regulated voltage can be measured on the Vcore pin.	2.4	2.55	2.7	V
Capacitance-to-Digital Converter (CDC)						
RES_{CDC}	Resolution		8		14	Bits
f_{MULT1}	Excitation Frequency of External Capacitances C0 and C1 (for a system frequency f_{SYS})	Mult 1		$f_{SYS}/2$		kHz
f_{MULT2}		Mult 2		$f_{SYS}/4$		kHz
f_{MULT4}		Mult 4		$f_{SYS}/8$		kHz
f_{MULT8}		Mult 8		$f_{SYS}/16$		kHz
INL_{CDC}	Integral Nonlinearity (INL) [c]	Mult 1, 10% to 90% input, 14-bit			0.2	%
DNL_{CDC}	Differential Nonlinearity (DNL) [b]	Mult 1, 10% to 90% input, 14-bit			0.9	LSB
EEPROM						
n_{WRI_EEP}	Number of Erase/Write Cycles	At 85°C			100k	
t_{WRI_EEP}	Data Retention	At 100°C			10	Year
Temperature Conversion						
RES_{TEMP}	Resolution in °C [b]	-40 to 125°C, 8-bit mode	0.64	0.96	1.6	°C
		-40 to 125°C, 14-bit mode	0.01	0.015	0.025	
INL_{CDC}	Nonlinearity First Order Fit [b], [d]	-40 to 125°C		±0.5	±1	°C
INL_{CDC}	Nonlinearity Second Order Fit [b], [e]	-40 to 125°C		±0.2	±0.4	°C
PSR_{TEMP}	Voltage Dependency [b]	$V_{SUPPLY} > V_{REG}+0.25V$		0.03	0.1	°C/V
		$2.3V \le V_{SUPPLY} \le V_{REG} + 0.25V$		1.25	2.25	
PDM Output						
V_{PDM_Range}	Output Range [b]		10		90	$\%V_{SUPPLY}$
f_{PDM}	PDM Frequency			$f_{SYS}/8$		kHz
t_{SETT}	Filter Settling Time [b], [f]	0% to 90% LP filter 10kΩ/400nF			9.2	ms
V_{RIPP}	Ripple [b], [f]	0% to 90% LP filter 10kΩ/400nF			1.0	mV/V

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Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
E_{PDM}	PDM Additional Error (Including Ratiometricity Error) [b]	-40 to 125°C		0.1	0.5	%
Digital I/O						
V_{OL}	Voltage Output Level Low			0	0.2	V_{SUPPLY}
V_{OH}	Voltage Output Level High		0.8	1		V_{SUPPLY}
V_{IL}	Voltage Input Level Low			0	0.2	V_{SUPPLY}
V_{IH}	Voltage Input Level High		0.8	1		V_{SUPPLY}
C_{IN}	Communication Pin Input Capacitance [b]				10	pF
Total System						
C_{tol}	Capacitive Tolerance Between Parts [b]	All capacitive values in the specification are subject to this variation			±10	%
f_{SYS}	Trimmed System Frequency	All timing in this specification is subject to this variation.	1.76	1.85	1.94	MHz
f_{var}	Frequency Variation Over Voltage and Temperature	All timing in this specification is subject to this variation.			±10	%
t_{STA}	Start-Up-Time [b], [g], [h] Power-on (POR) to data ready	Fastest and slowest settings	4.25		173	ms
t_{RESP_UP}	Update Rate (Update Mode) [b], [g], [h]	Fastest and slowest settings	0.70		288	ms
t_{RESP_SL}	Response Time (Sleep Mode) [b], [g], [h]	Fastest and slowest settings	1.25		163	ms
	Parasitic to Ground Tolerance Including package parasitics (Pins C0, CC, and C1) [b]	Mult 1			10	pF
		Mult 2			20	pF
		Mult 4			40	pF
		Mult 8			80	pF
N_{OUT}	Peak-to-Peak Noise @ output (100 measurements in 14 bit) [b]	Mult 1, 2, 4, 8		5	20	LSB
AE_{out}	Error Mult 1, -40 to 125°C [b], [i], [j], [k]	3V±10%, 3.3V±10%, 5V±10%		±0.25	±0.75	%FSO
		2.5V±10%		±0.50	±1.25	%FSO
AE_{out}	Mult 2, 4, 8, -40 to 125°C [b], [i], [j], [k]	3V±10%, 3.3V±10%, 5V±10%		±0.50	±1.25	%FSO
		2.5V±10%		±1.50	±3.00	%FSO

[a]See section 6 for full details for current consumption in each mode.
[b]Parameter not tested during production but guaranteed by design.
[c]Parameter measured using internal test capacitors (0pF to 7pF in Mult 1).
[d]Assumes optimal calibration points of 0°C and 100°C; see section 8 for more details.
[e]Assumes optimal calibration points of -20°C, 40°C and 100°C; see section 8 for more details.
[f] See section 10.7 for more details.
[g]See section 10 for more details.
[h]Timing values are for a nominal oscillator, for worst case, ±10% total frequency variation, multiply by 0.9 (minimum time) or 1.1 (maximum time).
[i] Accuracy specification includes a 2-point temperature calibration for correcting the internal TC.
[j] Accuracy specification assumes maximum parasitics of 10pF to ground.
[k]Accuracy specification does not include PDM errors; see the PDM Output electrical parameters for additional errors when using PDM.

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6. Current Consumption Graphs

Part current consumption depends on a number of different factors including voltage, temperature, capacitive input, Mult, resolution, and power down time. The best method for calculating the ZSSC3123's power consumption is to measure the current consumption with the actual setup. If measurement is not possible, then the graphs in this section can provide a starting point for estimating the current consumption.

6.1 Update Mode Current Consumption

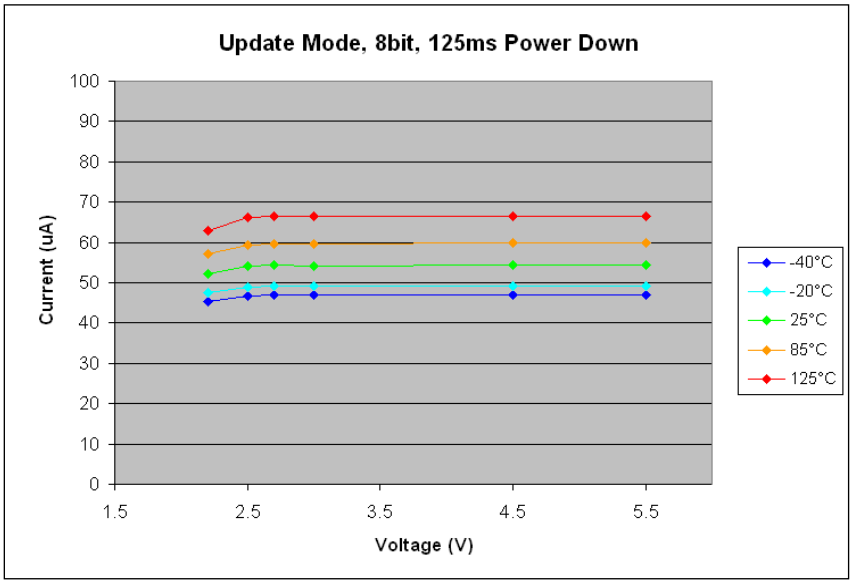

Figure 2. Best Case Settings (Typical Part)

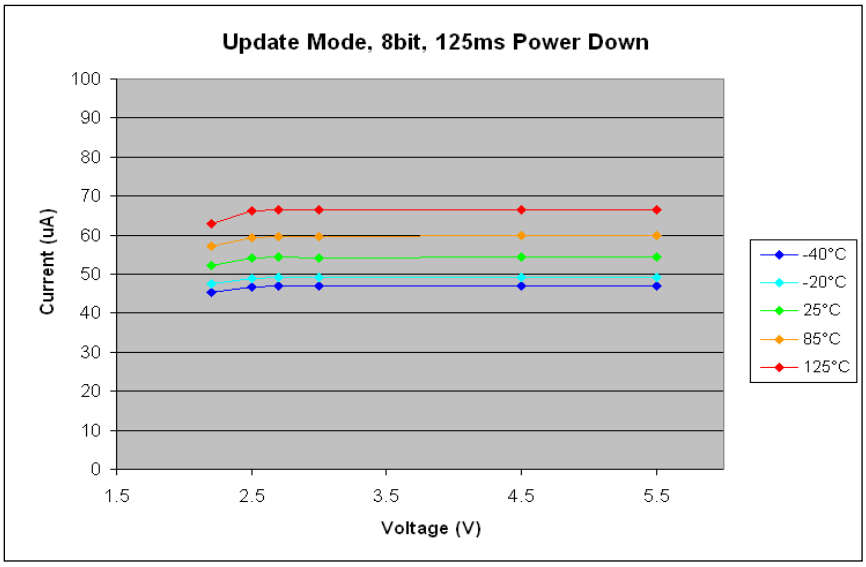

Figure 3. Worst Case Settings (Typical Part)

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6.2 Sleep Mode Current Consumption

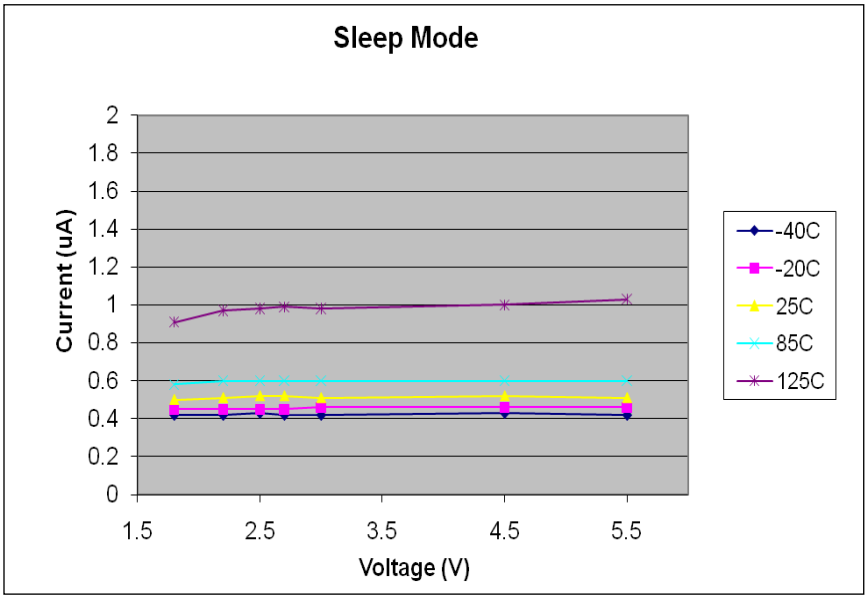

Figure 4. Typical Current Consumption during Sleep Mode (No Measurements)

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7. Output Pad Drive Strength

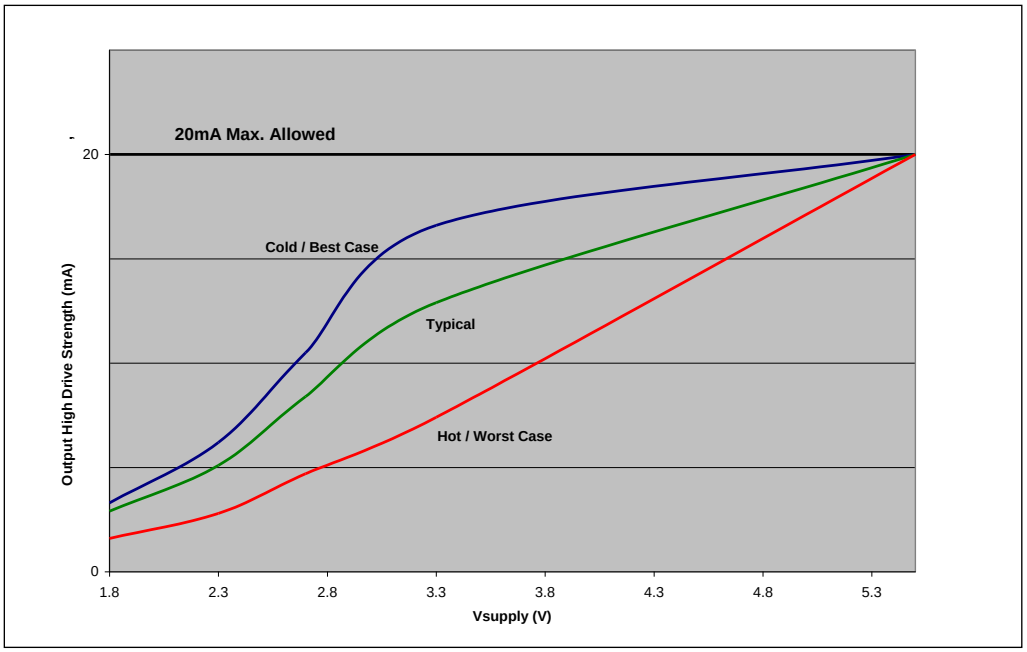

Figure 5. Output High Drive Strength Graph

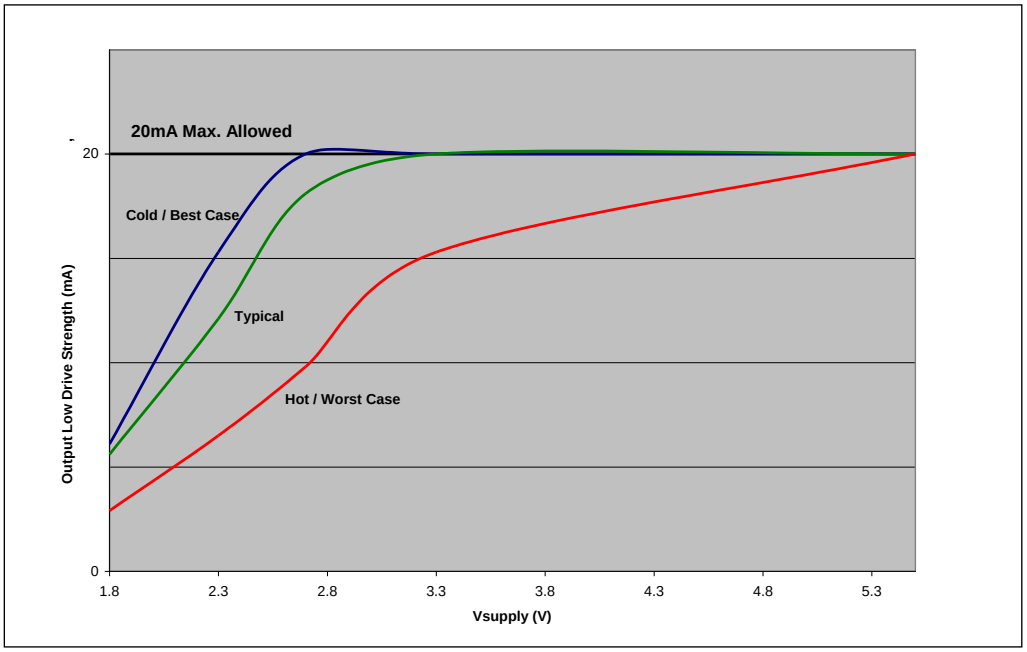

Figure 6. Output Low Drive Strength Graph

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8. Temperature Sensor Nonlinearity

Temperature sensor nonlinearity can vary depending on the type of calibration and the selected calibration points. It is highly recommended that a temperature calibration is done with calibration points at least 20°C apart from each other. The following figures show the resulting nonlinearity error for the full temperature range (-40°C to 125°C) using the optimal calibration points 0°C and 100°C for a first-order fit and -20°C, 40°C, and 100°C for a second-order fit.

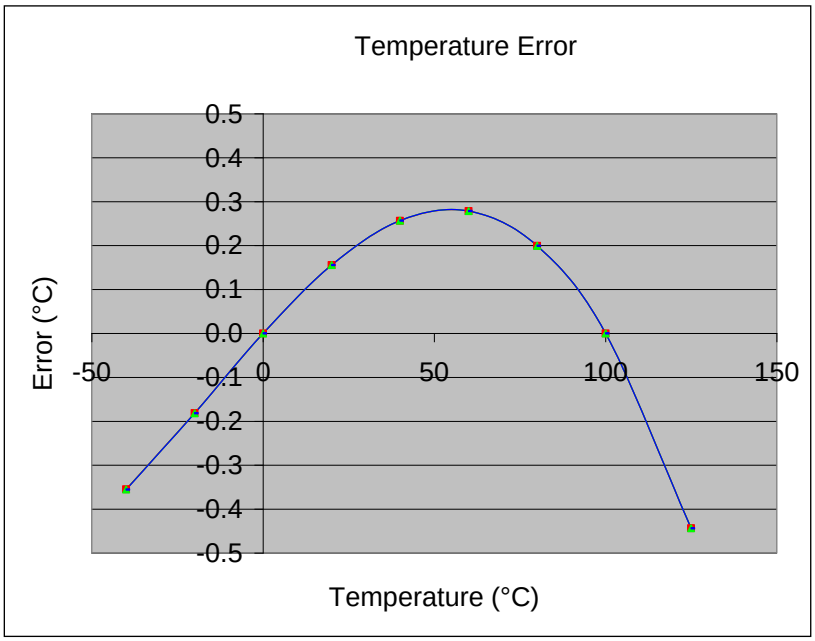

Figure 7. First Order Fit (Typical Part)

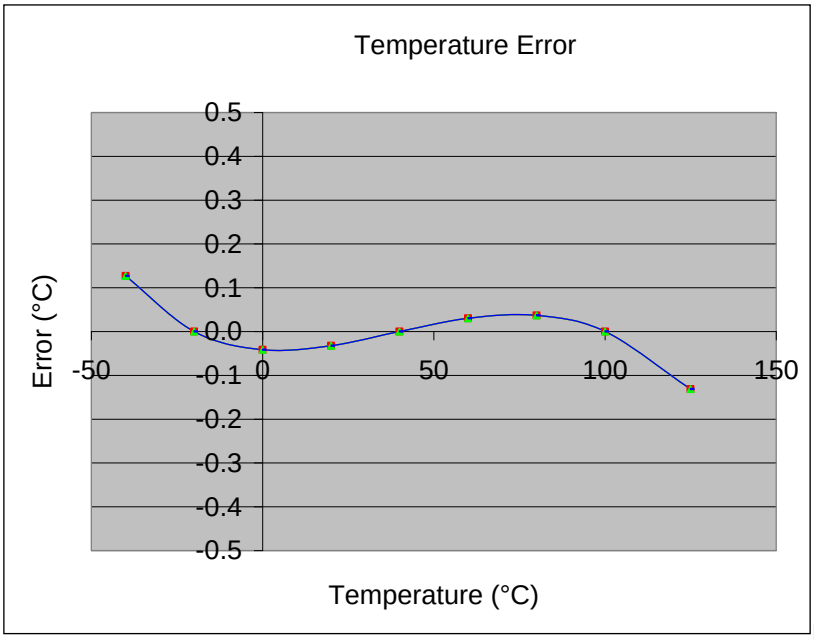

Figure 8. Second Order Fit (Typical Part)

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9. Circuit Description

9.1 Signal Flow and Block Diagram

As seen in the following figure, the ZSSC3123 comprises three main blocks: the analog core, digital core, and output communication. The capacitive input is first sampled by the analog core using a charge-balancing CDC and is adjusted for the appropriate capacitance range using the CDC_Offset, CDC_Reference, and CDC_Mult settings. The digital core corrects the digital sample with an on-chip digital signal processor (DSP), which uses coefficients stored in EEPROM for precise conditioning. An internal temperature sensor can be used to compensate for temperature effects of the capacitive input. A temperature value can also be calibrated and output as a 14-bit reading.

The corrected capacitance value can be read using four different output types, I2C, SPI, PDM, and alarms. They can all be directly interfaced with a microcontroller, and optional filtering of the PDM output can provide a ratiometric analog output. The alarm pins can also be used to control a variety of analog circuitry.

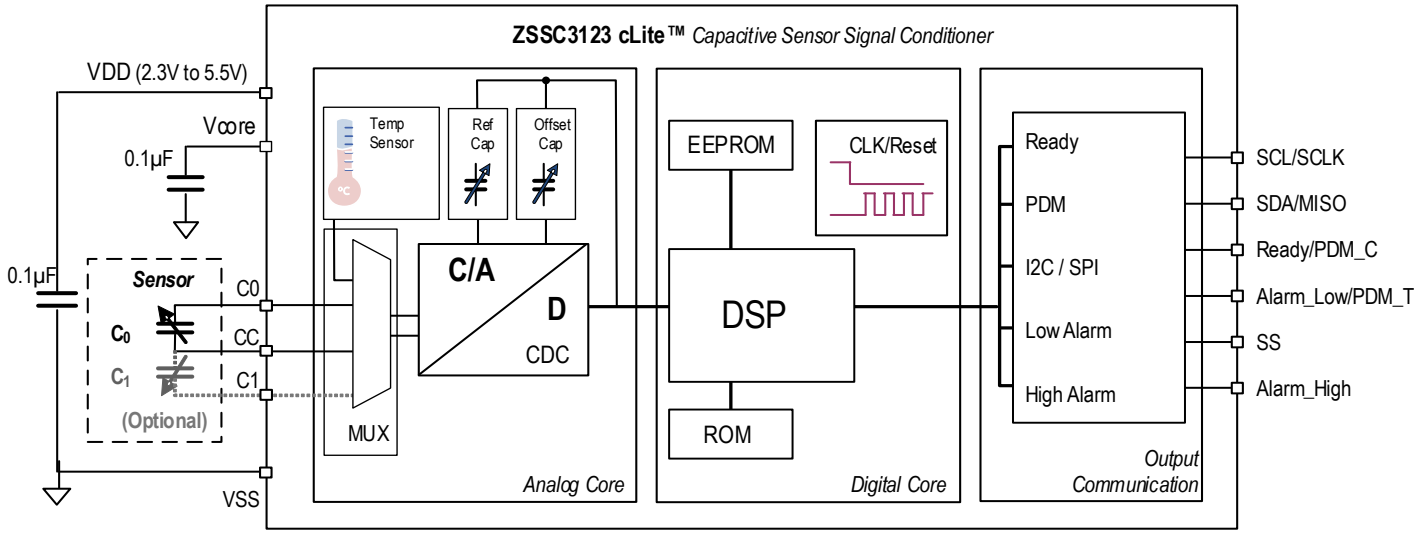

Figure 9. ZSSC3123 Block Diagram

9.2 Analog Front End

9.2.1 Capacitance-to-Digital Converter

A 1st-order charge-balancing capacitance-to-digital converter (CDC) is used to convert the input capacitance to the digital domain. The CDC uses a chopper-stabilized design to decrease any drift over temperature. The CDC interfaces to the sensor capacitor through the input multiplexer that controls whether the measurement is a capacitance or a temperature measurement. The input multiplexer also allows for two sensor capacitance configurations: a single-sensor capacitance or a two-sensor, ratio-based differential capacitance configuration, where the reference capacitor is part of the sensor.

As part of a switched-capacitor network, the reference capacitor C1 is driven by a square-wave voltage of the frequency f_{EXC} (see section 5). The sensor capacitance C0 is not exposed to DC voltages in order to prevent the aging effects of some sensor types. The configuration of the CDC is controlled by programming settings in EEPROM word *C_Config*. (See Table 30 for settings.)

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9.2.1.1 Single Ended

In the case of a single-sensor capacitor, the CDC output is proportional to the ratio of the sensor capacitor to an internal reference capacitor (C_{REF}). This internal reference capacitor value can be adjusted using the 3-bit trim CDC_Reference and a 2-bit range selection CDC_Mult (bit settings in Table 30). To optimize the measured end-resolution further, another internal capacitor (C_{OFF}) allows the subtraction of a defined offset capacitance using the 3-bit trim CDC_Offset (bit setting in Table 30). Equation 1 and Equation 2 describe the CDC output for a single sensor capacitance measurement. For C_{MULT}, use the multiplier in the "Total Capacitance Multiplier (C_{MULT})" column in Table 5. Select the values of CDC_Offset, and CDC_Reference by using the settings given in Table 6 to Table 9, depending on the Mult value. Note: Use the bit settings (0-7) and not the value in pF.

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_{REF}}$$ **Equation 1**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 2**

With

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF$$ **Equation 3**

And

$$C_{REF} = C_{MULT} * CDC\_Reference * 1pF$$ **Equation 4**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio, must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_{REF}	Reference capacitance
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30.
C_{MULT}	Capacitance range multiplier (see Table 5)
CDC_Offset	CDC offset trim setting (see section 9.2.1.4 and bit setting see Table 30
CDC_Reference	CDC reference setting (see section 9.2.1.4 and bit setting see Table 30)

9.2.1.2 Single Ended with External Reference

Some sensors include an external reference capacitor as part of the sensor construction. If the external reference capacitance (C_1) is constant or increases with increasing input sensor capacitance (C_0), then use CDC output Equation 5 through Equation 7. In this case, the CDC_Reference should be set to zero (bit setting in Table 30).

$$Z_{SENSOR} = \frac{(C_0 - C_{OFF})}{C_1}$$ **Equation 5**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 6**

$$C_{OFF} = C_{MULT} * CDC\_Offset * 1pF$$ **Equation 7**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio; must be in the range [0 to 1]
C_0	Input sensor capacitance
C_{OFF}	Zero shift of CDC
C_1	External reference capacitance
Z_{CDC}	Digital raw converted capacitance value

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Symbol	Description
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30)
C_{MULT}	Capacitance range multiplier (see Table 5)
CDC_Offset	CDC offset trim setting (see section 9.2.1.4 and Table 30)

9.2.1.3 Differential

A differential capacitive sensor includes two capacitors C_0 and C_1 that are captured as a ratio. The differential sensor is built so that the sensor input capacitance C_0 increases while the external reference capacitance C_1 decreases over the input signal range, but the total sum always remains constant. Equation 8 and Equation 9 describe the CDC output for a differential sensor capacitance measurement. The CDC_Reference and CDC_Offset capacitor trim bits must be set to zero, and the Differential bit must be set to one. (See Table 30 for bit numbers and settings). The Mult bits should be set so that the total capacitance (C_0 + C_1) falls in the corresponding capacitance range (see Table 5). The sum of C_0 and C_1 must not be larger than the selected Mult's maximum input range, except when CC is used as a decoupling capacitor.

In differential mode special sensor types can allow a non-galvanic connection with an external isolating capacitor C_{CC} between the sensor and the CC pin to avoid wear caused by mechanical moving parts.

$$Z_{SENSOR} = \frac{C_0}{(C_0 + C_1)}$$ **Equation 8**

$$Z_{CDC} = 2^{RES} * Z_{SENSOR}$$ **Equation 9**

Where:

Symbol	Description
Z_{SENSOR}	Measured sensor ratio; must be in the range [0 to 1]
C_0	Input sensor capacitance (moves in the opposite direction of C_1)
C_1	External reference capacitance (moves in the opposite direction of C_0)
Z_{CDC}	Digital raw converted capacitance value
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 30)

9.2.1.4 Capacitive Range Selection

Whether the application uses a single-ended or a differential sensor, the correct capacitance range as defined in Table 5 must be selected using the Mult bits, which are configured in the *C_Config* register (see Table 30). If using a single-ended sensor, then the minimum and maximum capacitance inputs should fall into the specified ranges. If using a differential sensor then the total capacitance (C_0 + C_1) must fall into this range. The Mult range affects the conversion time (see section 10.2).

Note: If the externally applied capacitance exceeds the configured capacitance range, the converted output signal can still show an apparently correct value, which is not valid. The limit is about 500% of the selected maximum input value. For example, for a capacitance setting of Mult1, CDC_Offset at zero, and CDC_Reference at 7, an input value above 117pF will give a non-saturated input value.

Table 5. CDC Multiplier

EEPROM Encoding (CDC_Mult)	Frequency Multiplier (Mult)	Reference Multiplier	Total Capacitance Multiplier (C_{MULT})	Capacitance Range (Full Scale Values)
00_{BIN}	1	1.44	1.44	2pF to 8pF
01_{BIN}	2	2.88	5.76	8pF to 32pF
10_{BIN}	4	5.76	23.04	32pF to 130pF
11_{BIN}	8	11.52	92.16	130pF to 260pF

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For single-ended sensors, use Table 6, Table 7, Table 8, and Table 9 as guidance for selecting appropriate values for the CDC (C_{OFF}) and (C_{REF}) for a particular capacitance input range. The CDC_Offset and CDC_Reference bits are found in EEPROM word C_Config. (Refer to Table 30 for bit numbers). Using the tables, the CDC input range can be adjusted to optimize the coverage of the sensor signal and offset values to give the maximum sensor span that can be processed without losing resolution. Choose a range by fitting the input sensor span within the narrowest range in the table, but note that these tables are only approximate, so the range should be chosen experimentally with the actual setup. Also note that since internal capacitance values can vary over process (see specification C_{tol} in Table 4), the minimum and maximum sensor span should be at least ±10% within the minimum and maximum of the chosen range respectively. Note: Take into consideration the effects of parasitics; if the parasitics for a particular Mult range exceed the parasitic to ground tolerance given in section 1, then the next Mult range should be considered since the CDC frequency is reduced by the Mult factor.

Note: A C_{REF} setting of 0 (marked with * in the following tables) is only supported with an external reference capacitor (C1) for single-ended sensors. C1 capacitance values should be within the defined range for each Mult setting.

Selection settings for C_{REF}, and C_{OFF}, and Mult are given in the following tables (capacitance ranges are nominal values).

Table 6. Mult 1: Sensor Capacitors Ranging from 2pF to 10pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	1.4	0.0	2.9	0.0	4.3	0.0	5.8	0.0	7.2	0.0	8.6	0.0	10.1
	1	1.4	C1	1.4	2.9	1.4	4.3	1.4	5.8	1.4	7.2	1.4	8.6	1.4	10.1	1.4	11.5
	2	2.9	C1	2.9	4.3	2.9	5.8	2.9	7.2	2.9	8.6	2.9	10.1	2.9	11.5		
	3	4.3	C1	4.3	5.8	4.3	7.2	4.3	8.6	4.3	10.1	4.3	11.5				
	4	5.8	C1	5.8	7.2	5.8	8.6	5.8	10.1	5.8	11.5						
	5	7.2	C1	7.2	8.6	7.2	10.1	7.2	11.5								
	6	8.6	C1	8.6	10.1	8.6	11.5										
	7	10.1	C1	10.1	11.5												

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not recommended

Table 7. Mult 2: Sensor Capacitors Ranging from 8pF to 32pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	5.8	0.0	11.5	0.0	17.3	0.0	23.0	0.0	28.8	0.0	34.6	0.0	40.3
	1	5.8	C1	5.8	11.5	5.8	17.3	5.8	23.0	5.8	28.8	5.8	34.6	5.8	40.3		
	2	11.5	C1	11.5	17.3	11.5	23.0	11.5	28.8	11.5	34.6	11.5	40.3				
	3	17.3	C1	17.3	23.0	17.3	28.8	17.3	34.6	17.3	40.3						
	4	23.0	C1	23.0	28.8	23.0	34.6	23.0	40.3								
	5	28.8	C1	28.8	34.6	28.8	40.3										
	6	34.6	C1	34.6	40.3												
	7																

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Table 8. Mult 4: Sensor Capacitors Ranging from 32pF to 130pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	23.0	0.0	46.1	0.0	69.1	0.0	92.2	0.0	115.2	0.0	138.2	0.0	161.3
	1	23.0	C1	23.0	46.1	23.0	69.1	23.0	92.2	23.0	115.2	23.0	138.2	23.0	161.3		
	2	46.1	C1	46.1	69.1	46.1	92.2	46.1	115.2	46.1	138.2	46.1	161.3				
	3	69.1	C1	69.1	92.2	69.1	115.2	69.1	138.2	69.1	161.3						
	4	92.2	C1	92.2	115.2	92.2	138.2	92.2	161.3								
	5	115.2	C1	115.2	138.2	115.2	161.3										
	6	138.2	C1	138.2	161.3												
	7																

PROHIBITED

not recommended

Table 9. Mult 8: Sensor Capacitors Ranging from 130pF to 260pF (Full Scale Values)

		CDC_Reference															
3-bit set		0*		1		2		3		4		5		6		7	
CDC_Offset	0	0.0	C1	0.0	92.2	0.0	184.3	0.0	276.5								
	1	92.2	C1	92.2	184.3	92.2	276.5										
	2	184.3	C1	184.3	276.5												
	3																
	4																
	5																
	6																
	7																

PROHIBITED

not recommended

9.2.2 Temperature Measurement

The temperature signal comes from an internal PTAT (proportional to absolute temperature) circuit that is a measure of the die temperature. The PTAT (VPTAT) voltage is used in the CDC to charge an internal capacitor (CT), while the bandgap voltage (VBG) is used to charge the offset and the reference trimmable capacitors. The CDC temperature output (ZTEMP) is defined by Equation 10 through Equation 13:

$$Z_{TEMP} = 2^{RES} * \frac{(V_{PTAT} / V_{BG}) * C_T - C_{TOFF}}{C_{TREF}} \quad \textbf{Equation 10}$$

With

$$C_T = 1.44 * Temp\_Trim * 1pF \quad \textbf{Equation 11}$$

With

$$C_{TOFF} = 1.44 * CDC\_Offset * 1pF \quad \textbf{Equation 12}$$

And

$$C_{TREF} = 1.44 * CDC\_Reference * 1pF \quad \textbf{Equation 13}$$

Where:

Symbol	Description
Z_{TEMP}	Measured internal temperature
RES	Programmable CDC resolution of 8, 10, 12, or 14 bits (bit setting in Table 31)
V_{PTAT}	Internal PTAT voltage
V_{BG}	Internal bandgap voltage

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Symbol	Description
C_T	Temperature measurement capacitor
C_{TOFF}	Temperature CDC zero shift
C_{TREF}	Temperature reference capacitance
Temp_Trim	Temperature trim setting (bit setting in Table 31)
CDC_Offset	CDC offset trim setting (bit setting in Table 31)
CDC_Reference	CDC reference setting (bit setting in Table 31)

Note: The factory settings for Temp_Trim, CDC_Offset, and CDC_Reference are optimized for the full temperature range of -40°C to 125°C guaranteeing a minimum effective resolution of 13 bits when 14 bits of resolution is selected. Unless a different temperature range is needed, it is strongly recommended that these settings not be changed.

9.3 Digital Core

The digital core provides control logic for the analog front-end, performs input signal conditioning, and handles external communication. A digital signal processor (DSP) is used for conditioning and correcting the converted sensor and temperature inputs. The DSP can correct for up to a two-region piece-wise non-linear sensor input, and up to a second-order non-linear temperature input. Alternatively a third-order correction of the sensor input for one region and up to a second-order, non-linear temperature input can be selected. Refer to section 13 for details on the signal conditioning and correction math. The analog front-end configuration and correction coefficients for both the capacitive sensor and the temperature sensor are stored in an on-chip EEPROM.

Four different types of outputs are available: I2C, SPI, PDM, and the Alarms. These output modes are used in combination with the two measurement modes: Update Mode and Sleep Mode. For a full description of normal operation in each mode, refer to section 10.

The ZSSC3123 has an internal 1.85MHz temperature-compensated oscillator that provides the time base for all operations. When VDD exceeds the POR level, the reset signal de-asserts and the clock generator starts. See section 10.1 for the subsequent power-on sequence. The exact clock frequency influences the measurement cycle time (see the frequency variation spec in section 5). To minimize the oscillator error as the VDD voltage changes, an on-chip regulator supplies the oscillator block.

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10. Normal Operation Mode

The following figure gives a general overview of ZSSC3123 operation. Details of operation, including the power-up sequence, measurement modes, output modes, diagnostics, and commands, are given in the subsequent sections.

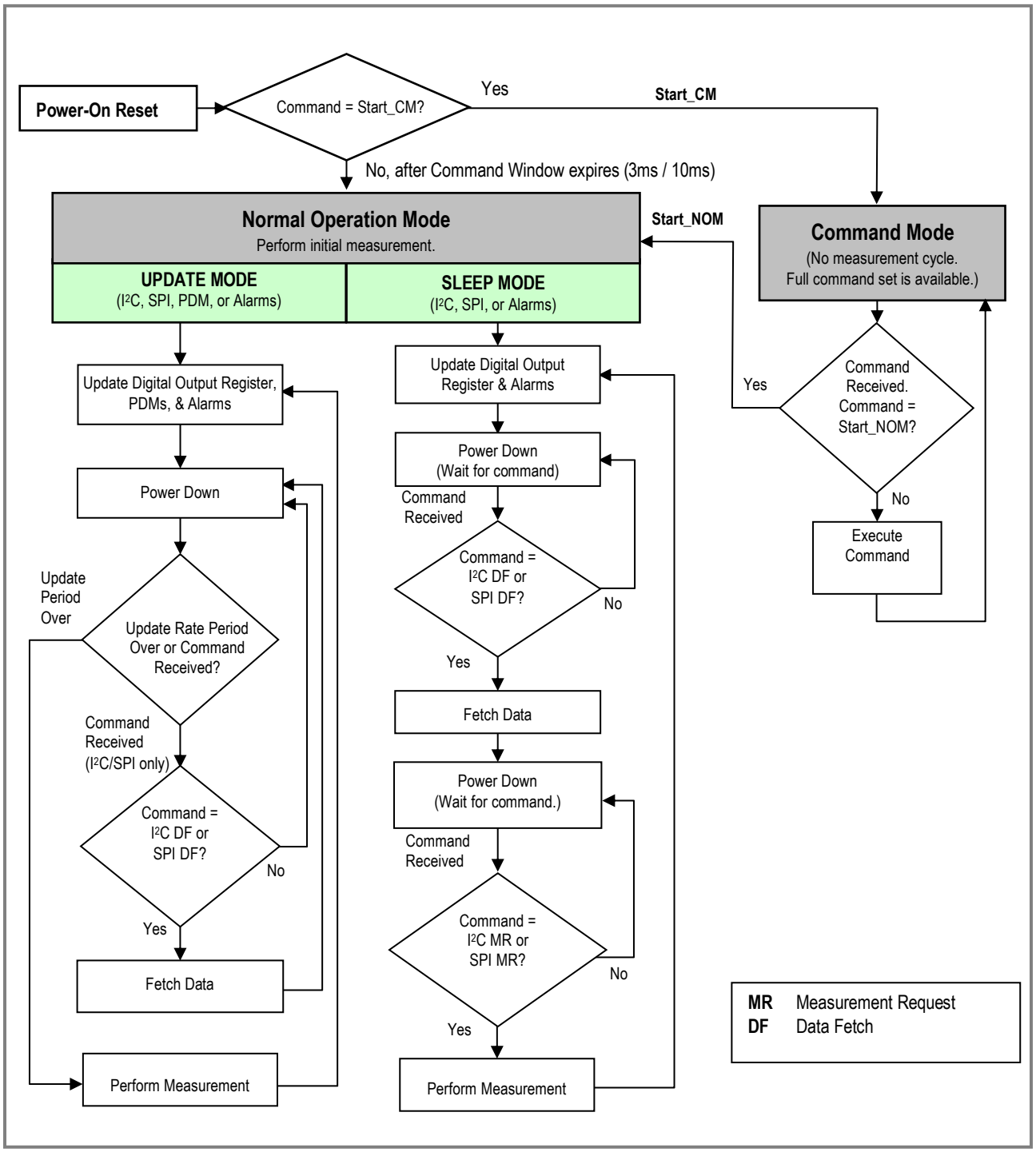

Figure 10. General Operation

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10.1 Power-On Sequence

The following figure shows the power-on sequence of the ZSSC3123. On system power-on reset (POR), the ZSSC3123 wakes as an I2C device regardless of the output protocol programmed in EEPROM. After power-on reset, the ZSSC3123 enters the command window. It then waits for a Start_CM command for 3ms if the Fast_Startup EEPROM bit is set or if the bit is not set, it waits10ms (see Table 32). If the ZSSC3123 receives the Start_CM command during the command window, it enters and remains in Command Mode. Command Mode is primarily used in the calibration environment. See section 11 for details.

If during the power-on sequence, the command window expires without receiving a Start_CM or if the part receives a Start_NOM command in Command Mode, the device will immediately assume its programmed output mode and will perform one complete measurement cycle. Timing for the initial measurement is described in section 10.2. At the end of the capacitance DSP calculation, the first data is written to the output register. Beyond this point, conversions are performed according to the programmed measurement mode settings (see section 11.3).

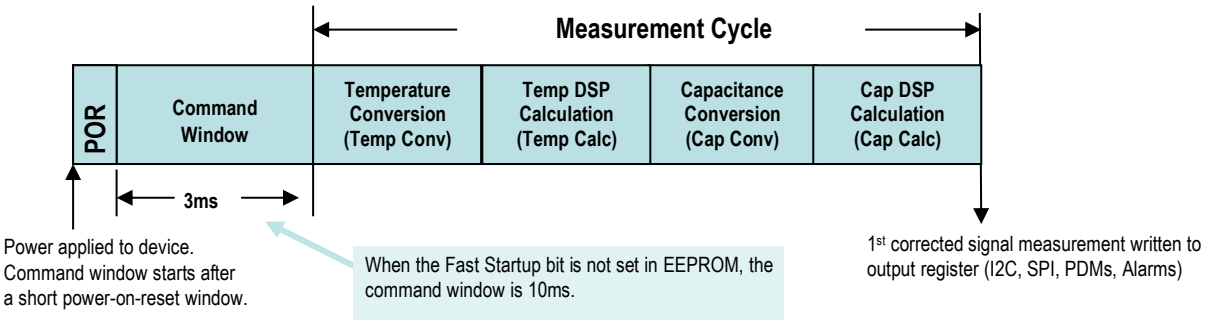

Figure 11. Power-On Sequence with Fast Startup Bit Set in EEPROM

Note: See section 10.2 for timing of the measurement cycle. Timing values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

10.2 Measurement Cycle

Figure 12 shows a typical measurement cycle. At the start of a measurement, there is a small wakeup period and then an internal temperature conversion/temperature DSP calculation is performed followed by a capacitance conversion/capacitance DSP calculation. The length of these conversions depends on the settings for the two Resolution bits in the C_Config and T_Config EEPROM words (refer to Table 10, Table 30, and Table 31). For capacitance measurements, conversion time also depends on the Mult selected by the CDC_Mult bits in C_Config (see Table 5 and Table 30). Each conversion cycle is followed by a DSP calculation, which uses the programmed calibration coefficients to calculate corrected temperature and capacitance measurements. In Update Mode, a temperature conversion is not performed every measurement cycle because it is considered a slower moving quantity. In this case, the measurement cycle timing is the same as in the figure without the temperature conversion/ temperature DSP calculation (see section 10.3.1 for more information).

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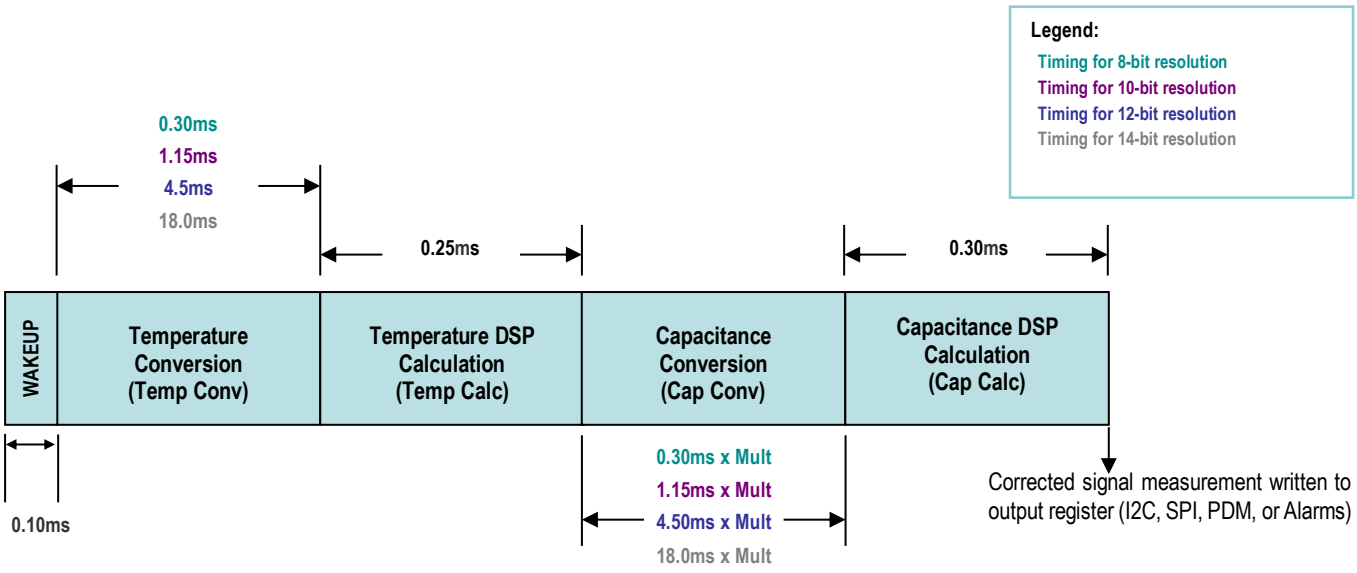

Figure 12. Measurement Cycle Timing

Table 10. CDC Resolution and Conversion Times

Resolution Bits in C_Config and T_Config Words	CDC Resolution (Bits)	Temperature Conversion Time[a] (ms)	Capacitance Conversion Time[a] (ms)
00_{BIN}	8	0.30	0.30 * Mult
01_{BIN}	10	1.15	1.15 * Mult
10_{BIN}	12	4.50	4.50 * Mult
11_{BIN}	14	18.0	18.0 * Mult

[a]All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

10.3 Measurement Modes

The ZSSC3123 can be programmed to operate in either Sleep Mode or Update Mode. The measurement mode is selected with the Measurement_Mode bit in the ZMDI_Config EEPROM word (see Table 29). In Update Mode, measurements are taken at a fixed, selectable rate (see section 10.3.1). In Sleep Mode, the part waits for commands from the master before taking measurements (refer to section 10.3.2).

Figure 10 shows the differences in operation between the two measurement modes.

10.3.1 Update Mode

In Update Mode, the digital core will perform conversions at an update rate selected with the Power_Down_Period bit field in the ZMDI_Config EEPROM word (see Table 29). Table 11 shows the power-down periods between conversions for the four Power_Down_Period settings. The benefit of slower update rates is power savings. Update Mode is compatible with all the different output modes; I2C, SPI, PDMs, and the Alarms. As shown in the following figure, at the completion of a measurement cycle, the digital output register, PDMs, and/or Alarms will be updated before powering down. When the power-down period expires, the ZSSC3123 will wake up and perform another measurement cycle. If the part is programmed for the fastest update rate, there is no power-down period, and measurements happen continuously.

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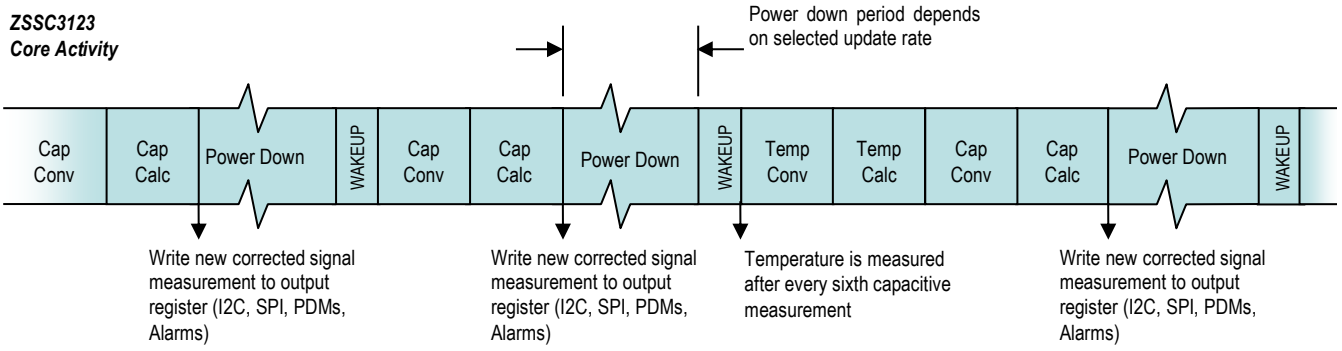
Table 11. Update Rate Settings (Power_Down_Period Bit Field in ZMDI_Config)

Note: All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

Power_Down_Period Setting	Power Down Period (ms)
00_{BIN}	0
01_{BIN}	5
10_{BIN}	25
11_{BIN}	125



Note: See section 10.2 for measurement cycle timing.

Figure 13. Measurement Sequence in Update Mode

To calculate the total time between capacitive measurements in Update Mode, add the measurement cycle timing from section 10.2 and the power down timing from Table 11. For example, typical settings might be a capacitance measurement resolution of 12-bits with a Mult of 1. In this example, the time between measurements = (4.5ms ∗ 1 + 0.1ms + 0.3ms) + (power down period). See Table 12 through Table 15 and

Figure 12 for the time between measurements for the different update rate settings and bit resolutions.

Temperature measurements are performed every six capacitive measurements. The actual frequency of temperature conversions varies with the update rate and AFE configuration settings. As shown in

Note: See section 10.2 for measurement cycle timing.

Figure 13, when a temperature measurement is performed, a capacitance measurement occurs immediately after, so the total measurement cycle time is increased by the length of the temperature conversion and temperature DSP calculation.

To calculate the total time between temperature measurements in Update Mode, take the time between capacitive measurements as calculated in the above text and multiply that number by six (there are six capacitive measurements to every temperature measurement) and then add the temperature conversion time/temperature DSP calculation time from Table 11 For example a temperature measurement with a resolution of 12-bits has a conversion time/DSP calculation time of 4.5ms +0.25ms (from Table 11) Continuing with the above example (12-bit capacitive measurement with a multiplier of 1) the time between temperature measurements is (capacitance update time * 6) + 4.75ms.

Table 12. Time Periods between Capacitance and Temperature Measurements for Mult1, Different Resolutions, and Update Rates

Mult1			Total Time between Capacitance Measurements (ms)			Total Time between Temperature Measurements (ms)		
CDC Res. (Bits)	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}
8	0.70	5.70	25.70	125.70	4.75	34.75	154.75	754.75

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10	1.55	6.55	26.55	126.55	10.70	40.70	160.70	760.70
12	4.90	9.90	29.90	129.90	34.15	64.15	184.15	784.15
14	18.40	23.40	43.40	143.40	128.65	158.65	278.65	878.65

Table 13. Time Periods between Capacitance and Temperature Measurements for Mult2, Different Resolutions, and Update Rates

Mult2			Total Time between Capacitance Measurements (ms)			Total Time between Temperature Measurements (ms)		
CDC Res. (Bits)	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}
8	1.00	6.00	26.00	126.00	6.55	36.55	156.55	756.55
10	2.70	7.70	27.70	127.70	17.60	47.60	167.60	767.60
12	9.40	14.40	34.40	134.40	61.15	91.15	211.15	811.15
14	36.40	41.40	61.40	161.40	236.65	266.65	386.65	986.65

Table 14. Time Periods between Capacitance and Temperature Measurements for Mult4, Different Resolutions, and Update Rates

Mult4			Total Time between Capacitance Measurements (ms)			Total Time between Temperature Measurements (ms)		
CDC Res. (Bits)	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}
8	1.60	6.60	26.60	126.60	10.15	40.15	160.15	760.15
10	5.00	10.00	30.00	130.00	31.40	61.40	181.40	781.40
12	18.40	23.40	43.40	143.40	115.15	145.15	265.15	865.15
14	72.40	77.40	97.40	197.40	452.65	482.65	602.65	1202.65

Table 15. Time Periods between Capacitance and Temperature Measurements for Mult8, Different Resolutions, and Update Rates

Mult8			Total Time between Capacitance Measurements (ms)			Total Time between Temperature Measurements (ms)		
CDC Res. (Bits)	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}	Update Rate 00_{BIN}	Update Rate 01_{BIN}	Update Rate 10_{BIN}	Update Rate 11_{BIN}
8	2.80	7.80	27.80	127.80	17.35	47.35	167.35	767.35
10	9.60	14.60	34.60	134.60	59.00	89.00	209.00	809.00
12	36.40	41.40	61.40	161.40	223.15	253.15	373.15	973.15
14	144.40	149.40	169.40	269.40	884.65	914.65	1034.65	1634.65

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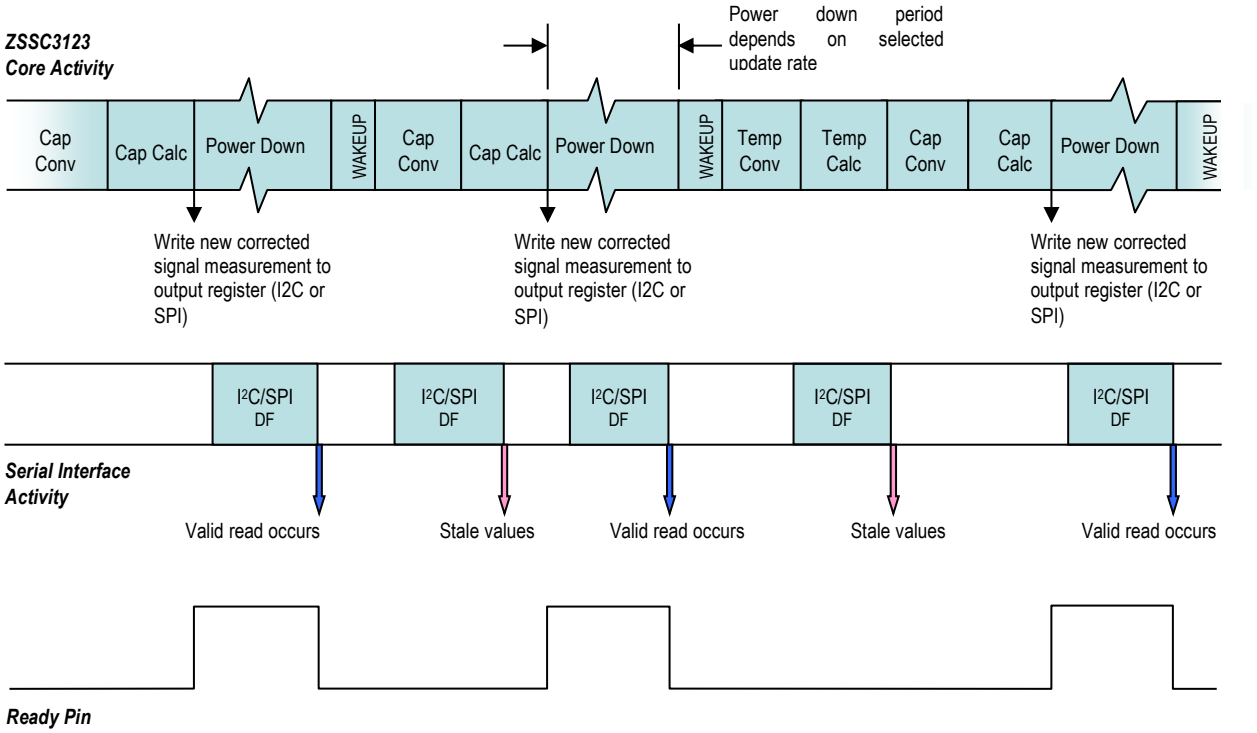
10.3.1.1 Data Fetch in Update Mode

In Update Mode, I2C and SPI are used to fetch data from the digital output register using a Data Fetch (DF) command (see section 10.6.3).

Detecting when data is ready to be fetched can be handled either by polling or by monitoring the Ready pin (see section 10.6.6 for details on the Ready pin). The status bits of a DF tell whether or not the data is valid or stale (see section 10.4 regarding the status bits). As shown in Figure 14 after a measurement cycle is complete, valid data can be fetched. If the next data fetch is performed too early, the data will be the same as the previous fetch with stale status bits. As shown in the figure, a rise on the Ready pin can also be used to tell when valid data is ready to be fetched.



Note: See section 10.2 for timing of measurements.

Figure 14. I2C and SPI Data Fetching in Update Mode

10.3.2 Sleep Mode

In Sleep Mode, the digital core will only perform conversions when the ZSSC3123 receives a Measurement Request command (MR); otherwise, the ZSSC3123 is always powered down. Measurement Request commands can only be sent using I2C or SPI, so PDM is not available. The Alarms can be used in Sleep Mode but only in combination with I2C or SPI. More details about MR commands in Sleep Mode operation can be found in section 10.3.2.1.

Note: Sleep Mode power consumption is significantly lower than Update Mode power consumption (see section 5 for exact values).

The following figure shows the measurement and communication sequence for Sleep Mode. The master sends an MR command to wake the ZSSC3123 from power down. After the ZSSC3123 wakes up, a measurement cycle is performed consisting of both a temperature and a capacitance conversion followed by the DSP correction calculations.

At the end of a measurement cycle, the digital output register and Alarms will be updated before powering down. An I2C or SPI data fetch (DF) is performed during the power-down period to fetch the data from the output register. In I2C the user can send another MR to start a new measurement cycle without fetching the previous data, but in SPI, a DF must be done before another MR can be sent. After the data has been fetched, the ZSSC3123 remains powered down until the master sends an MR command.

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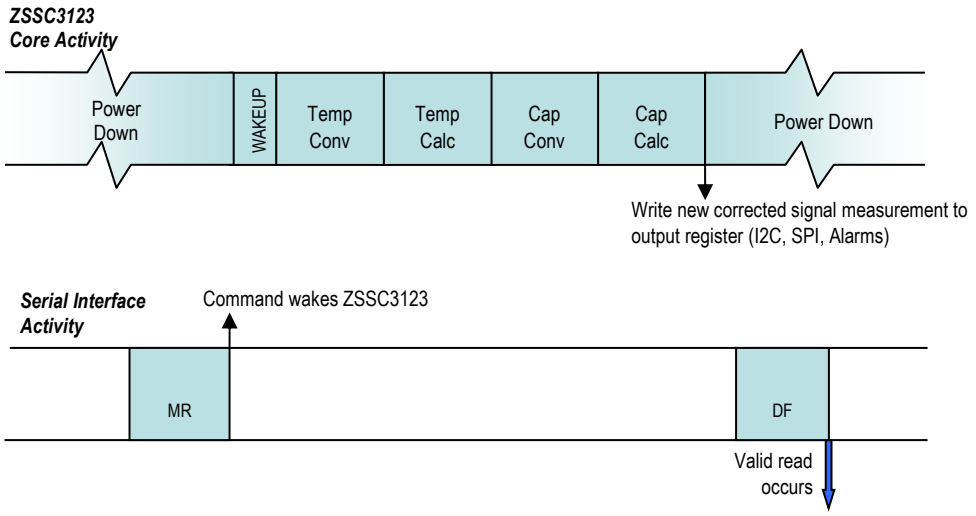

Note: See section 10.2 for timing of measurements.

Figure 15. Measurement Sequence in Sleep Mode (Only I2C, SPI, or Alarms)

10.3.2.1 Data Fetch in Sleep Mode

In Sleep Mode, I2C and SPI are used to request a measurement with a MR command and to fetch data from the digital output register using a Data Fetch (DF) command (see section 10.6.3).

As shown in the following figure, after a measurement cycle is complete, valid data can be fetched. The preferred method of detecting valid data is to wait for a rise on the Ready pin (see section 10.6.6 for details on the Ready pin). If the Ready pin is not available, the user must wait for the measurements to complete before performing the DF. The status bits of the DF can be used to tell whether the data is valid or stale (see section 10.4 regarding the status bits), but polling for the result must not be done before the time required for conversion has elapsed.

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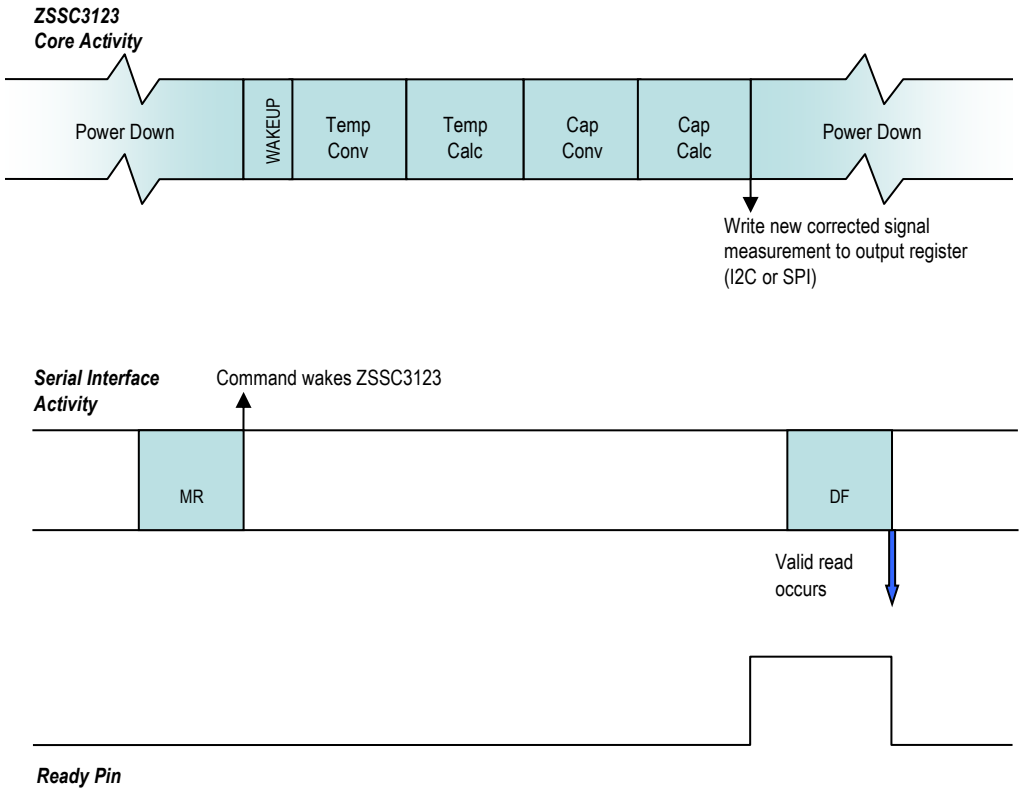

Note: See section 10.2 for timing of measurements.

Figure 16. I2C and SPI Data Fetching in Sleep Mode

10.4 Status and Diagnostics

Status bits (the two MSBs of the fetched high data byte; see Table 16) are provided in I2C and SPI but not in PDM. The status bits are used to indicate the current state of the fetched data. Diagnostic detection is available in I2C, SPI, and PDM. In I2C and SPI diagnostics are reported as a saturated high capacitance and temperature output (see Table 16). In PDM, diagnostics are reported as a railed high output level for both PDM_C (capacitive PDM) and PDM_T (temperature PDM). If a diagnostic value is reported then one or more of the errors shown in Table 18 occurred in normal operation.

Configuration EEPROM diagnostics are detected at initial power-up of the ZSSC3123 or a wakeup in Sleep Mode and are permanent diagnostics. All other diagnostics are detected during a measurement cycle and reported in the subsequent data fetch for I2C or SPI or in an output register update for PDM.

Table 16. Status Bit Definitions

Status Bits (I2C or SPI)	PDM Output	Definition
00_{BIN}	Clipped normal output	Valid data: Data that has not been fetched since the last measurement cycle.
01_{BIN}	Not applicable	Stale data: Data that has already been fetched since the last measurement cycle. **Note**: If a data fetch is performed before or during the first measurement after power-on reset, then “Stale data” will be returned, but this data is actually invalid since the first measurement has not been completed.

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Status Bits (I2C or SPI)	PDM Output	Definition
10_{BIN}	Not applicable	Command Mode: The ZSSC3123 is in Command Mode.
11_{BIN}	Not used	Not used

Table 17. Diagnostic Detection

I2C or SPI Output	PDM Output	Definition
Saturated output $3FFF_{HEX}$	High output (railed) level	A diagnostic fault has occurred in normal operation (see the following table).

Table 18. Normal Operation Diagnostic Table

Diagnostic	Type	Definition
Configuration Error	Permanent	An EEPROM or RAM parity error occurred in the initial loading of the configuration registers.
RAM Parity Error	Transient	A RAM parity error occurred during a microcontroller instruction in the last measurement cycle.
EEPROM Error	Transient	A double-bit error detection (DED) EEPROM error occurred in the last measurement cycle (see section 10.4.1).
Math Warning	Transient	An internal math overflow has occurred in the last measurement cycle and the output might be invalid.

10.4.1 EEPROM Error Detection and Correction

The contents of the EEPROM are protected via error checking and correction (ECC). Each of the 32 16-bit words contains 6 parity bits enabling single-bit error correction (SEC) and double-bit error detection (DED) per word. In Command Mode both SEC and DED errors are reported in the response byte (see section 11.3). If the fetched EEPROM data has a DED error, then the fetched data will be incorrect; however, if a SEC error was reported then the fetched data has been corrected, and it is the user's choice to write the data back to attempt to correct the error. During Normal Operation Mode, a diagnostic will be flagged on any DED error, but an SEC error will be automatically corrected and not flagged as a diagnostic.

10.4.2 Alarm Diagnostics

The alarm outputs do not report diagnostics. If diagnostics are needed with alarm outputs, then either digital or PDM outputs must also be used.

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10.5 Output Modes

The ZSSC3123 has four different output modes as shown in the following table. See the corresponding reference sections for specifics on each mode.

Table 19. Output Modes

Output Mode	Reference Sections
I2C	Section 10.6
Read only SPI	
PDM	Section 10.7
Alarms	Section 10.8

As illustrated in the pin configuration in section 1, the output communication modes share pins. The Output_Selection bits in EEPROM word ZMDI_Config (see section 12.1) select which of these outputs will be enabled. The following table shows the pin configuration for the different output selections.

Table 20. Pin Assignment for Output Selections

Pin	Output Selection			
	I2C (001_{BIN})	SPI (011_{BIN})	PDM_C (100_{BIN})	PDM_C+T (110_{BIN})
Pin 8	Alarm_Low	Alarm_Low	Alarm_Low	PDM_T
Pin 9	Alarm_High	Alarm_High	Alarm_High	Alarm_High
Pin 10	Ready	Ready	PDM_C	PDM_C
Pin 12	SDA	MISO	SDA	SDA
Pin 13	SCL	SCLK	SCL	SCL
Pin 14	No input	SS	No input	No Input

10.6 I2C and SPI

Two-wire I2C and three-wire read-only SPI are available for fetching data from the ZSSC3123. I2C is used to send calibration commands to the ZSSC3123. To choose I2C or SPI, set the corresponding Output_Selection bits in the EEPROM word ZMDI_Config.

10.6.1 I2C Features and Timing

The ZSSC3123 uses an I2C-compatible communication protocol[1] with support for 100kHz and 400kHz bit rates. The ZSSC3123 I2C slave address (00_{HEX} to $7F_{HEX}$) is selected by the Device_ID bits in the *Cust_Config* EEPROM word (see Table 32 for bit assignments). The device will respond only to this address if the communication lock is set by programming 011_{BIN} in the Comm_lock bits in the *ZMDI_Config* EEPROM word (see Table 29 for bit assignments); otherwise, the device will respond to all I2C addresses. The factory setting for the I2C slave address is 28_{HEX} with Comm_lock set.

See

[1] For details, refer to the current version of the I2C specification available at https://www.nxp.com/docs/en/user-guide/UM10204.pdf?fsrch=1&sr=2&pageNum=1 or other websites for this specification.

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Figure 17 for the I2C timing diagram, and see Table 21 for the definitions of the parameters shown in the diagram.

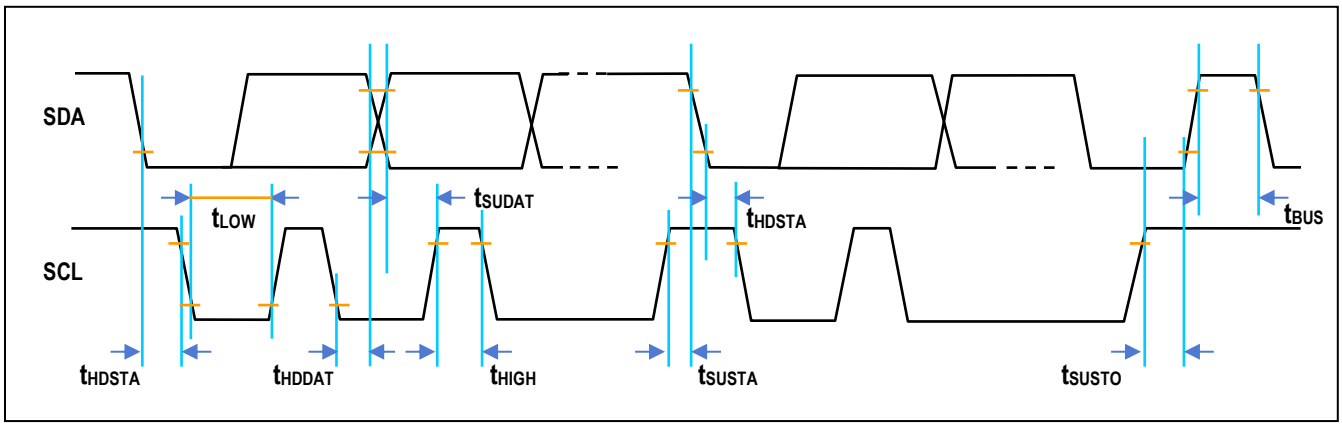

Figure 17. I2C Timing Diagram

Table 21. I2C Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCL clock frequency[a]	f_{SCL}	20		400	kHz
Start condition hold time relative to SCL edge	t_{HDSTA}	0.1			µs
Minimum SCL clock low width[b]	t_{LOW}	0.6			µs
Minimum SCL clock high width[b]	t_{HIGH}	0.6			µs
Start condition setup time relative to SCL edge	t_{SUSTA}	0.1			µs
Data hold time on SDA relative to SCL edge	t_{HDDAT}	0		0.5	µs
Data setup time on SDA relative to SCL edge	t_{SUDAT}	0.1			µs
Stop condition setup time on SCL	t_{SUSTO}	0.1			µs
Bus free time between stop condition and start condition	t_{BUS}	1			µs

[a]The min. frequency of 20kHz applies to calibration/test only (required to meet Command Window timing). There is no minimum for NOM.
[b]Combined low and high widths must equal or exceed the minimum SCL period.

10.6.2 SPI Features and Timing

SPI is available only as half duplex (read-only from the ZSSC3123). SPI speeds of up to 800kHz can be supported. The SPI interface can be programmed to allow the master to sample MISO on the falling-edge or rising-edge of SCL via the SPI_Phase bit in EEPROM word *Cust_Config* (see Table 32 for bit assignments). See the following figure for the SPI timing diagram and the following table for definitions of the parameters shown in the timing diagram.

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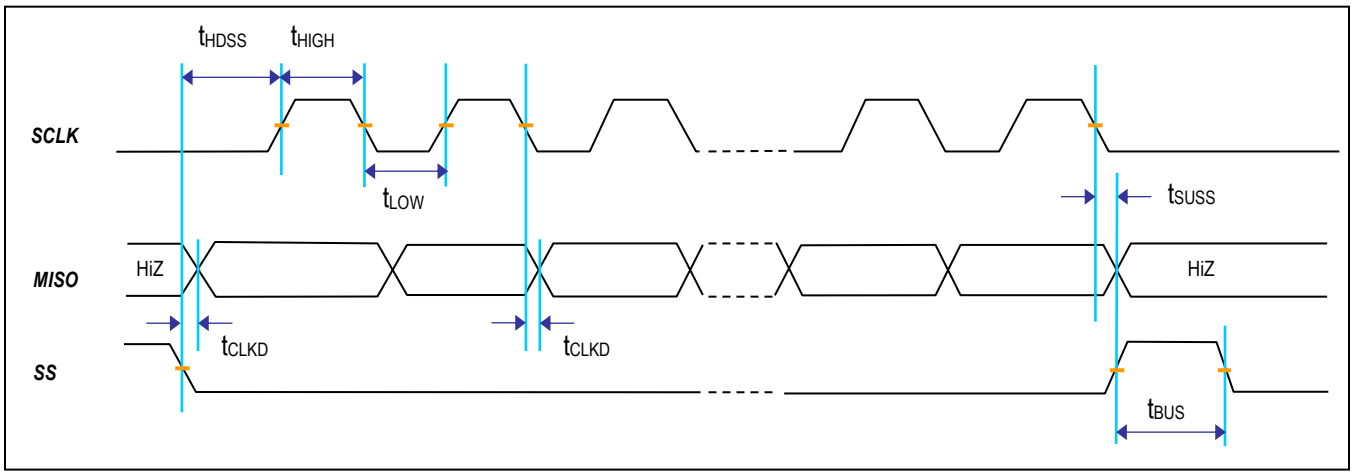

Figure 18. SPI Timing Diagram

Table 22. SPI Parameters

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SCLK clock frequency	f_{SCL}	50		800	kHz
SS drop to first clock edge	t_{HDSS}	2.5			µs
Minimum SCLK clock low width[a]	t_{LOW}	0.6			µs
Minimum SCLK clock high width[a]	t_{HIGH}	0.6			µs
Clock edge to data transition	t_{CLKD}	0		0.5	µs
Rise of SS relative to last clock edge	t_{SUSS}	0.1			µs
Bus free time between rise and fall of SS	t_{BUS}	2			µs

[a]Combined low and high widths must equal or exceed minimum SCLK period.

10.6.3 I2C and SPI Commands

As detailed in Table 23, there are three types of commands that allow the user to interface with the ZSSC3123 in the I2C or SPI modes.

Table 23. I2C and SPI Command Types

Type	Description	Communication Supported	Reference Sections
Data Fetch (DF)	Used to fetch data in any digital mode	I2C and SPI	Section 10.6.4
Measurement Request (MR)	Used to start measurements in Sleep Mode	I2C and SPI	Section 10.6.5
Calibration Commands	Used in Command Mode during the calibration process	I2C Only	Section 11.2

10.6.4 Data Fetch (DF)

The Data Fetch (DF) command is used to fetch data in any digital output mode. With the start of communication (for I2C after reading the slave address; for SPI at the falling edge of SS), the entire output packet will be loaded in a serial output register. The register will be updated after the communication is finished. The output is always scaled to 14 bits independent of the programmed resolution. The ordering of the bits is big-endian.

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10.6.4.1 I2C Data Fetch

An I2C Data Fetch command starts with the 7-bit slave address and the 8th bit = 1 (READ). As the slave, the ZSSC3123 sends an acknowledge (ACK) indicating success. The number of data bytes returned by the ZSSC3123 is determined by when the master sends the NACK and stop condition. The following figure shows examples of fetching two and three bytes respectively. The full 14 bits of capacitive data are fetched in the first two bytes. The MSBs of the first byte are the status bits.

If temperature data is needed, additional temperature bytes can be fetched. As illustrated in

Figure 19, the three-byte data fetch returns 1 byte of temperature data (8-bit accuracy) after the capacitive data. A fourth byte can be fetched where the six MSBs of the fetched byte are the six LSBs of a 14-bit temperature measurement. The last two bits of the fourth byte are undetermined and should be masked off in the application.

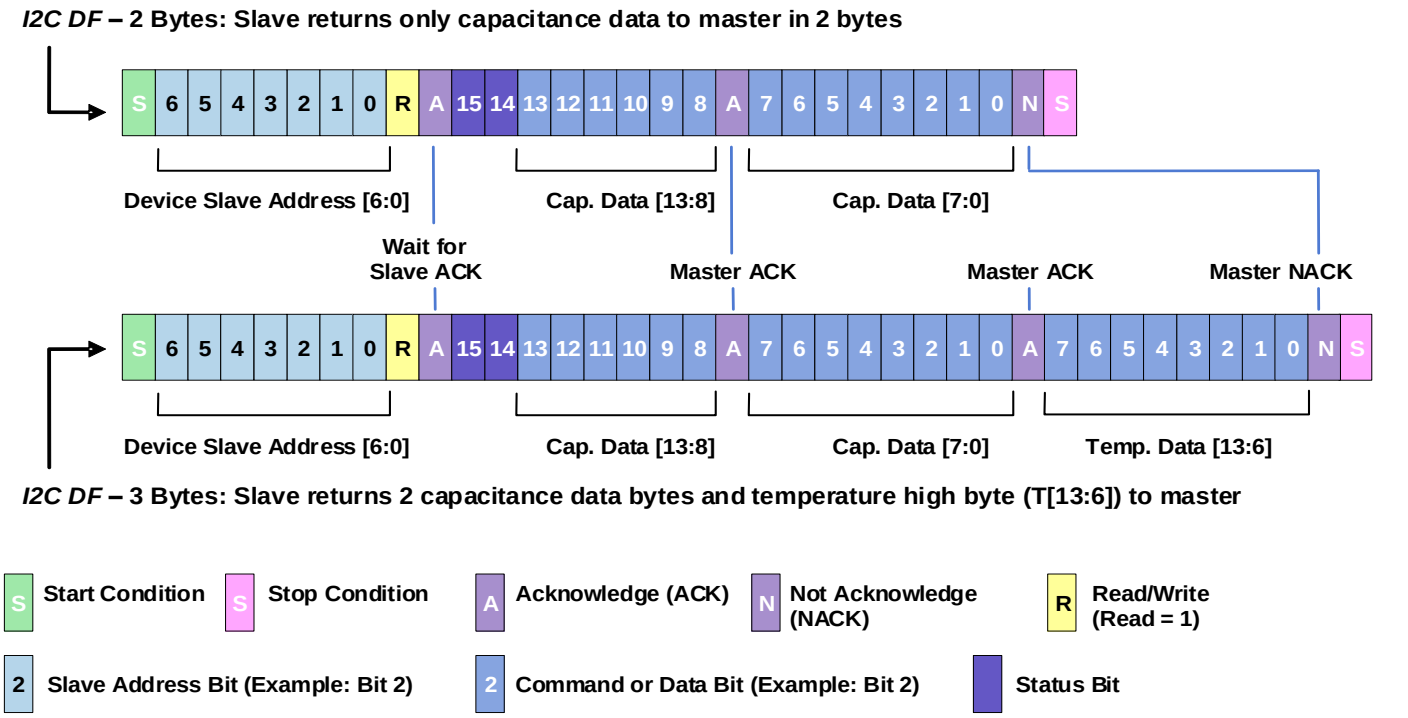

Figure 19. I2C Measurement Packet Reads

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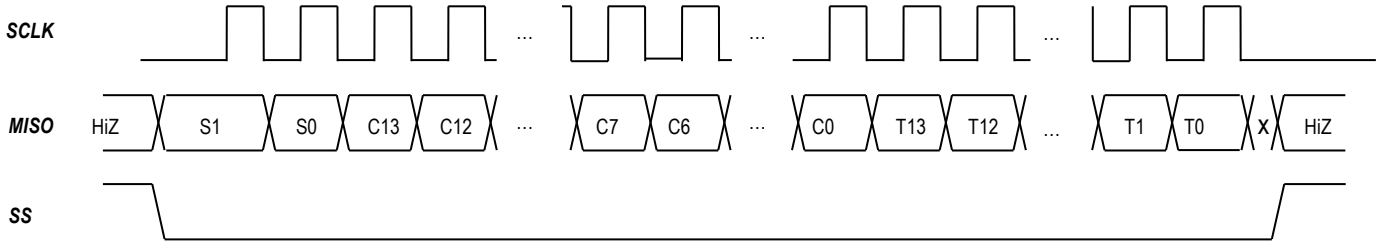
10.6.4.2 SPI Data Fetch

By default, the SPI interface will have data change after the falling edge of SCLK. The master should sample MISO on the rising (opposite) edge of SCLK. This is configurable via the SPI_Phase bit in the EEPROM word Cust_Config (see Table 32 for bit assignments). The SPI protocol can handle high and low polarity of the clock line without a configuration change.

As displayed in the following figure, the entire output packet is 4 bytes (32 bits). The high capacitive data byte comes first, followed by the low byte. Then 14 bits of corrected temperature (T[13:0]) are sent: first the T[13:6] byte and then the {T[5:0],xx} byte. The last 2 bits of the final byte are undetermined and should be masked off in the application. If the user only requires the corrected capacitance value, the read can be terminated after the 2nd byte. If the corrected temperature is also required but only at an 8-bit resolution, the read can be terminated after the 3rd byte is read.



Packet = [{S(1:0),C(13:8)}, {C(7:0)}, {T(13:6)},{T(5:0),xx}]

Where

S(1:0) = Status bits for the packet (normal, command, busy, diagnostic)

C(13:8) = Upper 6 bits of the 14-bit capacitance data

C(7:0) = Lower 8 bits of the 14-bit capacitance data

T(13:6) = Corrected temperature data (if application does not require corrected temperature, terminate read early)

T(5:0),xx =. Remaining bits of corrected temperature data for full 14-bit resolution

HiZ = High impedance

Figure 20. SPI Output Packet with Positive Edge Sampling

10.6.5 Measurement Request (MR)

A measurement request (MR) is a Sleep-Mode-only command sent by the master to wake up the ZSSC3123 and start a new measurement cycle in both I2C and SPI modes. See section 10.3.2 for more information on Sleep Mode.

10.6.5.1 I2C Measurement Request

The I2C MR is used to wake up the device in Sleep Mode and start a complete measurement cycle starting with a temperature measurement, followed by a capacitance measurement, followed by the DSP calculations, and then the results are written to the digital output register. As shown in

Figure 21, the communication contains only the slave address and the WRITE bit (0) sent by the master. After the ZSSC3123 responds with the slave ACK, the master creates a stop condition.

Note: The I2C MR function can also be accomplished by sending “don’t care” data after the address instead of immediately sending a stop bit.

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I2C MR– Measurement Request: Slave starts a measurement cycle

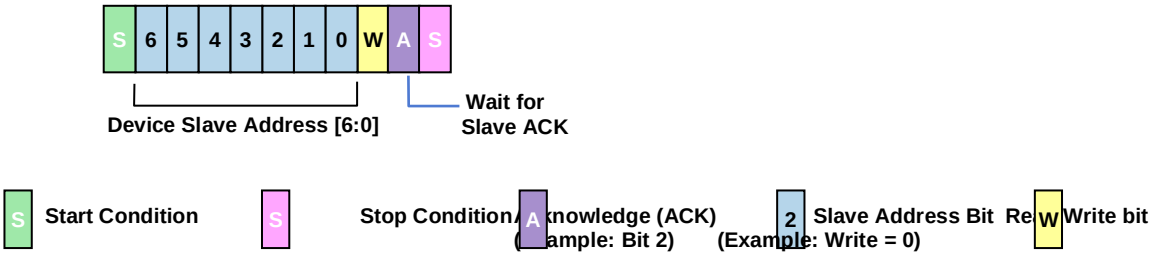

Figure 21. I2C MR

10.6.5.2 SPI Measurement Request

The SPI measurement request (SPI MR) is used to wake the device in Sleep Mode and then start a complete measurement cycle, starting with the temperature measurement / temperature DSP calculation, followed by the capacitance measurement / capacitance DSP calculations, and then the results are written to the digital output register. As shown in

Figure 22, executing an SPI MR command is a read of 8 bits, ignoring the data that is returned.

Note: The SPI MR function can also be accomplished by performing a full SPI Data Fetch (see section 10.6.4.2) and ignoring the invalid data that will be returned.

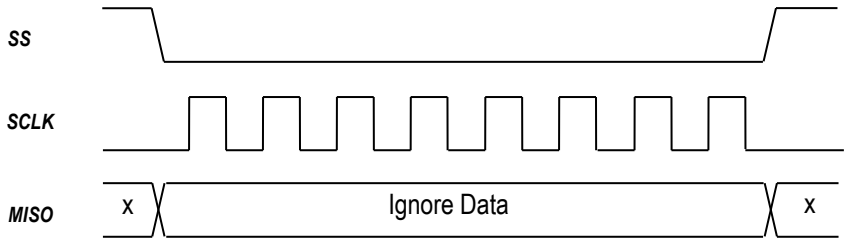

Figure 22. SPI MR

10.6.6 Ready Pin

A rise on the Ready pin indicates that new data is ready to be fetched from either the I2C or SPI interface. The Ready pin stays high until a Data Fetch (DF) command is sent (see section 10.6.3); it stays high even if additional measurements are performed before the DF. In Sleep Mode, sending a Measurement Request (MR) command resets the Ready pin.

The Ready pin's output driver type is selectable as either full push-pull or open drain via the Ready_Open_Drain bit in EEPROM word Cust_Config (see Table 32 for bit assignments and settings). Point-to-point communication typically uses the full push-pull driver. If an application requires interfacing to multiple parts, then the open-drain option can allow for just one wire and one pull-up resistor to connect all the parts in a bus format.

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10.7 Pulse Density Modulation (PDM)

PDM outputs for both corrected capacitance and temperature are provided on the ZSSC3123. PDM_C (capacitance PDM) appears on the READY/PDM_C pin, and PDM_T (temperature PDM) appears on the ALARM_LOW/PDM_T pin if enabled using the Output_Selection bits (see Table 29). The PDM frequency is 231.25kHz ±10% (i.e., the oscillator frequency 1.85MHz ±10% divided by 8). Both PDM signals are 14-bit values. In PDM Mode, the ZSSC3123 must be programmed to Update Mode (see section 10.3.1). Every time a conversion cycle has finished, the PDM will begin outputting the new value.

An analog output value is created by low-pass filtering the output; a simple first-order RC filter will work in this application. Select the time constant of the filter based on the requirements for settling time and/or peak-to-peak ripple.

Important: The resistor of the RC filter must be ≥10kΩ.

The following table shows some filter examples using a 10kΩ resistor.

Table 24. Low Pass Filter Example for R = 10kΩ

Filter Capacitance (nF)	PDM_C		Desired Analog Output Resolution
	VPP Ripple (mV/V)	0 to 90% Settling Time (ms)	
100	4.3	2.3	8
400	1.0	9.2	10
1600	0.3	36.8	12
6400	0.1	147.2	14

For a different (higher) resistor, the normalized ripple VPP[mV/V] can be calculated as:

$$VPP[mV/V] = \frac{4324}{(R[k\Omega] * C[nF])}$$ **Equation 14**

or the settling time t_{SETT} for a 0% to 90% settling can be calculated as:

$$t_{SETT}[ms] = 0.0023 * R[k\Omega] * C[nF]$$ **Equation 15**

The ZSSC3123 provides high and low clipping limits for the PDM output. EEPROM words PDM_Clip_High and PDM_Clip_Low (EEPROM registers 16_{HEX} and 17_{HEX}; see Table 28) are the 14-bit high and low clipping limit registers respectively. The 14-bit values map directly to the output of the IC and can be calculated as:

$$PDM\_Clip = ROUND(\frac{2^{14} * clip\_level\_\%}{100})$$ **Equation 16**

These registers apply to both PDM_C and PDM_T. Since diagnostics are reported via the PDM_C or PDM_T pin (see section 10.4), clipping limits allow diagnostics to be differentiated from the normal output. For detection of the diagnostic signal, a PDM_Clip_High limit of 97.5% ($3E66_{HEX}$) or lower is recommended.

Important: The default values for the high and low clipping limits (00_{HEX}) are not compatible with PDM output, so the clipping limits must be changed if the PDM output is used. Otherwise, the PDM output will not function as expected. If the PDM output is not used, it is important to retain the default values of 00_{HEX} for the clipping limits.

10.8 Alarm Output

The alarm output can be used to monitor whether a corrected capacitance reading has exceeded or fallen below pre-programmed values. The alarm can be used to drive an open-drain load connected to VDD, as demonstrated in section 14.2, or it can function as a full push-pull driver. If a high voltage application is required, external devices can be controlled with the Alarm pins, as demonstrated in section 14.3.

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The two alarm outputs can be used at the same time, and these alarms can be used in combination with any of the other three modes; I2C, SPI, or PDM.

Note: When both PMD_C and PDM_T are selected, only Alarm_High is available (see section 10.5).

The alarm outputs are updated when a conversion cycle is completed. The alarm outputs can be used in both Update Mode and Sleep Mode, but if Sleep Mode is used, I2C or SPI must also be used to control the measurements (see section 10.3).

10.8.1 Alarm Registers

Four registers are associated with the alarm functions: Alarm_High_On, Alarm_High_Off, Alarm_Low_On, and Alarm_Low_Off (see Table 28 for EEPROM addresses). Each of these four registers is a 14-bit value that determines where the alarms turn on or off. The two high alarm registers form the output with hysteresis for the Alarm_High pin, and the two low alarm registers form the output with hysteresis for the Alarm_Low pin. Each of the two alarm pins can be configured independently using Alarm_Low_Cfg and Alarm_High_Cfg located in EEPROM word Cust_Config (see Table 32 for bit assignments).

Note: If two high alarms or two low alarms are needed, see section 10.8.4.

10.8.2 Alarm Operation

As shown in the following figure, the Alarm_High_On register determines where the high alarm trip point is and the Alarm_High_Off register determines where the high alarm turns off if the high alarm has been activated. The high alarm hysteresis value is equal to Alarm_High_On – Alarm_High_Off. The same is true for the low alarm where Alarm_Low_On is the low alarm trip point with Alarm_Low_Off determining the alarm shut off point. The low alarm hysteresis value is equal to Alarm_Low_Off – Alarm_Low_On.

Figure 24 shows the output operation flowcharts for both the Alarm_High and Alarm_Low pins.

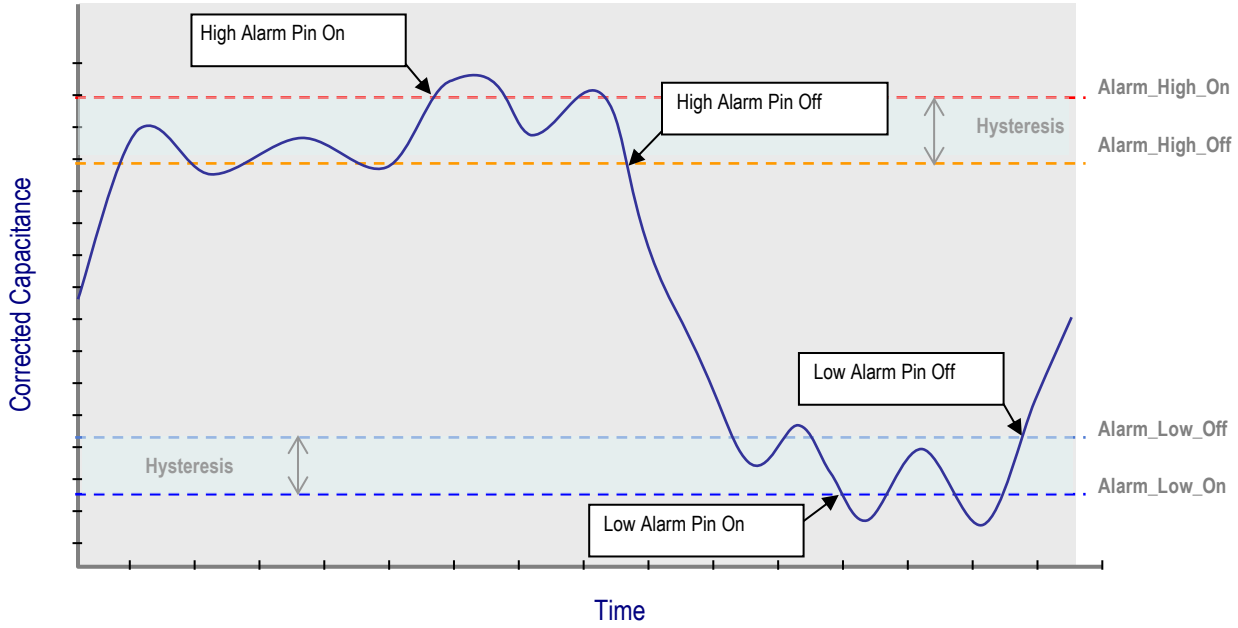

Figure 23. Example of Alarm Function

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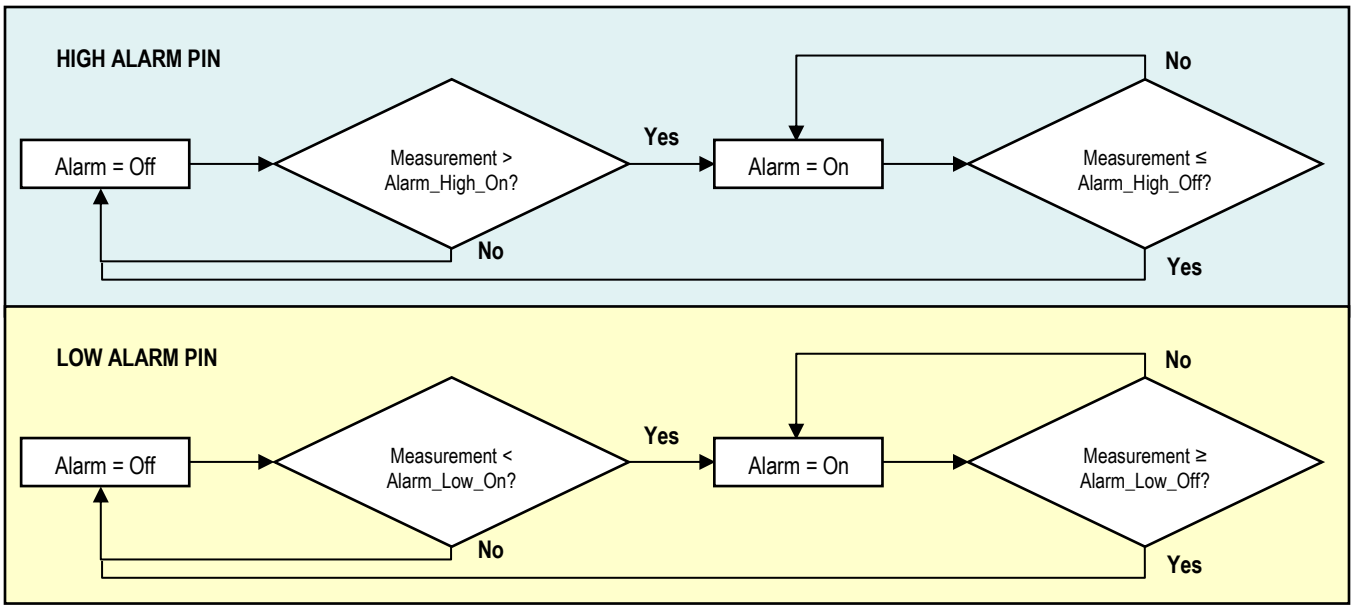

Figure 24. Alarm Output Flow Chart

10.8.3 Alarm Output Configuration

The user can select the output driver configuration for each alarm using the Output Configuration bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 32 for bit assignments). For applications, such as interfacing with a microcontroller or controlling an external device (as seen in section 14.3), select the full push-pull driver for the alarm output type. For an application that directly drives a load connected to VDD, as demonstrated in section 14.2, the typical selection is the open-drain output type.

An advantage of making an alarm output open drain is that in a system with multiple devices, the alarm outputs of each ZSSC3123 can be connected together with a single pull-up resistance so that one can detect an alarm on any device with a single wire.

10.8.4 Alarm Polarity

For both alarm pins, the polarity of the alarm output is selected using the Alarm Polarity bit in the Alarm_High_Cfg and Alarm_Low_Cfg registers in EEPROM word Cust_Config (see Table 32 for bit assignments). As shown in the example in section 14.3, the alarms can be used to drive a high voltage humidity control system. Since the humidifier or dehumidifier relays must be on when the alarms are on, the alarm polarity bits are set to 0 (active high). In the example given in section 14.2, an alarm is used to turn on an LED in an open drain configuration. In order for the LED to be on when the alarm is on, the output must be low, so the alarm polarity bit is set to 1 (active low).

Another feature of the polarity bits is the ability to create two high alarms or two low alarms. For example, with applications requiring two high alarms, flip the polarity bit of the Alarm_Low pin, and it will act as a high alarm. However, in this case, the effect of the alarm low registers is also changed: the Alarm_Low_On register would act like the Alarm_High_Off register and the Alarm_Low_Off register would act like the Alarm_High_On register. The same can be done to achieve two low alarms: the Alarm_High pin would have the polarity bit flipped, and the two Alarm_High registers would have opposite meanings.

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11. Command Mode

The Command Mode is primarily used for calibrating the ZSSC3123. Command Mode is entered by sending a Start_CM during the command window (see section 3.1 for more details on how to enter Command Mode). In Command Mode, a set of commands is available to the user to calibrate the part (see Table 25).

11.1 Command Format

Command Mode commands are only supported for the I2C protocol. As shown in the following figure, commands are 4-byte packets with the first byte being a 7-bit slave address followed by 0 for the write operation. The second byte is the command byte and the last two bytes form a 16-bit data field.

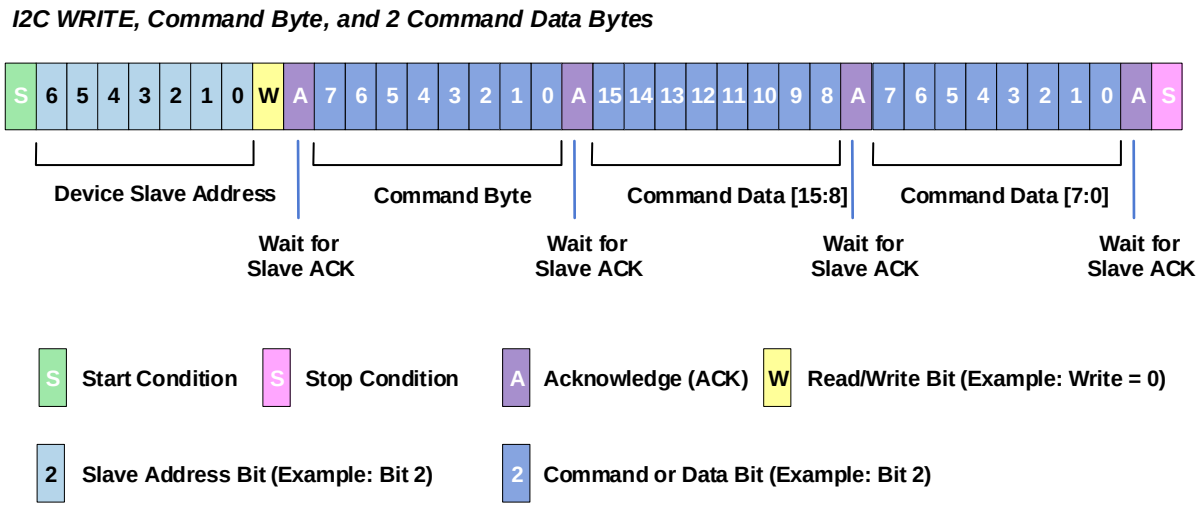

Figure 25. I2C Command Format

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11.2 Command Encodings

The following table describes all the commands that are offered in Command Mode.

Note: Only the commands listed in the following table are valid. Other encodings might cause unpredictable results. If data is not needed for the command, zeros must be supplied as data to complete the 4-byte packet.

Table 25. Command List and Encodings

Command Byte 8 Command Bits (HEX)	Third and Fourth Bytes 16 Data Bits (HEX)	Description	Response Time [a]
00_{HEX} to $1F_{HEX}$	0000_{HEX}	EEPROM Read of addresses 00_{HEX} to $1F_{HEX}$ After this command has been sent and executed, a data fetch must be performed (see section 10.6.4).	100µs
40_{HEX} to $5F_{HEX}$	$YYYY_{HEX}$ (Y = data)	Write to EEPROM addresses 00_{HEX} to $1F_{HEX}$ The 2 bytes of data sent will be written to the address specified in the 6 LSBs of the command byte.	12ms
80_{HEX}	0000_{HEX}	Start_NOM Ends Command Mode and transitions to Normal Operation Mode.	Length of initial conversions depends on temperature and capacitance resolution set-tings and the capacitance “mult” setting (for details, see section 10)
$A0_{HEX}$	0000_{HEX}	Start_CM Start Command Mode: used to enter the command interpreting mode. Start_CM is only valid during the power-on Command Window (see section 10.1).	100µs
$B0_{HEX}$	0000_{HEX}	Get Revision Get the revision of the part. After this command has been sent and executed, a data fetch must be performed (see section 10.6.4).	100µs

[a]All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

11.3 Command Response and Data Fetch

After a command has been sent and the execution time defined in Table 25 has expired, an I2C Data Fetch (DF) can be performed to fetch the response. As shown in

Figure 26, after the slave address has been sent, the first byte fetched is the response byte. The upper two status bits will always be 10_{BIN} to represent Command Mode (see section 10.4). The lower two bits are the response bits. Table 26 describes the different responses that can be fetched.

To determine if a command has finished executing, poll the part until a Busy response is no longer received. The middle four bits of the response byte are command diagnostic bits where each bit represents a different diagnostic (see Table 27). For more information on EEPROM errors, see section 10.4.1.

Note: Regardless of what the response bits are, one or more of the diagnostic bits might be set, indicating an error occurred during the execution of the command.

Note: Only one command can be executed at a time. After a command is sent, another command must not be sent until the execution time of the first command defined in Table 25 has expired.

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For all commands except EEPROM Read and Get Revision, the data fetch should be terminated after the response byte is read. If the command was a Get Revision, then the user will fetch the one-byte Revision value as shown in

Figure 26, example 2. The revision is coded with the upper nibble being the letter corresponding to a full layer change and the lower nibble being the metal change number, for example A0. If the command was an EEPROM Read, then the user will fetch two more bytes as shown in

Figure 26, example 3. If a Corrected EEPROM Error diagnostic was flagged after an EEPROM read, the user has the option to write this data back to attempt to fix the error.

Instead of polling to determine if a command has finished executing, the user can use the Ready pin. In this case, wait for the Ready pin to rise, which indicates that the command has executed. Then a data fetch can be performed to get the response and data (see

Figure 26). See section 10.6.6 for more information on the Ready pin.

Table 26. Response Bits

Encoding	Name	Description
00_{BIN}	Busy	The command is busy executing.
01_{BIN}	Positive Acknowledge	The command executed successfully.
10_{BIN}	Negative Acknowledge	The command was not recognized or an EEPROM write was attempted while the EEPROM was locked.

Table 27. Command Diagnostic Bits

Bit Position	Name	Description
2	Corrected EEPROM Error	A corrected EEPROM error occurred during execution of the last command.
3	Uncorrectable EEPROM Error	An uncorrectable EEPROM error during execution of the last command.
4	RAM Parity Error	A RAM parity error occurred during a microcontroller instruction in the execution of the last command.
5	Configuration Error	An EEPROM or RAM parity error occurred in the initial loading of the configuration registers.

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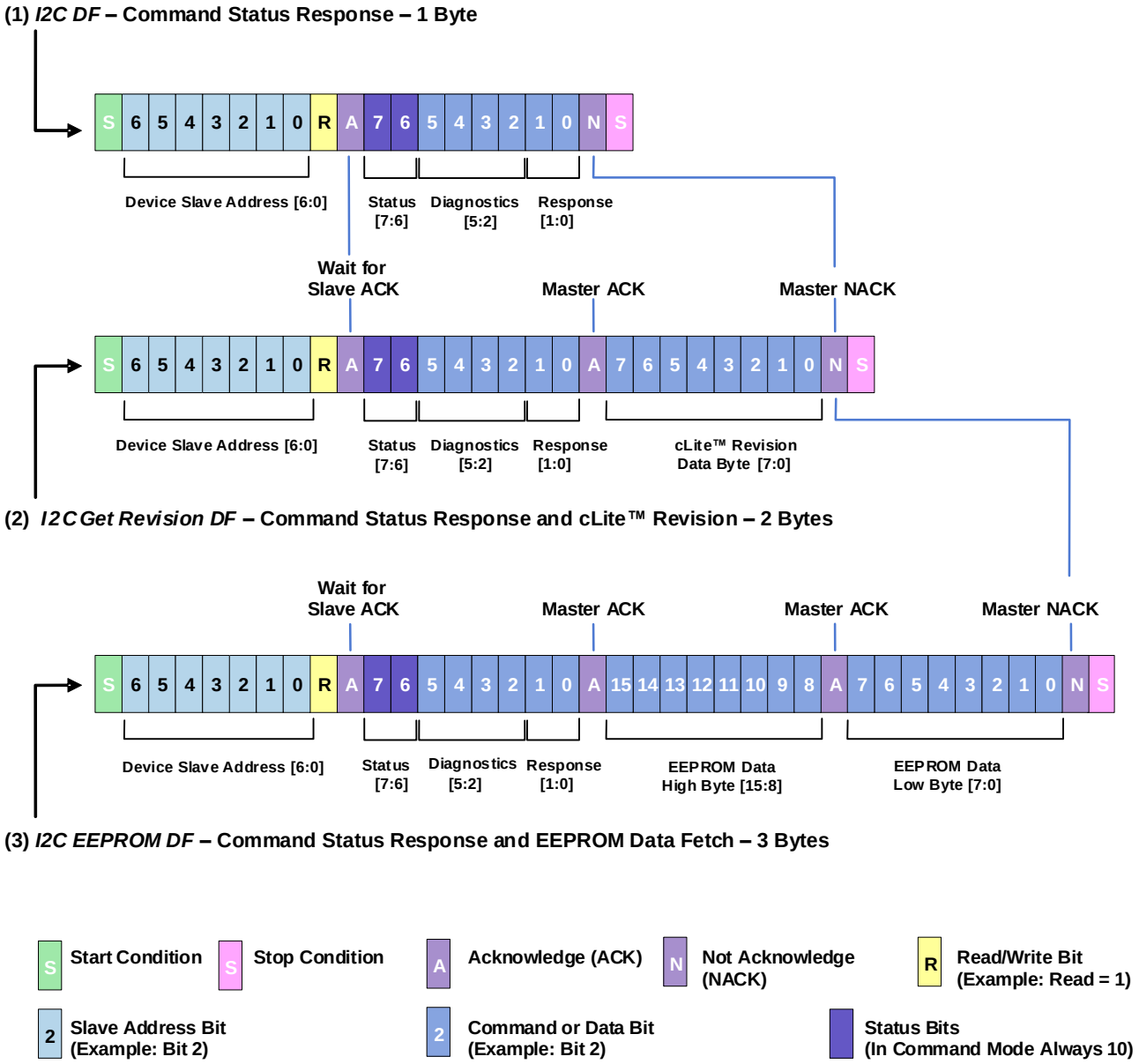

Figure 26. Command Mode Data Fetch

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12. EEPROM

The EEPROM array contains the calibration coefficients for gain and offset, etc., and the configuration bits for the analog front-end, output modes, measurement modes, etc. The ZSSC3123 EEPROM is arranged as 32 16-bit words (see Table 28). The EEPROM is divided into two sections. Words 0_{HEX} to 15_{HEX} can only be written to if the EEPROM is unlocked. After the EEPROM is locked, these locations can no longer be written to. The EEPROM lock bits are in the ZMDI_Config register (see Table 28 for the bit assignment). Words 16_{HEX} to $1F_{HEX}$ (highlighted blue in Table 28) are always unlocked and available for writing to at all times. See section 11 for instructions on reading and writing to the EEPROM in Command Mode via the I2C interface. When programming the EEPROM, an internal charge pump voltage is used; therefore a high voltage supply is not needed.

Note: If the EEPROM was accidentally locked, it can be unlocked with the following instructions (see section 11 for how to send commands).

1. Enter Command Mode with a Start_CM command.
2. Send an $A2_{HEX}$ for the command byte and 0000_{HEX} for the command data.
3. Send an $F0_{HEX}$ for the command byte and 0021_{HEX} for the command data.
4. Clear the EEPROM_Lock bits in the *ZMDI_Config* register with an EEPROM Write command.
5. Reset the part.

There are four Customer_ID words available for customer use, two in the locked region and two in the unlocked region. They can be used as a customer serial number for module traceability. (See the following table for Customer_ID EEPROM addresses.) The integrity of the contents of the EEPROM array is ensured via ECC (see section 10.4.1).

The following table provides a summary of the EEPROM contents. The configuration register bits are explained in detail in the following subsections.

Table 28. EEPROM Word Assignments

Note: See important notes at the end of the table.

EEPROM Word	Bit Range	IC Default	Name	Description and Notes
00_{HEX}	15:0	$XXXX_{HEX}$	Cust_ID0	Customer ID byte 0: For use by customer (default value is the upper 16 bits of the lot number)
01_{HEX}	15:0	$XXXX_{HEX}$ ($LLLLLLLL_B$ $0000ssss_B$)	Cust_ID1	Customer ID byte 1: For use by customer (default value is the lower 8 bits of the lot number and an 8 bit wafer number)
02_{HEX}	15:0	$0B00_{HEX}$	ZMDI_Config	Renesas configuration register (see section 12.1)
03_{HEX}	15:0	0006_{HEX}	Not Available	**Do Not Change**; must leave at factory settings
04_{HEX}	15:0	$00FT_{HEX}$	Not Available	**Do Not Change**; must leave at factory settings [a]
05_{HEX}	15:0	0000_{HEX}	Not Available	**Do Not Change**; must leave at factory settings
06_{HEX}	15:0	$0C06_{HEX}$	C_Config	AFE capacitance configuration register (see Table 30)
07_{HEX}	15:0	0000_{HEX}	SOT_tco	2nd order temperature offset correction for capacitance
08_{HEX}	15:0	0000_{HEX}	Tco	Temperature offset correction for capacitance
09_{HEX}	15:0	0000_{HEX}	SOT_tcg	2nd order temperature gain correction for capacitance
$0A_{HEX}$	15:0	0000_{HEX}	Tcg	Temperature gain correction for capacitance
$0B_{HEX}$	15:0	0000_{HEX}	Offset	Offset correction for capacitance
$0C_{HEX}$	15:0	2000_{HEX}	Gain_1	Gain correction for capacitance (region 1)
$0D_{HEX}$	15:0	0000_{HEX}	SOT_1	2nd order correction for capacitance (region 1)
$0E_{HEX}$	15:0	2000_{HEX}	Gain_2	Gain correction for capacitance (region 2)
$0F_{HEX}$	15:0	0000_{HEX}	SOT_2 Or TOT_1	2nd order correction for capacitance (region 2); alternatively 3rd order correction (only one region)

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EEPROM Word	Bit Range	IC Default	Name	Description and Notes
10_{HEX}	15:0	$7FFF_{HEX}$	Raw_Break	Break point dividing region 1 from region 2
11_{HEX}	15:0	$8D92_{HEX}$	T_Config	AFE temperature configuration register (see Table 31)
12_{HEX}	15:0	0000_{HEX}	Offset_T	Offset correction for temperature
13_{HEX}	15:0	2000_{HEX}	Gain_T	Gain correction for temperature
14_{HEX}	15:0	0000_{HEX}	SOT_T	2nd order correction for temperature
15_{HEX}	15:0	0000_{HEX}	TREF	Raw temperature reading reference point
16_{HEX}	13:0	0000_{HEX}	PDM_Clip_High	PDM high clipping limit (keep at zero unless PDM is enabled; must change default if PDM is used)
17_{HEX}	13:0	0000_{HEX}	PDM_Clip_Low	PDM low clipping limit (keep at zero unless PDM is enabled; may be changed if PDM is used)
18_{HEX}	13:0	$3FFF_{HEX}$	Alarm_High_On	High alarm on trip point
19_{HEX}	13:0	$3FFF_{HEX}$	Alarm_High_Off	High alarm off trip point
$1A_{HEX}$	13:0	0000_{HEX}	Alarm_Low_On	Low alarm on trip point
$1B_{HEX}$	13:0	0000_{HEX}	Alarm_Low_Off	Low alarm off trip point
$1C_{HEX}$	15:0	0028_{HEX}	Cust_Config	Customer configuration register (see section 12.4)
$1D_{HEX}$	15:0	0000_{HEX}	Not Available	**Do Not Change**; must leave at factory settings
$1E_{HEX}$	15:0	$XXXX_{HEX}$	Cust_ID2	Customer ID byte 2; for use by customer (default value is the 8-bit x and 8-bit y coordinates on the wafer)
$1F_{HEX}$	15:0	0000_{HEX}	Cust_ID3	Customer ID byte 3; for use by customer

[a]The T in the default setting for EEPROM word 04_{HEX} represents the custom trim value determined by final test. Do not change this setting.

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12.1 Renesas Configuration Register (ZMDI_Config, EEPROM Word 02_{HEX})

This register is loaded at power-on reset and upon exiting Command Mode using a Start_NOM command.

Table 29. ZMDI_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
0	0_{BIN}	Measurement_Mode	0 = Update Mode 1 = Sleep Mode
2:1	00_{BIN}	Power_Down_Period	Power Down Period: [a] 00_{BIN} = 0ms 01_{BIN} = 5ms 10_{BIN} = 25ms 11_{BIN} = 125ms
3	0_{BIN}	Scale_Sot_Tc	Scales the SOT TC Terms: 0 = Scale × 1 1 = Scale × 2
4	0_{BIN}	Gain4x_C	Multiply Gain_1 and Gain_2 by 0 = multiply by 1 1 = multiply by 4
7:5	000_{BIN}	EEPROM_lock	011_{BIN} = locked All other = unlocked When EEPROM is locked, the internal charge pump is disabled and the EEPROM can no longer be programmed. Note: If the EEPROM was accidentally locked, see section 12 for instructions for unlocking it.
10:8	011_{BIN}	Comm_lock	011_{BIN} = locked All other = unlocked When communication is locked, I2C communication will only respond to its programmed address; otherwise if communication is unlocked, I2C will respond to any address.
13:11	001_{BIN}	Output_Selection	001_{BIN} = I2C 011_{BIN} = SPI 100_{BIN} = PDM Capacitance (+ 2 alarms) 110_{BIN} = PDM Capacitance + Temperature (+ 1 alarm) All other configurations are not allowed See Table 20 for more details.
14	0_{BIN}	Third_order	0 = Piece-wise linear calibration with breakpoint 1 = Third-order calibration
15	0_{BIN}	Not Available	**Do Not Change** – must leave at factory settings

[a]All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

12.2 Capacitance Analog Front-End Configuration (C_Config, EEPROM Word 06_{HEX})

This register is loaded immediately before a capacitance measurement is taken, so a power cycle is not needed for changes to take effect.

Table 30. C_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
2:0	110_{BIN}	CDC_Reference	CDC reference capacitor selection (see Table 6 to Table 9)

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Bit Range	IC Default	Name	Description and Notes
5:3	000_{BIN}	CDC_Offset	CDC offset capacitor selection (see Table 6 to Table 9)
9:6	0000_{BIN}	Not Available	**Do Not Change** – must leave at factory settings
11:10	11_{BIN}	Resolution	CDC resolution and sample rate: [a] 00_{BIN} = 8 bits at 0.7ms rate 01_{BIN} = 10 bits at 1.6ms rate 10_{BIN} = 12 bits at 5.0ms rate 11_{BIN} = 14 bits at 18.5ms rate
13:12	00_{BIN}	CDC_Mult	CDC Multiplier: 00_{BIN} = 1 (2pF to 8pF) 01_{BIN} = 2 (8pF to 32pF) 10_{BIN} = 4 (32pF to 130pF) 11_{BIN} = 8 (130pF to 260pF)
14	0_{BIN}	Differential	Differential input capacitance selection: 0 = Single-ended 1 = Differential
15	0_{BIN}	Not Available	**Do Not Change** – must leave at factory settings

[a]All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%). See section 10.2 for additional timing factors.

12.3 Temperature Analog Front End Configuration (T_Config, EEPROM Word 11_{HEX})

This register is loaded immediately before a capacitance measurement is taken, so a power cycle is not needed for changes to take effect.

Table 31. T_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
2:0	010_{BIN}	CDC_Reference	CDC reference capacitor selection. The factory settings are set for a full-span temperature range from -40°C to +125°C. Note: Do not change this setting from the factory setting unless a different temperature range is needed.
5:3	010_{BIN}	CDC_Offset	CDC offset capacitor selection. The factory settings are set for a full-span temperature range from -40°C to +125°C. Note: Do not change this setting from the factory setting unless a different temperature range is needed.
8:6	110_{BIN}	Temp_Trim	Trim setting used for the temperature measurement. The factory settings are set for a full-span temperature range from -40°C to +125°C. Note: Do not change this setting from the factory setting unless a different temperature range is needed.
9	0_{BIN}	Not Available	**Do Not Change** – must leave at factory settings
11:10	11_{BIN}	Resolution	Temperature resolution and sample rate: [a] 00_{BIN} = 8 bits at 0.7ms rate 01_{BIN} = 10 bits at 1.6ms rate 10_{BIN} = 12 bits at 5.0ms rate 11_{BIN} = 14 bits at 18.5ms rate
15:12	1000_{BIN}	Not Available	**Do Not Change** – must leave at factory settings

[a]All time values shown are typical; for the worst case values, multiply by 1.1 (nominal frequency ±10%).

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12.4 Customer Configuration Register (Cust_Config, EEPROM Word $1C_{HEX}$)

This register is loaded at power-on reset and upon exiting Command Mode after receiving a Start_NOM command.

Table 32. Cust_Config Bit Assignments

Bit Range	IC Default	Name	Description and Notes
6:0	0101000_{BIN}	Device_ID	I2C slave address
8:7	00_{BIN}	Alarm_Low_Cfg	Configure the Alarm_Low output pin: **Bits** – **Description** 7 – Alarm Polarity: 0 = Active High, 1 = Active Low 8 – Output Configuration: 0 = Full push-pull, 1 = Open-drain
10:9	00_{BIN}	Alarm_High_Cfg	Configure the Alarm_High output pin: **Bits** – **Description** 9 – Alarm Polarity: 0 = Active High, 1 = Active Low 10 – Output Configuration: 0 = Full push-pull, 1 = Open drain
11	0_{BIN}	SPI_Phase	The edge of SCLK that the master samples MISO on: 0 = positive edge 1 = negative edge
12	0_{BIN}	Ready_Open_Drain	Ready pin is 0 = Full push-pull 1 = Open-drain
13	0_{BIN}	Fast_Startup	Sets the Command Window length: 0 = 10ms Command Window 1 = 3ms Command Window
15:14	00_{BIN}	Not Available	**Do Not Change** – must leave at factory settings

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13. Calibration and Signal Conditioning Math

Renesas can provide software and hardware with samples to perform the calibration. For a complete description and detailed examples, see *ZSSC3122/ZSSC3123_SSC_Modular_Evaluation_Kit_Description_RevX_xy.pdf*.

Note: For best results, the calibration should be done with all settings set to the final application including supply voltage, measurement mode, update rate, output mode, resolution, and AFE settings in the final packaging.

13.1 Capacitance Signal Conditioning

The ZSSC3123 supports signal conditioning for an up to two-region piece-wise, non-linear sensor input or a third-order correction, which is selectable. The general form of the capacitance signal conditioning equations are provided below.

Note: The following equations are only meant to show the general form and capabilities of the ZSSC3123 sensor signal conditioning.

Two-region piece-wise, non-linear sensor input:

$$RawTC = \frac{Raw\_C + OFFSET + \Delta T * (Tco + \Delta T * SOT\_tco)}{1 + \Delta T * (Tcg + \Delta T * SOT\_tcg)}$$ **Equation 17**

$$Raw_1 = MIN(RawTC, Raw\_Break)$$ **Equation 18**

$$Raw_2 = MAX(0, RawTC - Raw\_Break)$$ **Equation 19**

$$Out = SOT\_1 * (Gain\_1 * Raw_1)^2 + Gain\_1 * Raw_1 + SOT\_2 * (Gain\_2 * Raw_2)^2 + Gain\_2 * Raw_2$$ **Equation 20**

Or alternatively

Non-linear sensor input up to third-order correction:

$$Raw_1 = \frac{Raw\_C + OFFSET + \Delta T * (Tco + \Delta T * SOT\_tco)}{1 + \Delta T * (Tcg + \Delta T * SOT\_tcg)}$$ **Equation 21**

$$Out = TOT\_1 * (Gain\_1 * Raw_1)^3 + SOT\_1 * (Gain\_1 * Raw_1)^2 + Gain\_1 * Raw_1$$ **Equation 22**

Where:

Symbol	Description
Raw_C	Raw sensor reading.
RawTC	Temperature-corrected raw value.
Raw_1	Raw value to be used for region 1 correction.
Raw_2	Raw value used for region 2 correction.

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Symbol	Description
Raw_Break	Raw value at which the transition from region 1 to region 2 occurs.
Offset	Offset correction for sensor applied at 50% full scale input.
Gain_1	Gain correction for sensor applied to region 1.
SOT_1	Second-order correction for sensor region 1.
Gain_2	Gain correction for sensor applied to region 2 – not used if only 1 region is used.
SOT_2, alternatively TOT_1	Second-order correction for sensor region 2 – not used if only 1 region is used. Used as third-order term TOT_1 for third-order correction.
Tco	Correction for offset drift due to temperature.
Tcg	Correction for sensitivity (gain) change due to temperature.
SOT_tco	Second-order correction for offset drift due to temperature.
SOT_tcg	Second-order correction for sensitivity change due to temperature.
T_{REF}	Raw temperature reading used as a reference temperature for the removal of all TC components.
ΔT	Difference between current raw temperature and the reference temperature.
OUT	Corrected capacitance output value.

13.2 Temperature Signal Compensation

Temperature is measured internally. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearity.

Note: Equation 23 is only meant to show the general form and capabilities of the internal ZSSC3123 temperature signal conditioning.

$$T = SOT\_T * (Raw\_T)^2 + Gain\_T * Raw\_T + Offset\_T$$ **Equation 23**

Where:

Symbol	Range	Description
Raw_T	[0,16383]	Raw temperature reading
Gain_T	[-32768,32767]	Gain correction for internal temperature
Offset_T	[-32768,32767]	Offset correction for internal temperature
SOT_T	[-32768,32767]	Second-order correction for internal temperature
T	[-32768,32767]	Corrected temperature output value

13.3 Limits on Coefficient Ranges

There are range limits on some of the calibration coefficients that will be enforced by the calibration routine provided by Renesas. These limits ensure the integrity of the internal calculations and would only limit the most extreme cases of sensor correction.

Note: For Alarm-only applications, it is critical that the coefficient verification feature of the calibration routine is used since diagnostics are not reported for the Alarms (see section 10.4 for more details).

Table 6.1 shows the limits for correction for the grade of temperature dependency and 2nd nonlinearity of this dependency.

Table 33. Limits on Coefficient Ranges

Coefficient	Correction	Condition
TCO	6060 PPM/K	
SOT_TCO	74 PPM/K²	

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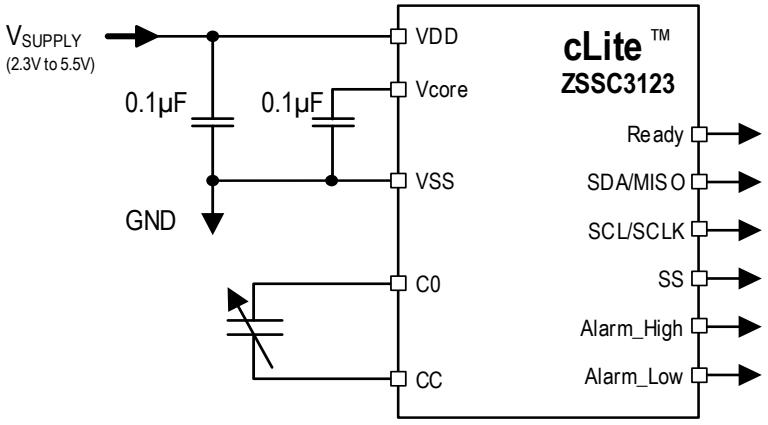
Coefficient	Correction	Condition
TCG	12120 PPM/K	Based on raw temperature values
SOT_TCG	147 PPM/K²	Based on raw temperature values

14. Application Circuit Examples

The ZSSC3123 provides functionality for many different configurations. The following examples correspond to the example circuits shown at the beginning of the specification; however, there are many other possibilities. Combinations of these examples and many other options can give the user maximum design flexibility. Settings for the configuration registers are given with each example. See Table 28 for register addresses. In the examples below, bits 3 and 4 of the *ZMDI_Config* register are marked with an X because they are calculated during calibration and are coefficient dependent (see Calibration and Signal Conditioning Math).

14.1 Digital Output with Optional Alarms

Figure 27. Digital Output with Optional Alarms Example



In this example, a single-ended input capacitance is converted to the digital domain, corrected, and output via I2C. The configuration settings are shown in the following table. The ZSSC3123 operates in Sleep Mode, in which measurement commands are used during normal operation. In this example, the I2C address is 28_{HEX} and the Comm_lock is set.

In this application, both Alarm_High and Alarm_Low are used for digital communication. As shown in the table, both alarms are configured as active high and full push-pull drivers for digital communication.

The AFE configuration registers select 14-bit resolution for capacitance with a capacitance range from 2.9pF to 7.2pF. The internal temperature is set to 14-bit resolution.

Table 34. Example 1: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 29)	0†	0	0	0	1	0	1	1	0	0	0	X	X	0	0	1
Cust_Config (Table 32)	0†	0†	0	0	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 30)	0†	0	0	0	1	1	0†	0†	0†	0†	0	1	0	0	1	1
T_Config (Table 31)	1†	0†	0†	0†	1	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.

† Reserved setting – do not change factory settings.

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14.2 Analog Output with Optional Alarms

In this example, a single-ended input capacitance is converted and corrected, and then both capacitance and temperature are output via the PDM_C and PDM_T pins, which are then low-pass filtered for analog outputs. One of the optional alarms controls an LED. The configuration settings are shown Table 35. In the *ZMDI_Config* register, the output selection bits are set to 10 to select PDM. Example low-pass filter values are given in section 10.7.

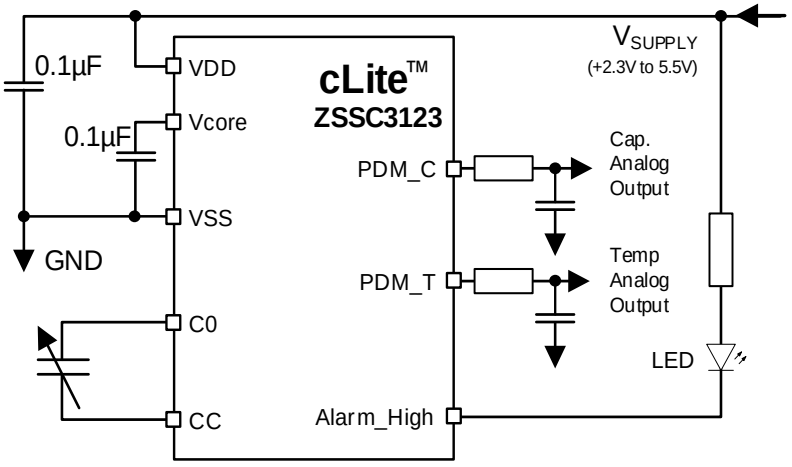

Figure 28. Analog Output with Optional Alarms Example

For PDM, Update Mode must be selected. In this application example, a 25ms power-down period has been used.

In this application, Alarm_High is used to turn on an LED in an open-drain configuration. The output must be low for the LED to be on, so the Alarm_High polarity bit is set to active low. The PDM clipping limits are set for 10% (666_{HEX}) to 90% (3999_{HEX}) output.

The AFE configuration registers show a resolution of 14 bits for capacitance; however, the PDM low-pass filter may be set for a lower resolution with a faster settling time (see section 10.7). A capacitance range of 1.4pF to 8.6pF has been chosen, which requires a Mult setting of 1. The internal temperature is set to 12-bit resolution.

Table 35. Example 2: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 29)	0†	0	1	1	0	0	1	1	0	0	0	X	X	1	0	0
Cust_Config (Table 32)	0†	0†	0	0	0	0	1	0	0	0	1	0	1	0	0	0
C_Config (Table 30)	0†	0	0	0	1	1	0†	0†	0†	0†	0	0	1	1	0	1
T_Config (Table 31)	1†	0†	0†	0†	1	0	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*
PDM_Clip_High	0	0	1	1	1	0	0	1	1	0	0	1	1	0	0	1
PDM_Clip_Low	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0

* The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.

† Reserved setting – do not change factory settings.

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14.3 Bang-Bang Control System

In this example, the only outputs are the alarm pins. They are programmed to control a high voltage bang-bang humidity control system. External devices are not needed if not using high voltage.

If the humidity gets too high, the ZSSC3123 activates the dehumidifier using the Alarm_High pin. If the humidity gets too low, it activates the humidifier with the Alarm_Low pin. The alarm registers must be set to appropriate trip and hysteresis points (see section 3.8). The configuration settings are shown in Table 36.

The output selection bits should either be set to I2C or SPI since, depending on the PDM configuration, both alarms are not supported. Additionally, I2C and SPI are lower power than PDM. This application does not use I2C or SPI, so Update Mode must be used because Sleep Mode commands cannot be sent. The fastest update rate is used for this example. External devices are needed to control the outputs because a voltage source greater than VDD is used.

The alarm pins control NMOS devices so the alarm pins must be full push-pull and output high when the alarm is on, so the polarity bits are set to 0 and the open-drain bits are set to 0.

In this example application, a faster response time may be needed, so the AFE configuration settings show 10-bit resolution for both capacitance and internal temperature. *C_Config* settings have been selected for a capacitance range of 5.8pF to 7.2pF (see Table 6).

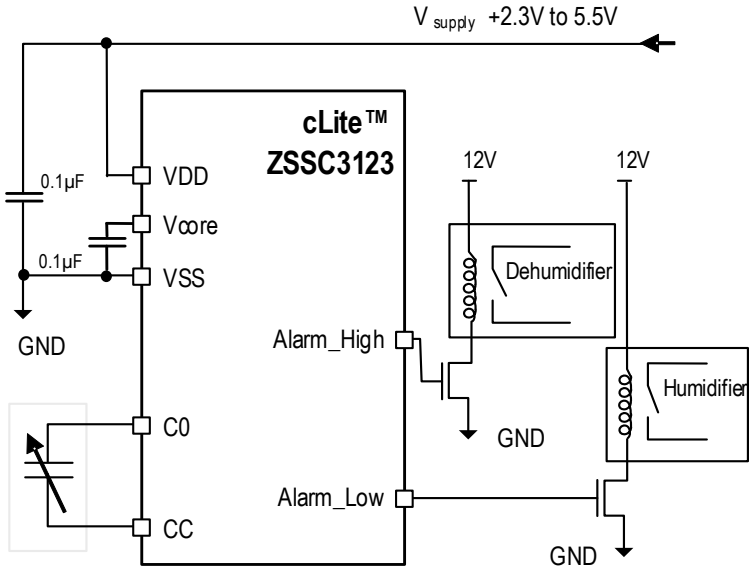

Figure 29. Bang-Bang Control System Example

Table 36. Example 3: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 29)	0†	0	0	0	1	0	1	1	0	0	0	X	X	0	0	0
Cust_Config (Table 32)	0†	0†	0	0	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 30)	0†	0	0	0	0	1	0†	0†	0†	0†	1	0	0	0	0	1
T_Config (Table 31)	1†	0†	0†	0†	0	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.

† Reserved setting – do not change factory settings.

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14.4 Differential Input Capacitance

This example shows that the full functionality of the ZSSC3123 including the applications illustrated in examples 1, 2, and 3, can be implemented with a differential input capacitance. The capacitor CCC allows a non-galvanic connection (e.g., to the moving part of a motion sensor as part of the sensor construction), but it is not needed for sensor types with existing galvanic connections.

The configuration settings are shown in Table 37. The differential bit is set to select differential input capacitance. In this example, SPI has been selected in Update Mode at the fastest update rate. The SPI phase is set to 1 so that the master samples MISO on the negative edge of SCLK. The EEPROM has been locked.

The AFE configuration registers select 14-bit resolution for capacitance and 10-bit resolution for internal temperature. Because this is the differential configuration, both the internal reference and offset capacitors are set to zero.

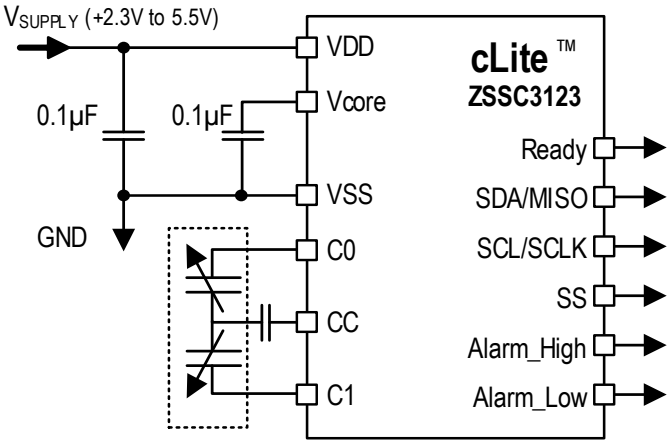

Figure 30. Differential Input Capacitance Example

Table 37. Example 4: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 29)	0†	0	0	1	1	0	0	0	0	1	1	X	X	0	0	0
Cust_Config (Table 32)	0†	0†	0	0	1	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 30)	0†	1	0	0	1	1	0†	0†	0†	0†	0	0	0	0	0	0
T_Config (Table 31)	1†	0†	0†	0†	0	1	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.

† Reserved setting – do not change factory settings.

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14.5 External Reference Capacitor

This example demonstrates that the full functionality of the ZSSC3123, including the applications illustrated in examples 1, 2, and 3, can be implemented with an external reference capacitor in conjunction with a single-ended input capacitance. In this example, the digital output is used. The external reference is used. The configuration settings are shown in Table 38.

Example configuration settings show I2C in Sleep Mode with the Comm_lock off so that the ZSSC3123 can respond to any I2C slave address. Also the Ready pin is configured as open-drain so that multiple devices can have their Ready lines connected together.

The AFE configuration registers select 12-bit resolution for capacitance and 12-bit resolution for internal temperature. This example also shows an offset setting of 4.3pF.

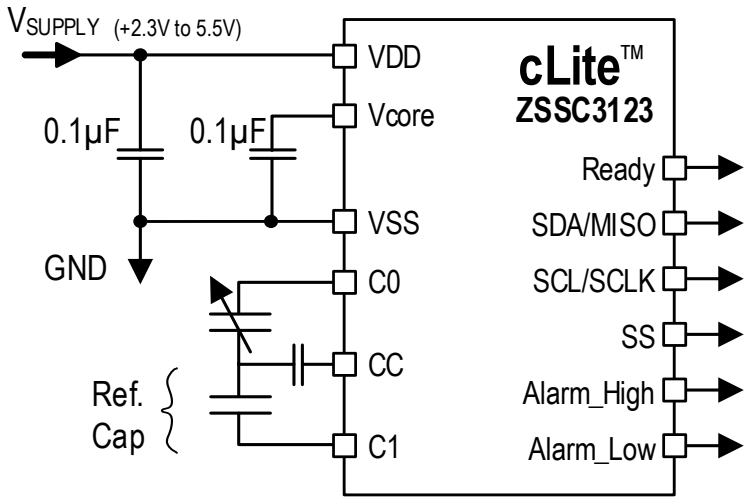

Figure 31. External Reference Input Capacitance Example

Table 38. Example 5: Configuration Settings

Configuration Register	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ZMDI_Config (Table 29)	0†	0	0	0	1	0	0	0	0	0	0	X	X	0	0	0
Cust_Config (Table 32)	0†	0†	0	1	0	0	0	0	0	0	1	0	1	0	0	0
C_Config (Table 30)	0†	0	0	0	1	0	0†	0†	0†	0†	0	1	1	0	0	0
T_Config (Table 31)	1†	0†	0†	0†	1	0	0†	1*	1*	0*	0*	1*	0*	0*	1*	0*

* The factory settings are set for a full span temperature range from -40°C to +125°C. Do not change this setting unless a different temperature range is needed.

† Reserved setting – do not change factory settings.

15. ESD/Latch-Up-Protection

All external module pins have an ESD protection of >4000V and a latch-up protection of ±100mA or (up to +8V / down to –4V) relative to VSS/VSSA. The internal module pin VCORE has an ESD protection of > 2000V. ESD protection referenced to the Human Body Model is tested with devices in TSSOP14 packages during product qualification. The ESD test follows the Human Body Model with 1.5kΩ/100pF based on MIL 883, Method 3015.7.

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16. Test

The test program is based on this datasheet. The final parameters, which will be tested during production, are listed in the tables and graphs of section 5.

17. Reliability

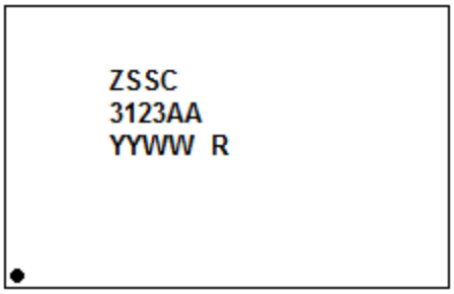
A reliability investigation according to the in-house non-automotive standard will be performed.

18. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.renesas.com/document/psc/14-tssop-package-outline-drawing-44mm-body-065mm-pitch-pgg14t1

19. Example Marking Diagram for TSSOP14 Parts



Line1: Partial part number.

Line 2: Next characters in the partial part number. Refer to section 22 for the available part code variations.

Line 3: "YYWW" represents the last two digits of the year followed by two digits for the work week that the part was assembled. "R" indicates part is "RoHS compliant."

20. Storage and Soldering Conditions

Table 39. Storage and Soldering Condition – TSSOP14

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units
Maximum Storage Temperature	$T_{max\_storage}$	Less than 10hrs, before mounting			150	°C
Minimum Storage Temperature	$T_{min\_storage}$	At original packing only	-55			°C
Maximum Drybake Temperature	$T_{drybake}$	Less than 100hrs in total, before mounting			125	°C
Soldering Peak Temperature	T_{peak}	Less than 30s (IPC/JEDEC-STD-020 Standard)			260	°C

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21. Glossary

Term	Description
ADC	Analog-to-Digital Converter
CDC	Capacitance-to-Digital Converter
DAC	Digital-to-Analog Converter
ECC	Error Checking and Correction
SSC	Sensor Signal Conditioner

22. Ordering Information

Note: Contact Renesas Sales for additional information and for sales and support for the ZSSC3123 Mass Calibration System

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC3123AA1B[a]	ZSSC3123 Die: Tested dice on un-sawn wafer	Not applicable	Wafer (370µm)	-40°C to +125°C
ZSSC3123AA6B	ZSSC3123 Die: Tested dice on un-sawn wafer	Not applicable	Wafer (370µm)	-40°C to +125°C
ZSSC3123AI1B[a]	ZSSC3123 Die: Tested dice on un-sawn wafer	Not applicable	Wafer (370µm)	-40°C to +85°C
ZSSC3123AI6B	ZSSC3123 Die: Tested dice on un-sawn wafer	Not applicable	Wafer (370µm)	-40°C to +85°C
ZSSC3123AA1C[a]	ZSSC3123 Die: Tested dice on frame	Not applicable	Fame (370µm)	-40°C to +125°C
ZSSC3123AA6C	ZSSC3123 Die: Tested dice on frame	Not applicable	Fame (370µm)	-40°C to +125°C
ZSSC3123AI1C[a]	ZSSC3123 Die: Tested dice on frame	Not applicable	Frame (370µm)	-40°C to +85°C
ZSSC3123AI6C	ZSSC3123 Die: Tested dice on frame	Not applicable	Frame (370µm)	-40°C to +85°C
ZSSC3123AA8B	ZSSC3123 Die: Tested dice on un-sawn wafer	Not applicable	Wafer (725µm)	-40°C to +125°C
ZSSC3123AA2T[a]	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Tube	-40°C to +125°C
ZSSC3123AA7T	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Tube	-40°C to +125°C
ZSSC3123AA2R[a]	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Reel	-40°C to +125°C
ZSSC3123AA7R	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Reel	-40°C to +125°C
ZSSC3123AI2T[a]	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Tube	-40°C to +85°C
ZSSC3123AI7T	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Tube	-40°C to +85°C
ZSSC3123AI2R[a]	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Reel	-40°C to +85°C
ZSSC3123AI7R	ZSSC3123 TSSOP14 lead-free package (4.4 × 5.0 mm)	1	Reel	-40°C to +85°C
ZSSC312223KITV1P0	ZSSC3122-3123 SSC Evaluation Kit: Communication Board, SSC Board, Sensor Replacement Board, USB Cable, 5 IC Samples (software can be downloaded from http://www.renesas.com/ZSSC3123)			

[a]Produced in wafer fab 1 location. Not recommended for new design in's.

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23. Revision History

Revision Date	Description of Change
November 19, 2021	▪ Changed to Renesas branding ▪ Update for ordering information ▪ Update for website links
August 16, 2018	▪ Update for template, including reorganization of sections. ▪ Update for typical current consumption value on page 1 to match existing typical specification (750µA) in section 5. ▪ Corrections for table notes in Table 3. ▪ Edits for the text in sections 9.2.1.4 and 10.3.1. ▪ Correction for CDC_Multi availability in Table 30. ▪ Removal of related documents section. Visit www.IDT.com/zssc3122 for related documents. ▪ Removal of references to *ZSSC3123 Technical Note—Detailed Equations for ZSSC3123 Rev C Silicon Math*. ▪ Correction for kit order code. ▪ Update for automatic web appending of the package outline drawing (POD). The POD is now located at the end of the document. ▪ Addition of the moisture sensitivity levels to the part order information table. ▪ Addition of the marking diagram description. ▪ Minor edits to text and figures.
January 26, 2016	Changed to IDT branding.
July 4, 2013	Update for part order codes.
May 20, 2013	▪ Revisions to section 10.3.2.1 to explain preferred method for detecting valid data. ▪ Revision to section 10.6.6 to update Ready pin behavior in Sleep Mode. ▪ Revision to Figure 16.
April 29, 2013	▪ Updated part numbers with new parts. ▪ Update for IDT contact information.
July 23, 2012	▪ Added note for clarity to “Active Regulated Voltage” specification in section 5. ▪ Deleted redundant specification for fOSC in section 5. ▪ Revised the “Excitation Frequency of External Capacitances C0 and C1” (fEXC) specification in Table 1.3 to list a separate specification f_{MULTx} for each Mult setting. ▪ Deleted inapplicable row for 2.0V for the “Error Mult 1, -40 to 125°C” specification in section 5. ▪ Revised specifications for CVCORE_SM and CVCORE_UM in specifications in section 4. ▪ Updated IDT contact information.
October 15, 2012	▪ Revision to maximum specifications for “Start-Up-Time,” “Update Rate (Update Mode),” and “Response Time (Sleep Mode)” in section 5. ▪ Revision to equations in section 9.2.1.1 and 9.2.1.2 ▪ Edits to text under ▪ Note: See section 10.2 for measurement cycle timing. ▪ Figure 13. ▪ Update for IDT contact information.
August 16, 2011	▪ Added specifications in section 5 for V_{POR} maximum, V_{REG} typical and maximum, and PSR_{TEMP}. ▪ Revisions to section 10.3.2.1 to explain preferred method for detecting valid data. ▪ Revised product ordering codes.

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Revision Date	Description of Change
June 29, 2011	▪ Added specification for “Excitation Frequency of External Capacitances C0 and C1” in section 5 and 9.2.1. ▪ Added “PDM frequency” specification to table in section 5. In section 5, clarified that clipping limit default values must be adjusted for PDM output functionality. Revised PDM frequency in sections 5 and 10.7 Revised PDM ripple and settling time specifications in section 5. Revised related examples in Table 24 and corrected Equation 14 for calculating ripple. Revisions to text explaining Equation 16 and subsequent text recommending limits for PDM_Clip_High. Revised Table 28 for PDM_Clip_High and PDM_Clip_Low. Added new settings for PDM clipping limits to section 14.2 and revised related settings in Table 35. ▪ Revised section 8 for addition of specifications for voltage dependency for the temperature channel to section 5. ▪ Revised section 9.2.1.3 regarding total capacitance. ▪ Revised default value for EEPROM word 04HEX from 007THEX to 00FTHEX in Table 28. ▪ Minor edits for clarity in section 14.3. ▪ Revised notes for VCORE pin 1 in Table 1. ▪ Revisions to section 10.3.2.1
February 15, 2011	First release.

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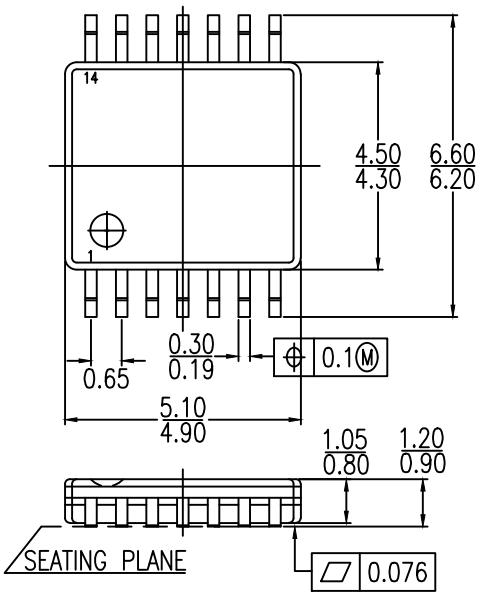

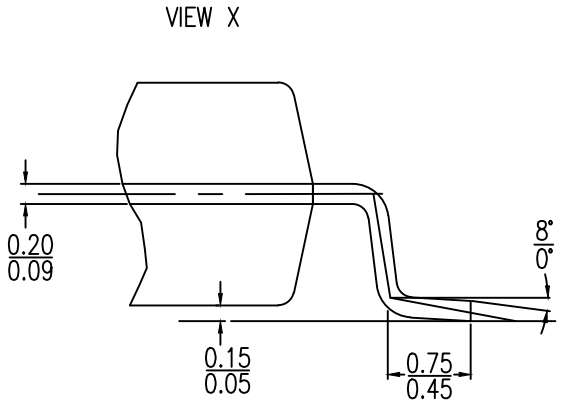

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

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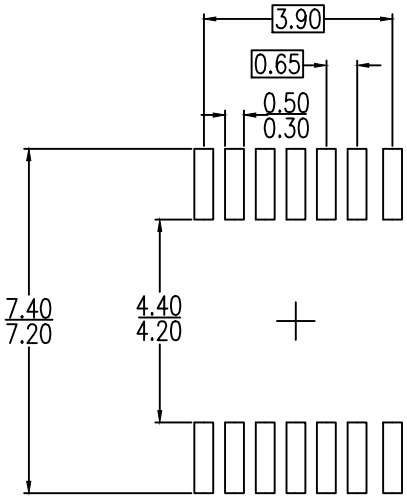

LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Mar, 10 2017	Rev 01	Added Land Pattern
Dec, 19 2017	Rev 02	New Format

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