ZSSC3241

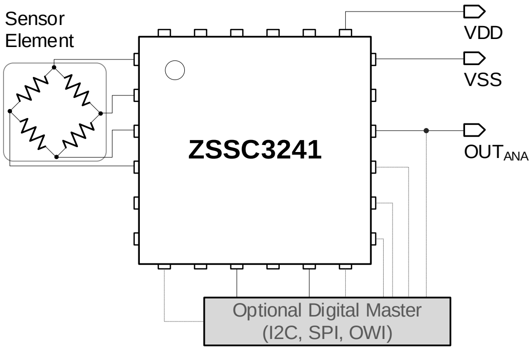
Sensor Signal Conditioner IC for Resistive Sensors

Description

The ZSSC3241 is a sensor signal conditioning IC (SSC) for highly accurate amplification, digitization, and sensor-specific correction of resistive sensor signals. The ZSSC3241 provides best-in-class sensor-element adaptability, and it is suitable for bridge and half-bridge sensors, as well as external voltage-source element and single-element sensors (e.g., Pt100 and external temperature sensor diodes) powered by an on-chip current source. Digital compensation of the sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via a 26-bit math core running a correction algorithm with calibration coefficients stored in a non-volatile, reprogrammable memory. A second, separate compensation for gain and offset, and digital-output independent analog-output correction is supported for optimum adaptability of dual-domain (analog and digital) sensor solutions. The programmable, integrated sensor front-end allows optimally applying various sensors for a broad range of applications.

The ZSSC3241 provides measurement value readouts and programming capabilities via an I2C, SPI, or one-wire interface (OWI). Three different operation modes allow optimal development of digital, digital-analog, and analog-output smart sensor modules including wake-up on request, continuous-on/fast-response, and automatic/cyclic sensor measurement operations. Absolute and ratiometric voltage, current-loop, or interrupt analog outputs are supported by the ZSSC3241. The analog output options and digital interface options (for calibration and/or a digital application interface) can be combined.

Basic Application Diagram



Features

- Digital communication and calibration interfaces
  - SPI up to 10MHz
  - I2C (Standard, Fast, and High-Speed Mode)
  - One-wire-interface (OWI), up to 100kBit/s
- Accommodates nearly all resistive bridge sensor types (signal spans from 1mV/V up to 500mV/V)
- Supports different sensor element configurations:
  - Resistive bridge or half-bridge
  - Resistive divider string
  - Voltage source
- On-chip temperature sensor
- External temperature sensing supported, e.g. sensor-bridge as temperature detector, external diode, etc.
- Support for Pt100
- Programmable 16-bit digital-to-analog-converter and output:
  - (0V to 1V) or (0V to 5V) absolute voltage output
  - V_{DD}-ratiometric voltage output
  - 4mA to 20mA current-loop output supported
- On-chip voltage regulators for sensor supply, and IC operation
- Support for extra regulation by external transistor, for example JFET
- Programmable 24-bit sensor-signal-conditioning (main) math core
- Programmable 16-bit signal-conditioning (support) math core for dual-domain sensor-applications
- Reprogrammable, nonvolatile memory (NVM)
- Programmable measurement scheduler for continuous sensing applications, with optimized balance of:
  - Energy consumption
  - Output update rate
  - Self-diagnostic coverage and system safety
- Programmable analog-output clipping
- On-chip diagnostics:
  - Sensor connection
  - Broken-chip-check / chipping-check
  - Memory integrity

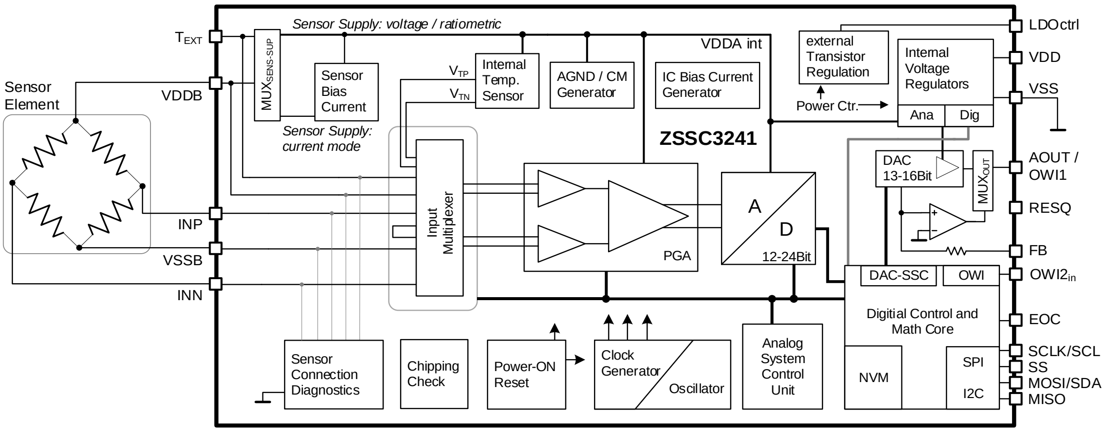
Physical Characteristics

- Supply voltage, V_{DD}: 2.7V to 5.5V; with external transistor, for example JFET: 5V to 48V
- Operating temperature: -40°C to 125°C
- Supported sensor elements: 0.5kΩ to 60kΩ
- Available as die on wafers or 4 × 4 mm^2 24-QFN with wettable flanks, allowing visual inspection of QFN reflow quality

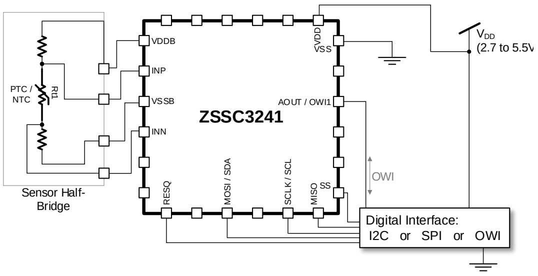
Typical Applications

- Calibrated, continuously operating sensors with digital interface and/or analog output: (absolute or ratiometric) voltage or current loop output
- Enables smart, digital sensors for energy-efficient solutions
- Pressure, flow, and level sensing
- Industrial applications; e.g. process/factory automation
- Consumer / white goods, e.g. HVAC, weight scales
- Medical applications, e.g. blood pressure, continuous smart health monitors

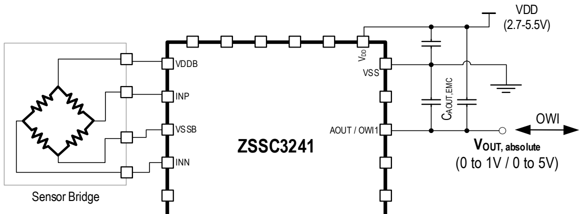
Block Diagram



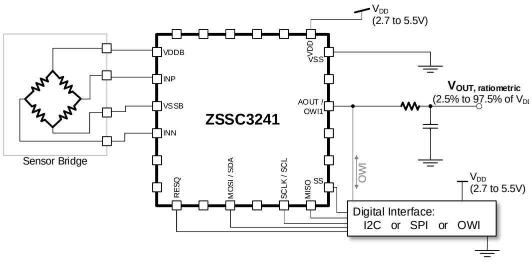
Typical Application Examples



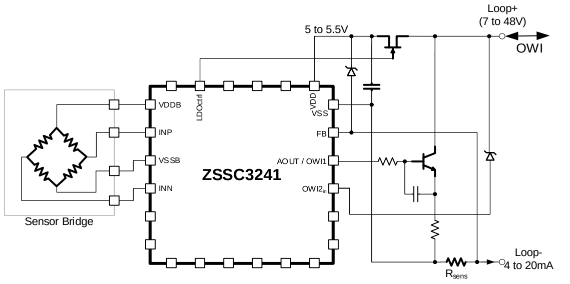
Digital Half-Bridge Sensor, e.g. PT100



Analog Sensor with Absolute Voltage Out



Sensor with Ratiometric Voltage Output and Digital Interface



Analog Sensor with Current Loop Output, OWI, and External JFET

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1. Pin Assignments

The ZSSC3241 is available as 8-inch wafers and in a 24-QFN package. Detailed information about die and wafers is available on request (see last page for contact information).

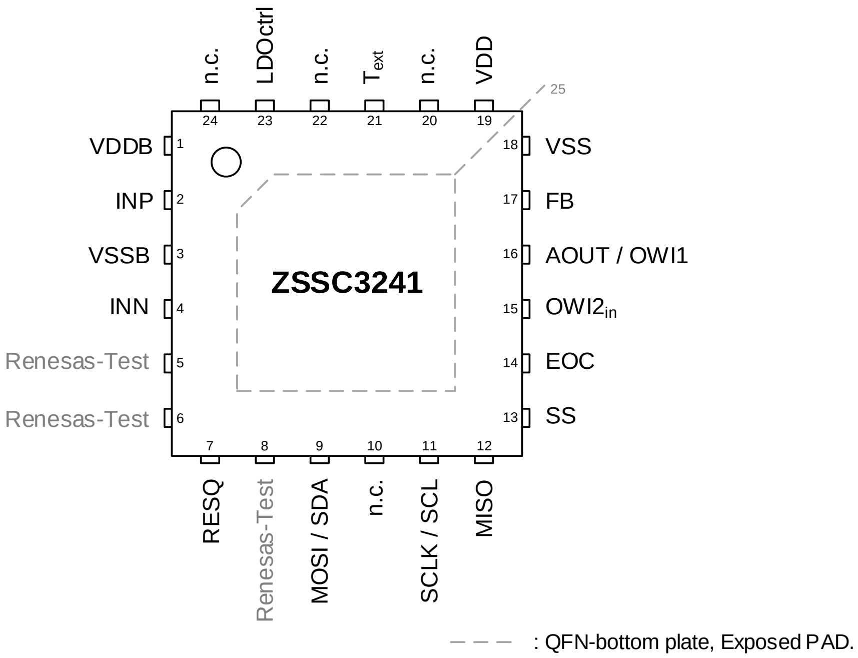


Figure 1. Pin Assignments for 4 × 4 mm² 24-QFN Package – Top View

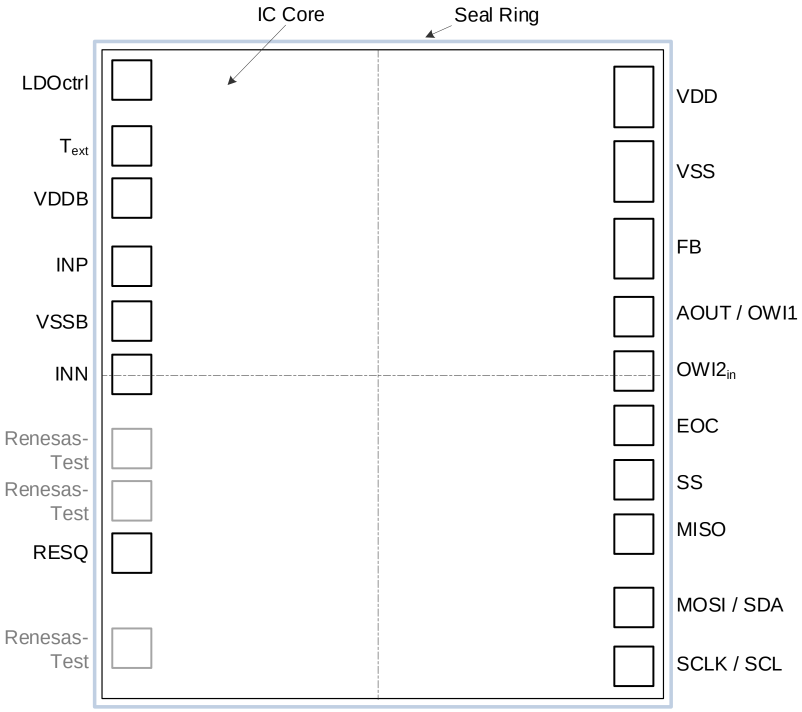


Figure 2. Pin (Pad) Assignments for Bare Die

2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description
1	VDDB	Analog Input/Output	Positive sensor (bridge) supply or sensor-signal input.
2	INP	Analog Input	Positive sensor (bridge) signal.
3	VSSB	Analog Input	Sensor (bridge) ground or sensor-signal input.
4	INN	Analog Input	Negative sensor (bridge) signal.
5	Renesas-test	–	Renesas-internal use only. Connect to VSS or no connection; leave pin floating.
6	Renesas-test	–	Renesas-internal use only. Connect to VSS or no connection; leave pin floating.
7	RESQ	Digital Input	Digital IC reset (low active); internal pull-up.
8	Renesas-test	–	Renesas-internal use only. Connect to VSS or no connection; leave pin floating.
9	MOSI / SDA	Digital Input/Output	Digital data input for SPI or bidirectional data I/O for I2C. Pull-up to VDD.
10	n.c.	–	No connection. Leave pin floating.
11	SCLK / SCL	Digital Input	Clock input for SPI or I2C interface. Referenced to applied VDD level.
12	MISO	Digital Output	Data output from ZSSC3241 to master for SPI interface. Referenced to applied VDD level.
13	SS	Digital Input	Slave select (interface enable) for SPI. Referenced to applied VDD level.
14	EOC	Digital Output	End-of-conversion and output interrupt signal.
15	$\mathrm{OWI2_{in}}$	Digital Input	Optional OWI interface input line for current-loop applications.
16	AOUT / OWI1	Analog Output; Digital Input/Output	Analog smart-sensor output signal and/or OWI-interface input/output line.
17	FB	Analog Output	Current-loop application feedback output (level below VSS!). No connection if not used.
18	VSS	Ground	Power supply ground.
19	V_{DD}	Supply	Power supply.
20	n.c.	–	No connection. Leave pin floating.
21	T_{EXT}	Analog Output	Current drive output for external temperature sensor and/or bridge in Current Mode. A 150Ω serial resistor is built in the IC internally for pad-protection purposes.
22	n.c.	–	No connection. Leave pin floating.
23	LDOctrl	Analog Output	Control output (reference signal) for (optional) external regulator / supply control loop.
24	n.c.	–	No connection. Leave pin floating.
25	Exposed PAD	-	QFN-bottom plate, i.e. Die-bottom/substrate. Leave pin floating (no electrical connection), PAD to be used for heat dissipation only.

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the ZSSC3241 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions might affect device reliability.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
T_J	Junction temperature			135	°C
T_S	Storage temperature		-45	150	°C
	ESD – Human Body Model			4000	V
	ESD – Charged Device Model			750	V
	Latch-up		-100	+100	mA
V_{DD_max}	Maximum allowed for voltage supply	Referenced to VSS.	-0.3	6.5	V
V_{IF_max}	Voltage at digital interface pins	I2C pins: SDA, SCL	-0.3	5.5	V
V_{FB_max}	Voltage at FB pin	4mA to 20mA current loop interface	-2	2	V

4. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
V_{DD}	Power supply voltage	2.7	–	5.5	V
T_A	Ambient temperature (depending on the part code)	-40	–	125	°C
C_{VDD}	External (parasitic) capacitance between VDD and VSS, without external supply transistor regulation	0	100	–	nF
	External (parasitic) capacitance between VDD and VSS, with (optional) external supply transistor regulation	80	100	120	
$C_{VDDB,EMC}$	Recommended, external capacitance between VDDB and VSS for electro-magnetic immunity (EMI)	0	6.8	8	nF
$C_{AOUT,EMC}$	Recommended, external capacitance between AOUT versus VSS, and versus VDD for EMI [a]	0	22	33	nF
I_{Sensor}	Load current through external sensor element [b]	0.02	0.5	4	mA
$V_{DioDrop}$	External temperature diode and RTD input range, drop over external element referenced to T_{EXT} pin	-0.2	–	1	V
V_{Sens_in}	Absolute sensor signal input level, INN, INP pins	0.5	–	1.2	V
$VDDB_{ratio\_min}$	Minimum level at VDDB [b]	0.9	–	–	V
$VSSB_{ratio\_max}$	Maximum level at VSSB [b] At maximum 85°C, up to VSSB=0.60V can be applied under ratiometric sensor supply (with internal Rt’).	-	–	0.55 (0.60)	V
$I_{max\_AOUT\_V}$	Maximum current load at AOUT pin for voltage outputs	-	-	18	mA
SR_{VDD_POR}	Recommended V_{DD} rise slew rate for power-on-reset (POR) [c]	1.5	–	–	V/ms

[a] For applications with OWI-interface or analog voltage-output.

[b] With ratiometric sensor supply configuration; e.g. a ratiometric bridge or bridge as temperature sensor with internal or external Rt.

[c] Per design, there is no (theoretical) minimum V_{DD} slew rate to trigger a clean POR. Nevertheless, a reasonable slew rate is recommended.

5. Electrical Characteristics

All parameter values are valid only under specified operating conditions. All voltages are referenced to V_{SS}.

Table 4. Electrical Characteristics

Note: See important notes at the end of this table.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
IC Supply						
I_{IC}	Current consumption, active IC	Excluding connected sensor elements (with LDOctrl enabled)	–	2.3	2.80	mA
I_{IDLE}	Idle current consumption, IC in Idle State	Typical value at 30°C, maximum value at 85°C (125°C) OWI and LDOctrl disabled	–	1.5	6 (22)	µA
I_{AVE}	Average current draw	Mean current consumption for one complete SSC measurement cycle per second at 16-bit digital-only output	–	–	3.5	µA
$V_{DD,LDOctrl}$	Target level regulation range to generate V_{DD} after external transistor, for example JFET	Using LDOctrl and external transistor; programmable setup: *VDD_ldoctrl_target* (see section 6.7)	4.6	5.2	5.5	V
Sensor Supply						
I_{SUP}	Sensor bias	In the case of a Current Mode sensor supply; setup in *temp_source* and *sensor_sup* (see section 6.2)	5	80	500	µA
Err_{TBIAS}	Relative sensor bias current error [a]		-3.5	-1	1.5	%
V_{TBIAS}	Drop over sensor bias current source	referenced $VDDA_{int}$ from internal analog regulator	–	200	230	mV
VDDB ($VDDA_{int}$)	Internally regulated analog (bridge) sensor front-end supply	In the case of a ratiometric sensor supply, setup in *temp_source* and *sensor_sup*	1.68	1.75	1.80	V
$PSRR_{LOW}$	Power supply rejection ratio[b], only internal regulator	Attenuation of V_{DD} fluctuations in the range of f_{VDD} = 0Hz to 10MHz	45	50	–	dB
$PSRR_{HIGH}$		f_{VDD} > 10MHz	20	–	–	dB
Analog-to-Digital Converter (ADC, A2D)						
r_{ADC}	Resolution		12	16	24	Bit
$f_{S,raw}$	Single-conversion rate, conversions per second	Single external sensor A2D conversion (without auto-zero measurement AZ); resolution dependent	0.21 (ADC: 24-bit)	2.56 (ADC: 16-bit)	5.81 (ADC: 12-bit)	kHz
V_{ADCmid} (AGND)	Differential ADC input common mode [c]	With internal regulator supplying VDDB pin, typical: VDDB/2 = 875mV (equals PGA output common mode level)	–	0.5	–	VDDB
ENOB [g]	Effective number of bits, $3\sigma_{Noise}$ based	For gain < 78, shorted input, r_{ADC} = 24-bit, no oversampling	15.8	18.1	–	Bit
Digital-to-Analog Converter (DAC) and Analog Output						
r_{DAC}	Resolution		13	14	16	Bit
$t_{DACsettle}$	Analog voltage output settling time	Time from 30% steady state until 99% of new DAC output (100% out) value is reached; varies with level differences	0	65	150	µs
V_{DACout}	Addressable output voltage at AOUT pin	Absolute output, *Aout_setup* = 010_{BIN} (see section 6.5.3.2)	0.025	–	1	V
		Absolute output, V_{DD} > 5.01V, *Aout_setup* = 011_{BIN}	0.025	–	5	V
		Ratiometric output, *Aout_setup* = 001_{BIN}	0.1	–	100	%VDD
BW_{DAC}	Output filter bandwidth	Without external components	12	15	20	kHz
SR_{out}	Output slew rate	Resistive load > 2kΩ, capacitive load < 20nF at Aout, temperature = 25°C	20	100	-	mV/µs
I_{OUTmax}	Maximum output current	This current level must be overdriven from an OWI-Master, if concurrent DAC-output and OWI communication is configured.	10	12	18	mA
I_{DRloop}	Current loop driving current	*Aout_setup* = 000_{BIN}; depends on connected bipolar transistor for current loop application	–	100	160	µA

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Programmable-Gain Amplifier (PGA)						
G_{amp}	Gain	120 steps	1.32	–	540	V/V
G_{err}	Gain error	Referenced to nominal gain, T = 25°C	-2.5	0	2.5	%
V_{CMin}	Supported input common mode	$VDDA_{int}$ = 1.75V, valid for ratiometric and current mode sensor supply	0.70	0.85	1.00	V
Sensor Signal Conditioning Performance						
f_{SSCout}	Output (Update) rate [d]	Cyclic operation	0.09	1.22	2.50	kHz
		SSC-corrected (*S, T*) digital output rate, ADC:16-bit (see section 6.5.1)	–	1.22	–	kHz
		Complete SSC cycle (*S, T*) including analog output update; ADC: 14-bit; DAC: 14-bit	1.33	1.43	1.58	kHz
$Err_{A,IC}$	ZSSC3241 accuracy error	Accuracy error with an ideally linear sensor (in temperature and measurand)	–	–	0.01	% FSO
V_{ioffsc}	Correctable (in PGA), absolute, differential input offset	Programmable in 1mV steps; accuracy: ±5% referenced to nominal setup	-15	0	15	mV
$\Delta_{ADC,c}$	Correctable (in ADC), relative, differential input offset	Percentage of sensor signal offset versus maximum sensor signal	0	–	98	%
Input						
V_{INP}, V_{INN}	Absolute sensor input	Voltages at INP and INN pin; resulting minimum/maximum differential voltages: $-700mV < V_{INdiff} < 700mV$	0.5	–	1.20	V
V_{TEXT}	External temperature diode or RTD input range	At T_{EXT} pin	0.5	–	1.25	V
R_{SENSOR}	External sensor (bridge) resistance	VDDB = 1.75V	0.5	–	60	kΩ
		For 4mA to 20mA current loop output	1.6	–	60	kΩ
$\lvert V_{DIFFin}\rvert$	Differential input signal range	Referenced to sensor supply ($VDDA_{int}$); leading to full scale analog excitation	2.6	50	700	mV
Diagnostics						
R_{open}	Sensor connection loss; i.e., open threshold	INP vs. INN	70	–	–	kΩ
R_{short}	Sensor connection short threshold	INP vs. INN; T_{EXT} vs. VDDB	–	–	400	Ω
$V_{s,valid}$	Valid sensor input signal	Beyond $V_{s,valid,}$ sensor connection checks (such as in-range, etc.) signalize Diagnostic *FAULT*s	0.44	–	1.31	V
Power-Up						
t_{STA1}	Start-up Time	V_{DD} ramp up to interface communication	–	–	2	ms
t_{STA2}		V_{DD} ramp up to analog operation	–	–	2.5	ms
t_{WUP1}	Wake-up Time	Sleep to Active State interface communication	–	2	10	µs
t_{WUP2}		Sleep to Active State analog operation	–	–	2	ms
Oscillator						
f_{CLK}	Internal oscillator frequency		5.9	6.0	6.1	MHz
Temperature Sensor(s)						
r_{Temp}	Internal temperature sensor resolution	Setup: $r_{ADC,Tsens,int}$ = 13-bit	12	35	–	Counts/K
Rt, Rt'	Internal low TC [f] top/bottom resistance for external temperature	Programmable with *internal_rt* and *extra_rt*; applied if *temp_source* ϵ {010; 110} (see section 6.2.4)	1.34	–	40	kΩ

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
Interface and Memory						
$f_{C,SPI}$	SPI clock frequency		0.05	1	12	MHz
$f_{C,I2C}$	I2C clock frequency		-	–	3.4	MHz
CD_{OWI}	OWI data rate		0.33	–	10	kBit/s
t_{PROG}	NVM program time	Programming time per 16-bit word	–	3	7	ms
n_{NVM}	NVM endurance	Number of reprogramming cycles	1000	10000	–	Numeric
$t_{RET,NVM}$	Data retention		10	–	–	Years

[a] Referenced to nominal value. Relative errors are typically < 1% for sensor bias current setups > 20µA.

[b] PSRR = $20 \cdot \log_{10}(V_{DD}/V_{DDB})$: will be improved when applying external filter elements at V_{DD} and/or also using an external JFET regulator.

[c] This parameter must be taken into account if automatic common mode regulation in the PGA is switched off (*pga_en_shift*; see section 6.2.1) and a non-symmetric sensor supply and input to the PGA ADC path have been configured.

[d] There are several setups and parameters that allow optimizing and maximizing the output update rate; e.g., ADC and DAC resolutions, configurations for the measurement sequence, usage of the internal or an external temperature sensor.

[e] V_{ioffsc} and $\Delta_{ADC,c}$ can be arbitrarily set up and combined. They work independently on each other.

[f] Typical residual temperature variation of voltage across Rt, Rt': 10ppm/K; maximum deviation: 150ppm/K at 40kΩ and >100°C, all other setups and conditions < 60ppm/K.

[g] ENOB = $\log_2(2^{rADC} / 3\sigma_{Noise})$ with, for example r_{ADC}[Bit] = 24.

6. Device Description

The ZSSC3241 can be set up to for one of three main operating modes:

Sleep Mode	The Sleep Mode is recommended for smart sensors with purely digital output. The ZSSC3241 automatically enters the idle state after command execution for minimum current consumption, whereas the interface is still listening and accepts commands. After receiving a valid command, the ZSSC3241 wakes up, executes the command, provides the results at the digital interface, where the results must be read, and returns to idle state after the data fetch. The results are only available once; repeated data fetch is not supported. In Sleep Mode, sensor measurement results cannot be provided at the analog output of ZSSC3241.
Command Mode	The Command Mode is most appropriate for evaluation, test, and calibration purposes. In this mode, all commands are available, both digital and analog outputs are supported and all functionality is available. Command Mode can be used for applications requiring re-occurring (or even continuous) digital interaction, potential analog output, and minimum latency. Applications in Command Mode are only active on command request.
Cyclic Mode	In Cyclic Mode, autonomous, cyclically repeated sensor measurements are performed and related digital and/or analog output updates are provided. Cyclic Mode is recommended for analog output applications. The cyclic sequence for measurements, diagnostics, and hence the output update rate is configurable.

The ZSSC3241 always enters the programmed *default_mode* after power-on (reset). One of the three operating modes can be set up as the default. After the ZSSC3241 is powered and has entered its default mode, changing to one of the other operating modes is possible via the mode change and start commands: *START_CM, START_CYC, START_SLEEP* (see section 6.6.1 for details).

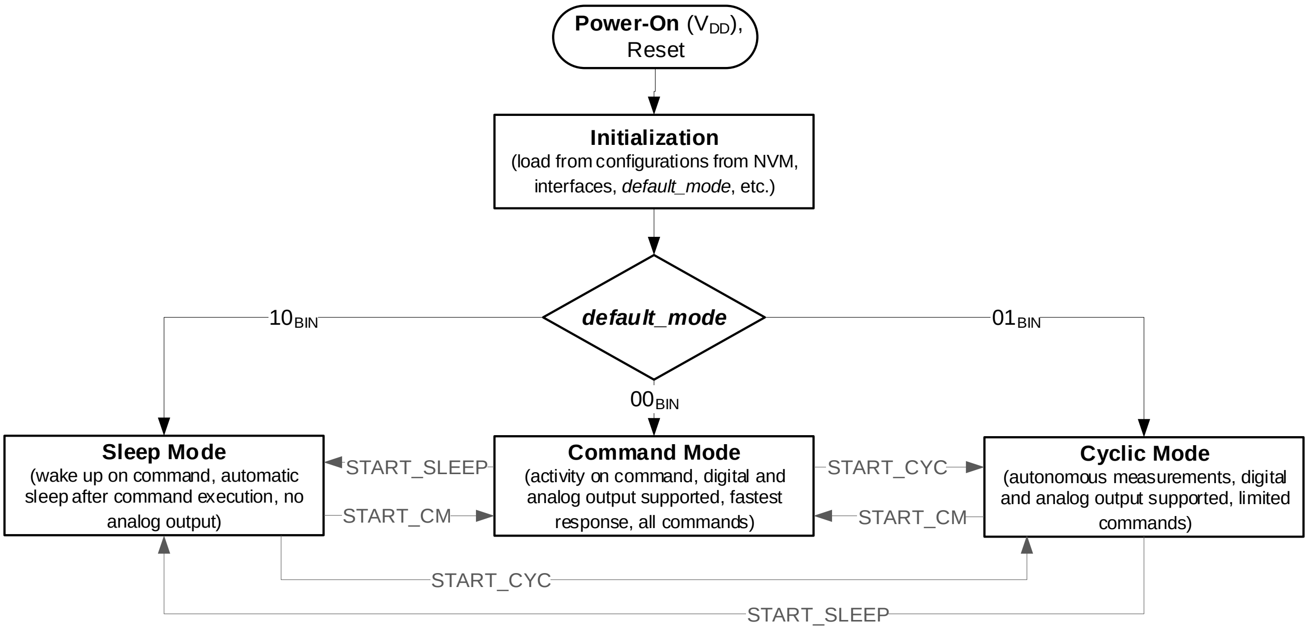


Figure 3. Main Operating Modes of the ZSSC3241

The ZSSC3241 supports three different types of digital interfaces: I2C, SPI, and OWI. All interface types allow application and control of each of the main operating modes.

Exception: The combination of Sleep Mode as the default mode (see the *default_mode* bit in the *SSF1* register in Table 35) and the OWI interface is not supported. The OWI interface must be disabled (*owi_off* = 1, bit[13] in the *SSF1* register) for correct Sleep Mode operation.

When using commands to change the operating mode, e.g. *START_CM* or *START_SLEEP*, validation of the new operating mode is recommended; e.g., by reading an NVM register or simply retrieving the status byte.

Note: The ZSSC3241 always requires two or more interface command interactions after an operating mode change prior to any additional changes in the mode.

6.1 Signal Flow

See the figures on page 2 for the ZSSC3241 block diagram and circuit diagrams for different input sensors. The ZSSC3241 supports two sensor supplies: ratiometric voltage and current mode, i.e., sensor current bias. In the ratiometric sensor-supply configuration, VDDB and the power supply for analog circuitry are provided by an on-chip voltage regulator, which is optimized for power supply disturbance rejection (PSRR). To improve noise suppression, the digital blocks are powered by a separate voltage regulator. A power supervision circuit monitors all supply voltages and generates appropriate reset signals for initializing the digital blocks.

The System Control Unit controls the analog circuitry to perform the measurement types: external sensor, external or internal temperature, and offset measurement. The multiplexer selects the signal input to the amplifier, which can be the external signals from the input pins INP, INN, T_{EXT}, VDDB, and VSSB or the internal temperature reference sensor signals. A full measurement request will trigger an automatic sequence of all measurement types and all input signals. The basic sensor signal source configuration is set up in the *SSF1* register (see Table 35) in the on-chip memory.

The programmable gain amplifier (PGA) consists of two stages with programmable gain values. The ZSSC3241 employs a programmable analog-to-digital converter (ADC) optimized for conversion speed and noise suppression. The programmable resolution from 12 to 24 bits provides flexibility for adapting the conversion characteristics. To improve power supply noise suppression, the ADC uses the external sensor supply voltage, e.g., VDDB for the ratiometric supply of a connected full-bridge sensor element, as its reference voltage leading to a ratiometric measurement topology. The remaining IC-internal offset and the sensor element offset, i.e., the overall system offset for the amplifier and ADC, can be canceled via an offset and auto-zero measurement, respectively.

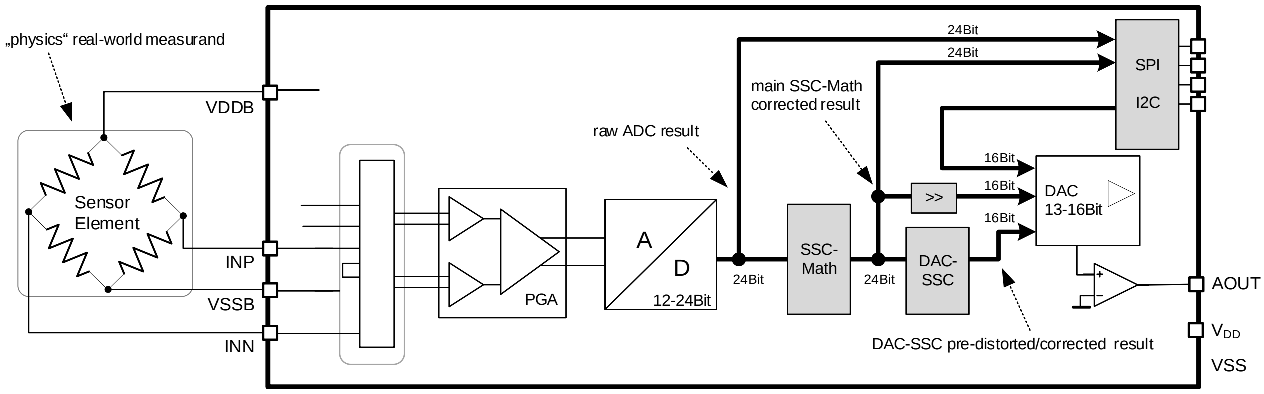


Figure 4. IC-Architecture View for Sensor-Signal-Transfer Perspective

The main math core accomplishes the auto-zero, span, and 1st and 2nd order temperature compensation of the measured external sensor signal. The correction coefficients are stored in the non-volatile memory. In addition to the main sensor or temperature signal compensation (see sections 6.6.3.1 and 6.6.3.2), a separate signal conditioning is integrated to correct DAC offset and gain (see section 6.6.3.3). It is programmable to provide SSC-corrected digital and analog outputs concurrently.

The ZSSC3241 supports SPI, OWI, and I2C interface communication for controlling the ZSSC3241, configuration, and measurement result output. Analog output signals can be provided, which are proportional to the sensor signal that has been compensated for nonlinearity and temperature. The ZSSC3241 can also check and signalize numerous sensor and self-check diagnostic values.

6.2 Analog (Sensor) Front-End

The main blocks and functions of the analog sensor front-end of the ZSSC3241 are illustrated in Figure 5. As a typical first setup, the type and supply of the connected (external) sensor element should be determined and configured. The *sensor_sup* and *temp_source* bits in the *SSF1* register (03_{HEX}; see Table 35) of the NVM must be set up according to the connected sensor configuration.

Important: If using the current mode sensor biasing via the “Sensor Bias Current” block, which is configured with the *Tbiasout* bit field (see section 6.2.4), ensure that the selection for bias current combined with the dimensioning for the connected external sensor is within the input common mode constraints, V_{CMin} (typical 0.85V) as defined in Table 4.

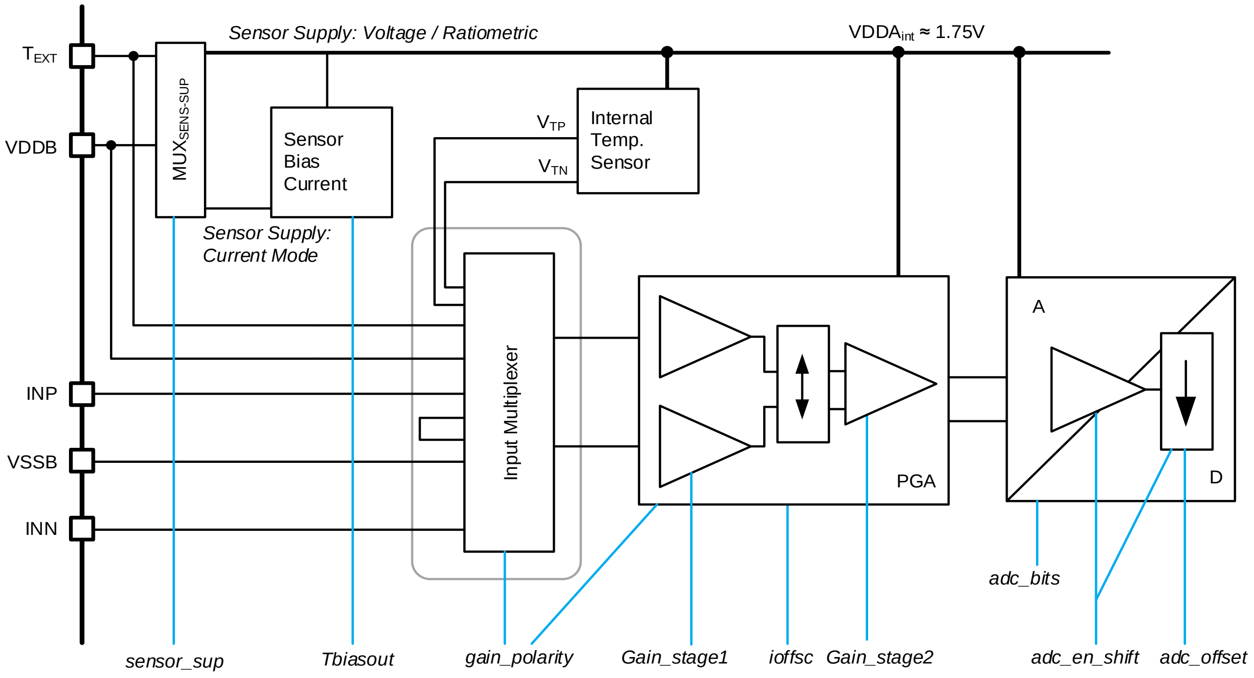


Figure 5. Analog Sensor Front-End Topology

6.2.1. Programmable-Gain Amplifier (PGA)

The amplifier has a fully differential architecture and consists of two stages. The amplification of each stage and the external sensor gain polarity are programmable via settings in the measurement configuration register:

- For the main sensor element: *SM_config1* and *SM_config2* (NVM addresses 14_{HEX} and 15_{HEX}; see Table 35)
- For an optional external temperature sensor: *extTemp_config1* and *extTemp_config2* (NVM addresses 16_{HEX} and 17_{HEX}; see Table 35).

The first 7 bits of the **_config1* registers are the programmable gain settings *Gain_stage1* and *Gain_stage2*. The options for the programmable gain settings are listed in Table 5 and

Table 6. The resulting analog gain is the linear product of the stage 1 and stage 2 selection:

$Gain_{PGA} = Gain_1 \cdot Gain_2$. With the programmable *Gain_polarity* bit in the **_config1* registers, the sign of the effective PGA gain can be swapped; e.g., to invert the sensor characteristic’s slope and invert signal processing of the differential signal between INP and INN.

Table 5. PGA Gain: Stage 1

Gain_stage1[3:0]				Gain$_1$ [V/V]
bit[3]	**bit[2]**	**bit[1]**	**bit[0]**	
0	0	0	0	1.2
0	0	0	1	2
0	0	1	0	4
0	0	1	1	6
0	1	0	0	12
0	1	0	1	20
0	1	1	0	30
0	1	1	1	40
1	0	0	0	60
1	0	0	1	80
1	0	1	0	120
1	0	1	1	150
1	1	0	0	200
1	1	0	1	240
1	1	1	0	300
1	1	1	1	Not assigned

Table 6. PGA Gain: Stage 2

Gain_stage2[2:0]			Gain$_2$ [V/V]
bit[2]	**bit[1]**	**bit[0]**	
0	0	0	1.1
0	0	1	1.2
0	1	0	1.3
0	1	1	1.4
1	0	0	1.5
1	0	1	1.6
1	1	0	1.7
1	1	1	1.8

In addition to the amplification of the sensor input signals, the PGA's first stage can perform an absolute offset shifting of the differential sensor signal. This shift operation can be programmed in 1mV steps with the configuration setup *ioffsc* bit field in the *SM_config2* and *extTemp_config2* registers. The effective voltage-shift depends on the selected Gain$_1$, *Gain_stage1*. The V_{IOFFSC} values (in Table 8) correspond to the higher Gain$_1$ values, i.e. Gain$_1$ > 100. The PGA-operation including shift effect for a differential input signal, V_{DIFFin} can be described as:

$$V_{ADC,IN} = Gain_2 \cdot Gain_1 \cdot (V_{DIFFin} + V_{IOFFSC}) - Gain_2 \cdot V_{IOFFSC} \qquad \textbf{Equation 1}$$

Table 7. Absolute Offset Shift – Properties

Symbol	Parameter	Minimum	Typical	Maximum	Units
Δ_{IOFFSC}	Relative accuracy of the effectively applied Offset Shift referenced to the selected setup per *ioffsc[4:0],* IC-to-IC variation	0.89	0.98	1.07	-
$TC_{neg,IOFFSC}$	1st order temperature coefficient for the change of the effective Offset Shift voltage for negative-voltage shift effects, i.e. *ioffsc[4]*=0	-0.25	-0.21	0	PPT/K
$TC_{pos,IOFFSC}$	1st order temperature coefficient for the change of the effective Offset Shift voltage for positive-voltage shift effects, i.e. *ioffsc[4]*=1	0	0.21	0.25	PPT/K
SNR_{IOFFSC}	Fluctuation of output offset signal (V_{IOFFSC}) versus nominal value at 25°C; $20 \cdot \log10(V_{IOFFSC}/\Delta V_{IOFFSC})$	–	74	–	dB

The shifting can be configured independently for the main sensor and the optional, external temperature sensor. If the absolute offset shifting is enabled, then the ZSSC3241 current consumption increases by 100µA. The advantage of absolute offset shifting is an increase of analog dynamic range in the ZSSC3241's sensor front-end, which results in higher measurement result quality (less noise/fluctuations).

Table 8. Absolute Offset Shift – Differential Sensor Signal's Offset Compensation

ioffsc[4:0]					Shift Effect, V_{IOFFSC}
bit[4]	**bit[3]**	**bit[2]**	**bit[1]**	**bit[0]**	
0	0	0	0	0	0mV, no shift
0	0	0	0	1	-1mV
0	0	0	1	0	-2mV
0	0	0	1	1	-3mV
0	0	1	0	0	-4mV
0	0	1	0	1	-5mV
0	0	1	1	0	-6mV
0	0	1	1	1	-7mV
0	1	0	0	0	-8mV
0	1	0	0	1	-9mV
0	1	0	1	0	-10mV
0	1	0	1	1	-11mV
0	1	1	0	0	-12mV
0	1	1	0	1	-13mV
0	1	1	1	0	-14mV
0	1	1	1	1	-15mV
1	0	0	0	0	0mV, no shift
1	0	0	0	1	1mV
1	0	0	1	0	2mV
1	0	0	1	1	3mV
1	0	1	0	0	4mV
1	0	1	0	1	5mV
1	0	1	1	0	6mV
1	0	1	1	1	7mV
1	1	0	0	0	8mV
1	1	0	0	1	9mV
1	1	0	1	0	10mV
1	1	0	1	1	11mV
1	1	1	0	0	12mV
1	1	1	0	1	13mV
1	1	1	1	0	14mV
1	1	1	1	1	15mV

The PGA can perform an automatic adjustment for the PGA input to ADC input common mode. This can be enabled via the *pga_en_shift* bit in the **_config2* registers. The supportable input common mode range at the PGA, i.e. at the sensor front-end input, is constant per IC because it is derived from the internally regulated voltage $VDDA_{int}$.

Table 9. PGA Input Span Ranges

Total Gain, G_{AMP} Examples	$Gain_1$	$Gain_2$	Max. Input Span, Differential Signal Range [mV]
540	300	1.8	5.0
420	300	1.4	6.4
330	300	1.1	8.1
280	200	1.4	9.6
220	200	1.1	12.2
144	120	1.2	18.5
103	80	1.3	25.9
88	80	1.1	30.5
72	60	1.2	37.5
60	40	1.5	45
48	40	1.2	56
39	30	1.3	69
30	20	1.5	90
19.2	12	1.6	140
13.2	12	1.1	204

Total Gain, G_{AMP} Examples	$Gain_1$	$Gain_2$	Max. Input Span, Differential Signal Range [mV]
10.2	6	1.7	264
5.2	4	1.3	519
3.0	2	1.5	900
1.32 [a]	1.2	1.1	1400

[a] There is a general PGA-input range constraint to support V_{INdiff} of ±700mV at maximum, which is especially dominating for $G_{AMP} < 2$.

6.2.2. Analog-to-Digital Converter (ADC)

An analog-to-digital converter (ADC) is used to digitize the amplifier signal. To allow optimizing the trade-off between conversion time and resolution, the resolution can be programmed from 12-bit to 24-bit (*adc_bits* bit fields in the *SM_config1,* and *extTemp_config1* registers; see section 6.6.2.1). The ADC processes differential input signals around its input common mode level: V_{ADCmid}. Table 10 lists the ADC resolution, signal ranges, conversion times for a single Analog-to-Digital conversion.

Table 10. Single Analog-to-Digital Conversion

adc_bits[3:0]				ADC Resolution [Bits]	Ratiometric ADC Input Range [a], [c], $V_{ADC,IN}$ [V]	Absolute ADC Input Range [b], $V_{ADC,IN}$ [V]	Conversion Time, Typical [µs]	Conversion Rate, Typical [kHz]
Bit[3]	Bit[2]	Bit[1]	Bit[0]					
0	0	0	0	12	±1.42	±1.07	172	5.8
0	0	0	1	13	±1.43	±1.08	202	5.0
0	0	1	0	14	±1.41	±1.06	245	4.1
0	0	1	1	15	±1.42	±1.07	304	3.3
0	1	0	0	16	±1.41	±1.06	390	2.6
0	1	0	1	17	±1.42	±1.07	507	2.0
0	1	1	0	18	±1.41	±1.06	680	1.5
0	1	1	1	19	±1.42	±1.07	913	1.1
1	0	0	0	20	±1.41	±1.06	1255	0.8
1	0	0	1	21	±1.42	±1.07	1725	0.6
1	0	1	0	22	±1.41	±1.06	2410	0.4
1	0	1	1	23	±1.42	±1.07	3345	0.3
1	1	0	0	24	±1.40	±1.06	4715	0.2
1	1	0	1	Not assigned	–	–	–	–
1	1	1	0	Not assigned	–	–	–	–
1	1	1	1	Not assigned	–	–	–	–

[a] With the following settings: ratiometric reference, sel_ref* = 1, and no ADC-shift (*adc_en_shift* = 0) nor extra ADC-gain, i.e. $Gain_{ADC}=1$

[b] With the following settings: absolute reference, sel_ref* = 0, and no ADC-shift (*adc_en_shift* = 0) nor extra ADC-gain, i.e. $Gain_{ADC}=1$

[c] Ratiometric reference together with application setup S2 or T2 (see section 6.2.4) leads to reduced ADC input range due to ADC reference voltage derivation from VDDB pin voltage. ADC reference voltage depends on the mean sensor-bridge resistance and applied sensor bias current.

The ADC can perform an additional offset shift (independent of the PGA shifting with *ioffsc*) in order to adapt input signals with offsets to the ADC input range. The shift feature is enabled by setting *adc_en_shift* = 1 (bit[8] in the *SM_config2* or *extTemp_config2* registers). As defined in Table 11, the respective analog offset shift can be selected with bits [14:12], *adc_offset* in *SM_config1* or *extTemp_config1*.

Note: Enabling the offset shift causes the ADC to perform an additional amplification of the ADC's input signal by factor 2. This must be considered for a correct analog sensor setup by means of the PGA's gain, the absolute offset shift in the PGA, the ADC offset shift, and the potential ADC gain.

The overall analog amplification $Gain_{TOTAL} = Gain_{PGA} \cdot Gain_{ADC}$ can be determined for the following potential use cases using Equation 2 or Equation 3 depending on the ADC offset setting:

If no ADC offset shift is selected, i.e., *adc_en_shift* = 0 and *adc_offset* = 000, then

$$\mathrm{Gain}_{TOTAL} = \mathrm{Gain}_{PGA} \cdot 1$$

Equation 2

If ADC offset shift is selected, i.e., *adc_en_shift* = 1 (*adc_offset* is configurable), then

$$\text{Gain}_{\text{TOTAL}} = \text{Gain}_{\text{PGA}} \cdot 2$$

Equation 3

Table 11. ADC Offset Shift

adc_offset[2:0]			Compensation of Percentage Offset in Input Signal	ADC Input Signal Range [$V_{ADC,IN}$]
bit[2]	**bit[1]**	**bit[0]**		
0	0	0	0%	-0.5 to 0.5
0	0	1	6.25%	-0.44 to 0.56
0	1	0	12.50%	-0.38 to 0.62
0	1	1	18.75%	-0.31 to 0.69
1	0	0	25.00%	-0.25 to 0.75
1	0	1	31.25%	-0.19 to 0.81
1	1	0	37.50%	-0.13 to 0.87
1	1	1	44.00%	-0.06 to 0.94
ADC-offset shift disabled, *adc_en_shift* = 0			0% (compensation, ×2-gain off)	-1 to +1

6.2.3. Internal Temperature Sensor

The ZSSC3241 provides an internal temperature sensor measurement to allow compensation for temperature effects. The temperature output signal is a differential voltage that is adapted by the amplifier (PGA) for the ADC input, comparable to the external sensor's signal. For ZSSC3241-internal temperature measurements, the respective settings are defined and programmed in the NVM by Renesas.

6.2.4. Supported Supplies for Sensor Elements and Additional, External Temperature Sensing

There are two options to supply and bias the external sensor element, which can be selected by the *sensor_sup* bit field in the *SSF1* register (03_{HEX}) in the NVM (see Table 35). The differential sensor signal (e.g., from a sensor bridge) is fed into the ZSSC3241 at the INP pin for the positive and the INN pin for the negative signal level.

Table 12. Sensor Supply Options

sensor_sup[1:0]		External Main Sensor Supply
bit[1]	**bit[0]**	
0	0	Ratiometric voltage: VDDB to VSSB.
0	1	Bias current out of VDDB.
1	0	No supply, INN internally connected to AGND, absolute voltage-source measurement (e.g., thermopile between INP and INN).
1	1	Not assigned.

There are multiple possible combinations of an external main sensing supply and the SSC-input signal generation with different sensing elements and approaches for generating a temperature signal for temperature-dependency compensation, see Table 13. Table 14 illustrates the possible main-sensor connections, application circuits, and ZSSC3241 configurations.

Note: The applications circuits S1 to S3 and T1 to T6 highlight the supply paths in blue and the input signal paths in red for the main sensing element connection and supply in Table 14 and for the supporting, external temperature sensing in Table 16.

Table 13. Supported Sensor Front-End Configuration Options

Supported Sensor Elements		Setup		
Temperature Sensing, T (AZT)	**Main Sensing, S (AZS)**	***temp_source***	***sensor_sup***	**Comment**
IC internal temperature sensor	Sensor bridge, ratiometric supply	000_{BIN}	00_{BIN}	Effect of *sel_ref1* according to Table 35; *Tbiasout; internal_rt, extra_rt, sel_ref2* content without effect

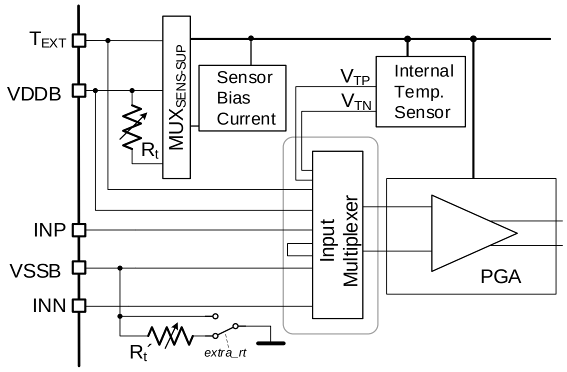
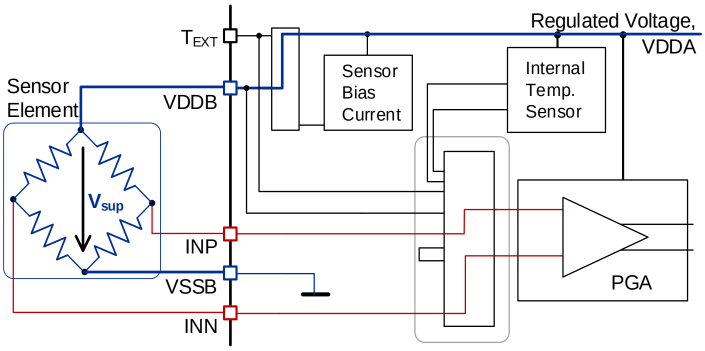
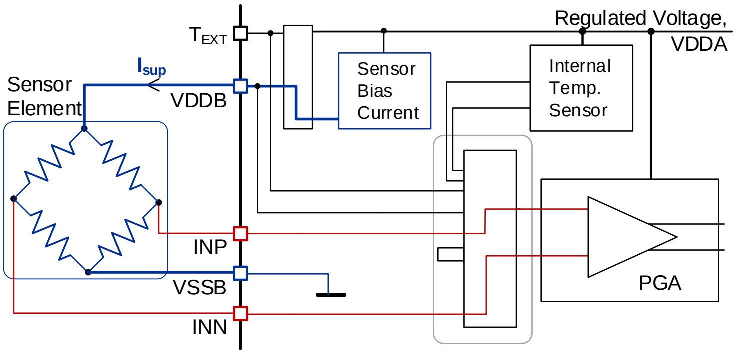
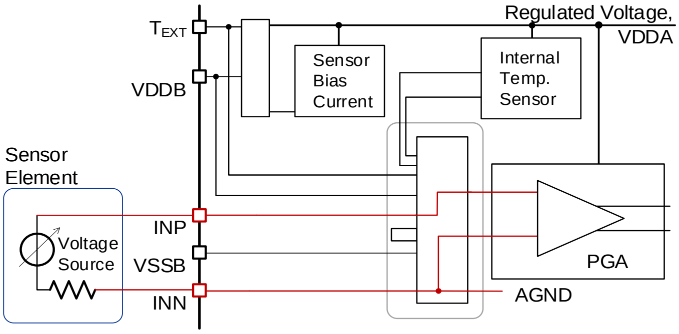
Supported Sensor Elements		**Setup**		
Temperature Sensing, T (AZT)	**Main Sensing, S (AZS)**	***temp_source***	***sensor_sup***	**Comment**
IC internal temperature sensor	Sensor bridge, current-bias supply	000_{BIN}	01_{BIN}	Effect of *sel_ref1* and *Tbiasout* according to Table 35; *internal_rt, extra_rt, extTemp_config* content without effect
IC internal temperature sensor	Absolute voltage source, for example, Thermopile	000_{BIN}	10_{BIN}	Must be set to *sel_ref1*=0_{BIN} *Tbiasout; internal_rt, extra_rt, extTemp_config* content without effect
Main sensor bridge as temperature sensor, ratiometric supply, with internal *Rt* and *Rt'* [b]	Sensor bridge, ratiometric supply	101_{BIN}	00_{BIN}	Must be set to *extra_rt*=0_{BIN}; effect of *internal_rt*, *sel_ref1*, *sel_ref2* according to Table 35; *Tbiasout* content without effect
Main sensor bBridge temperature sensor, current biased, with internal top-*Rt* and bottom-*Rt'*	Sensor bridge, current-bias supply	001_{BIN}	01_{BIN}	Must be set to *extra_rt*=0_{BIN} ; effect of *internal_rt*, *sel_ref1*, *sel_ref2, Tbiasout* as described
Main sensor bridge as temperature sensor, ratiometric supply, with external *Rt* between T_{EXT} and VDDB pads, no internal *Rt*, *Rt'*	Sensor bridge, ratiometric supply	110_{BIN}	00_{BIN}	Must be set to *extra_rt*=1_{BIN}; *sel_ref1*, *sel_ref2* according to Table 35 *Tbiasout; internal_rt* content without effect
Main sensor bridge temperature sensor, ratiometric supply, with external *Rt* between T_{EXT} and VDDB pads and internal bottom *Rt'*, no internal top-*Rt* [b]	Sensor bridge, ratiometric supply	110_{BIN}	00_{BIN}	Must be set to *extra_rt*=0_{BIN} ; *internal_rt, sel_ref1*, *sel_ref2* according to Table 35 *Tbiasout* content without effect
Main sensor bridge temperature sensor, current bias out of T_{EXT} pad, with external *Rt* between T_{EXT} and VDDB pads and internal bottom *Rt'*, no internal top-*Rt*	Sensor bridge, current-bias supply	010_{BIN}	01_{BIN}	Must be set to *extra_rt*=0_{BIN} ; *internal_rt, Tbiasout, sel_ref1*, *sel_ref2* according to Table 35 Note-1: If ratiometric reference is selected for the main sensor, then the reference source is the voltage between VDDB and VSSB (T2, S2 combination see tables below).
External diode or PTC between T_{EXT} and VSSB, current biased, internal bottom-*Rt'* at VSSB (to ground/VSS)	Sensor bridge, ratiometric supply	100_{BIN}	00_{BIN}	Must be set to *extra_rt*=0_{BIN} , *sel_ref2*=0_{BIN} ; *internal_rt, sel_ref1, and Tbiasout* in *extTemp_config* register according to Table 35 *Tbiasout* content in *BM_config* register without effect
External diode or PTC between T_{EXT} and VSSB, current biased, without internal bottom-*Rt'*	Sensor bridge, ratiometric supply	100_{BIN}	00_{BIN}	Must be set to *extra_rt*=1_{BIN} , *sel_ref2*=0_{BIN} ; *sel_ref1,* and *Tbiasout* in *extTemp_config* register according to Table 35 *internal_rt*, and *Tbiasout* content in *BM_config* register without effect
External diode or PTC between T_{EXT} and VSSB, current biased, internal top-*Rt* at T_{EXT} and bottom-*Rt'* at VSSB (to ground/VSS)	Sensor bridge, ratiometric supply	011_{BIN}	00_{BIN}	Must be set to *extra_rt*=0_{BIN} *sel_ref1* as described *internal_rt*, *sel_ref2*, and *Tbiasout* in *extTemp_config* register according to Table 35 *Tbiasout* content in *BM_config* register without effect
External diode or PTC between T_{EXT} and VSSB, current biased, internal bottom-*Rt'* at VSSB (to ground/VSS)	Absolute voltage source, for example, Thermopile	100_{BIN}	10_{BIN}	Must be set to *extra_rt*=0_{BIN}, *sel_ref1*=0_{BIN}, *sel_ref2*=$0_{BIN.}$ *internal_rt*, and *Tbiasout* in *extTemp_config* register according to Table 35 *Tbiasout* content in *BM_config* register without effect
External diode or PTC between T_{EXT} and VSSB, current biased, without internal *Rt*, and *Rt'*	Absolute voltage source, for example, Thermopile	100_{BIN}	10_{BIN}	Must be set to *extra_rt*=1_{BIN}, *sel_ref1*=0_{BIN}, *sel_ref2*=$0_{BIN.}$ *Tbiasout* in *extTemp_config* register according to Table 35*internal_rt*, and *Tbiasout* content in *BM_config* register without effect

Supported Sensor Elements		**Setup**		
Temperature Sensing, T (AZT)	**Main Sensing, S (AZS)**	***temp_source***	***sensor_sup***	**Comment**
External diode or PTC between T_{EXT} and VSSB, current biased, internal top-*Rt* at T_{EXT} and bottom-*Rt*' at VSSB (to ground/VSS)	Absolute voltage source, for example, Thermopile	011_{BIN}	10_{BIN}	Must be set to *extra_rt*=0_{BIN}, *sel_ref1*=0_{BIN}; *internal_rt*, *sel_ref2* and *Tbiasout* in *extTemp_config* register according to Table 35

[a] Any non-listed front end configuration setup leads to the IC internal default with *temp_source*=000_{BIN} and *sensor_sup*=00_{BIN}, i.e. usage of internal temperature sensor and the external sensor(-bridge), ratiometrically supplied, as main sensor.

[b] Take into consideration: max. level constraint for $VSSB_{ratio\ max}$ (see Table 3) in the case of ratiometric (external temperature) supply.

Table 14. Sensor Supply – Main Sensing

Application	Front-End Configuration, Sensor Application, and Connection Circuit[a]	Setup and Remarks
S0		General sensor front-end overview for main and supporting temperature sensor connection and setup
S1		Ratiometric bridge-type sensor setup: - Sensor element supplied through an ZSSC3241 internal, regulated voltage - *sensor_sup* = 00_{BIN}
S2		Current Mode bridge-type sensor setup: - Sensor element biased through an ZSSC3241 internal current source via VDDB pad - *sensor_sup* = 01_{BIN} Note: When combined with T2-application and if ratiometric reference is selected, the reference source is the voltage between VDDB and VSSB for the main sensor measurement.
S3		Absolute-voltage sensor setup: - Sensor element not supplied - *sensor_sup* = 10_{BIN} Note: Only up to a maximum of 50% of the input dynamic range is useable in this configuration

[a] Figure legend:

- Blue line: sensor supply
- Red line: sensor signal

For a ratiometric sensor supply, the $VDDA_{int}$ voltage from the ZSSC3241-internal regulator is used. As defined in Table 15, the alternative sensor bias current source generates a bias current that is programmable with the *Tbiasout* in bit field in the **_config2* registers (see Table 35).

Table 15. Sensor Bias Currents – Sensor Sourcing in Current Mode

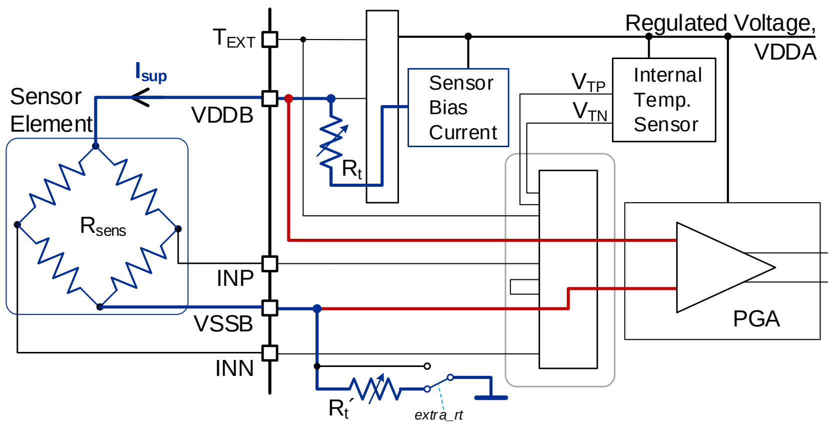
Tbiasout			Nominal Sensor Bias Current [µA]
bit[2]	**bit[1]**	**bit[0]**	
0	0	0	5
0	0	1	10
0	1	0	20
0	1	1	39
1	0	0	79
1	0	1	157
1	1	0	196
1	1	1	494

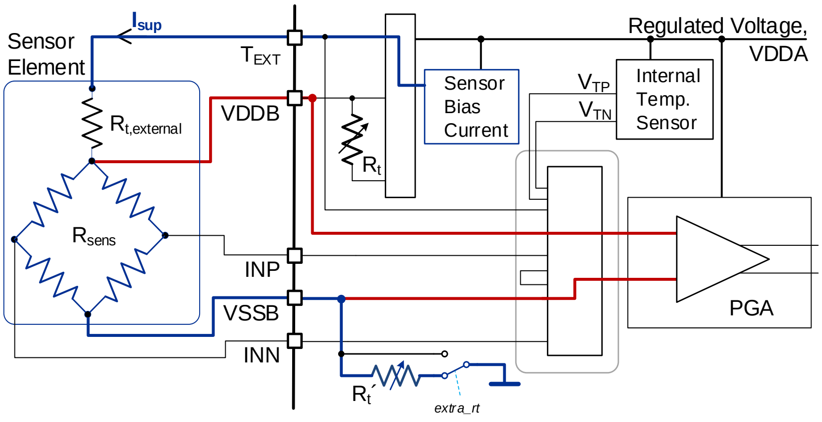
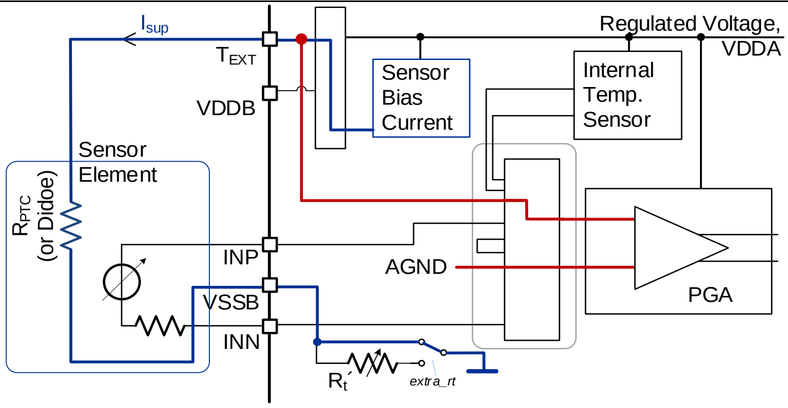
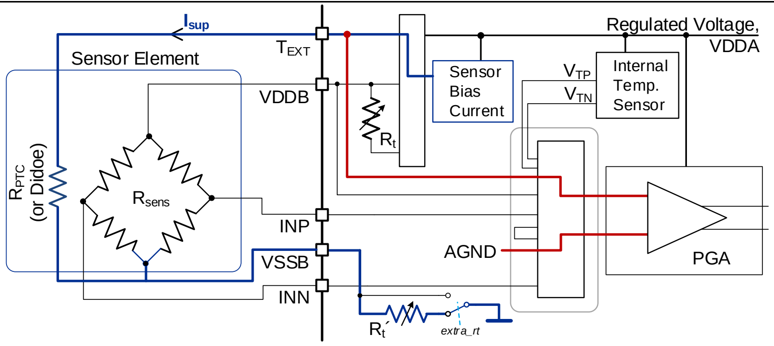
The ZSSC3241 supports internal and external temperature sensing for sensor-signal conditioning (SSC) purposes, i.e. an extra, separate temperature measurement in order to compensate temperature effects in the measurand signal from the main sensing element; e.g., a pressure sensor. The respective setup must be configured via the *temp_source* bit field in the *SSF1* register.

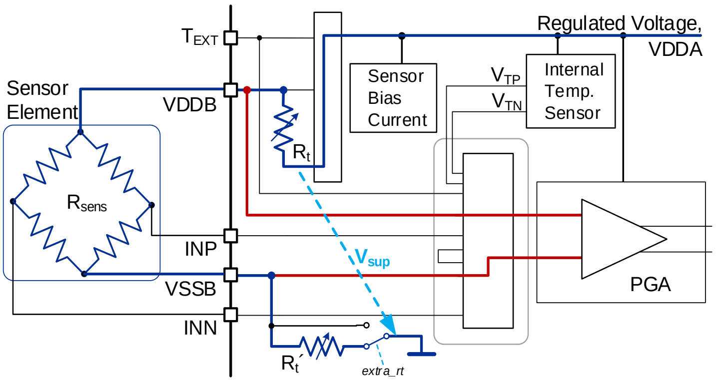
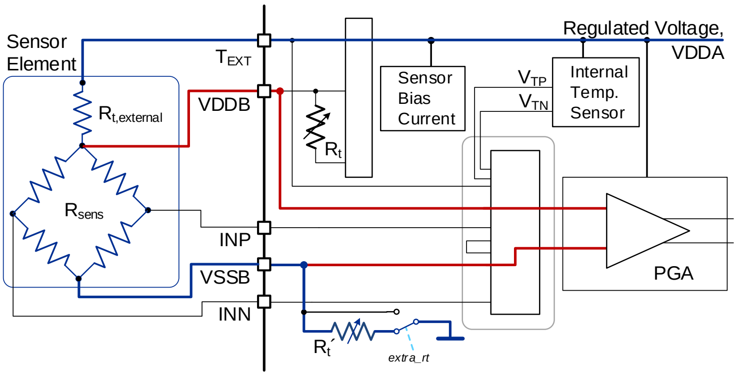
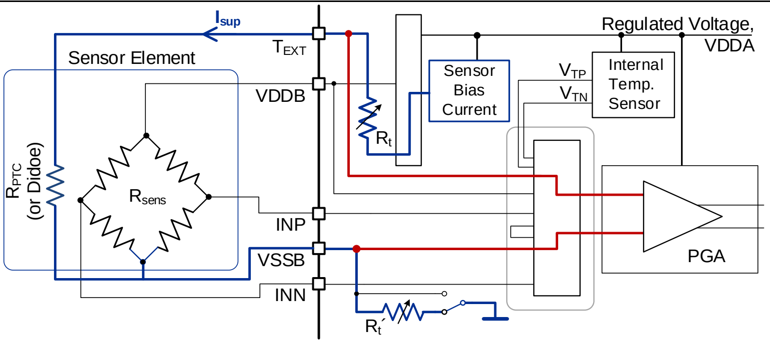
If the main sensing element itself with its inherent temperature sensitivity is used to generate the temperature information for SSC correction, then the *internal_rt* and *extra_rt* bit fields in the *SFF1* register must be programmed. Table 16 provides an overview of the supported IC external temperature measurement main options. The internal resistors *Rt* and *Rt’* have been designed for flat, almost zero-sensitivity to temperature, such that the resulting temperature sensor measurements’ characteristic is mainly dominated only by the (typically spurious) temperature characteristic of the main sensor element itself. The use of the bottom resistance *Rt’*, selectable by *extra_rt*=0_{BIN} is recommended for most related applications in order to have a bridge-resistance-related, symmetric temperature excitation, and not to introduce further differential signal offset when using the bridge-sensor element as the temperature sensor.

In any configuration, the constraints for the minimum/maximum absolute and differential input signal dynamics must be considered.

Table 16. Sensor Supply – IC External Temperature Sensing Configuration Examples

Application	Front-End Configuration, Temperature Sensor Application, and Connection Circuit[a]	Setup and Comments
T1		Bridge as the temperature sensor with the internal *Rt* and *Rt’* in Current Mode - Sensor element supplied through the ZSSC3241-internal bias, i.e., the current source - *temp_source* = 001_{BIN} - *internal_rt* = User selected - *extra_rt* = 0_{BIN} Note: Only combine this T1 application with *sensor_sup* = 01_{BIN} (i.e., main sensing application S2 in Table 14)

Application	Front-End Configuration, Temperature Sensor Application, and Connection Circuit[a]	Setup and Comments
T2		Bridge as temperature sensor with an external *Rt* in Current Mode: • Sensor element supplied through the ZSSC3241-internal bias, i.e., the current source • *temp_source* = 010_{BIN} • *internal_rt* = value close to $R_{t,external}$ • *extra_rt* = 0_{BIN} Note: Only combine this T2 application with *sensor_sup* = 01_{BIN} (i.e., main sensing application S2 in Table 14)
T3.1		Separate diode / PTC-resistor as temperature sensor in Current Mode: • Sensor element supplied through the ZSSC3241-internal bias, i.e., the current source • *temp_source* = 100_{BIN} • *internal_rt* = any • *extra_rt* = User selected • *sel_ref2* = 0_{BIN} must be selected Note: Only combine with *sensor_sup* = 10_{BIN} (i.e., main sensing application S3 in Table 14) Note: The voltage at T_{EXT} must fulfill input conditions and must be in the range of 0.5V to 1.25V
T3.2		Separate diode / PTC-resistor as temperature sensor in Current Mode: • Sensor element supplied through the ZSSC3241-internal bias, i.e., the current source • *temp_source* = 100_{BIN} • *internal_rt* = any • *extra_rt* = User selected • *sel_ref2* = 0_{BIN} must be selected Note: Only combine with *sensor_sup* = 00_{BIN} (i.e., main sensing application S1 in Table 14) Note: The voltage at T_{EXT} must fulfill input conditions and must be in the range of 0.5V to 1.25V

Application	Front-End Configuration, Temperature Sensor Application, and Connection Circuit[a]	Setup and Comments
T4		Temperature sensor with internal *Rt* with ratiometric supply • Sensor element supplied through the ZSSC3241-internal regulated voltage VDDA, i.e., radiometric supply • *temp_source* = 101_{BIN} • *internal_rt* = User selected • *extra_rt* = 0_{BIN} Note: Only combine this T4 application with *sensor_sup* = 00_{BIN} (i.e., main sensing application S1 in Table 14)
T5		Temperature Sensor with external *Rt* with ratiometric supply • Sensor element supplied through the ZSSC3241-internal regulated voltage VDDA; i.e., the radiometric supply • *temp_source* = 110_{BIN} • *internal_rt* = no value or any value close to the external *Rt* • *extra_rt* = User selected Note: Only combine this T5 application with *sensor_sup* = 00_{BIN} only (i.e., main sensing application S1 in Table 14)
T6[b]		Separate diode/PTC-resistor as temperature sensor with internal *Rt* and *Rt'* in Current Mode: • Sensor element supplied through the ZSSC3241 internal regulated voltage VDDA; i.e., the radiometric supply • *temp_source* = 011_{BIN} • *internal_rt* = any • *extra_rt* = 0_{BIN} • *sel_ref2* = User selected Note: Only combine with *sensor_sup* = 00_{BIN} or with *sensor_sup* = 10_{BIN} (i.e., main sensing applications S1 or S3 in Table 14)

[a] Figure legend:
- ○ Blue line: sensor supply
- ○ Red line: sensor signal

[b] The ratiometric supply for the main (bridge) sensor is kept on (if sensor_sup=00BIN is configured) by the IC during temperature measurements.
If T6 is configured together with a non-zero bottom Rt', the joint bias currents: Isup through the temperature sensor element and the current through the bridge sensor must be considered in order to determine the VSSB-level, and hence MIN/MAX of TEXT-VSSB as temperature sensing input signal.

When using scenario T1, "*Bridge as the temperature sensor with the internal Rt in Current Mode*" in Table 16, the setup for bias current (I_{sup}) and internal *Rt* must fulfill the requirements given in Equation 4 and Equation 5:

$$(0.5 \cdot R_{sens} + Rt) \cdot I_{sup} = 0.85\text{V} \pm 125\text{mV} \qquad \textbf{Equation 4}$$

Where R_{sens} is the nominal resistance of the sensor element; i.e. the typical, effective resistance generating the differential sensor signal as input to the INP and INN pads.

Important: Take into consideration the maximum specifications for the PGA common mode input level, V_{Cmin} (see Table 4).

$$(\text{MAX}[R_{sens}] - \text{MIN}[R_{sens}]) \cdot I_{sup} < 700\text{mV} \qquad \textbf{Equation 5}$$

Important: Take into consideration the maximum specifications for the input signal, MAX[V_{DIFFin}] (see Table 4).

The best method for deriving the respective values for *Rt* and I_{sup} is to choose an *Rt* value close to but greater than R_{sens} and to calculate I_{sup} accordingly.

When using scenario T4, "*Temperature sensor with internal Rt with ratiometric supply*," in Table 16 the setup for bias current (I_{sup}) and internal *Rt* must fulfill Equation 6:

Important: Take into consideration the maximum specifications for the PGA common mode input level, V_{Cmin}, which is automatically ensured if *Rt* and the extra *Rt*' are selected.

$$(\text{MAX}[R_{sens}] - \text{MIN}[R_{sens}]) \,/\, (R_{sens} + 2 \cdot Rt) \cdot VDDB_{typ} < 700\text{mV} \qquad \textbf{Equation 6}$$

Important: Take into consideration the maximum specifications for the input signal, MAX[V_{DIFFin}] with $VDDB_{typ}$ = 1.85V.

In most cases, a low *Rt* value will suffice for ratiometrically supplied configurations. The lower the applied *Rt* value, the less the noise-level effect onto the temperature measurement signal.

Sensor-bridge elements, which already contain a top resistor for temperature sensing purposes, can use the internal extra *Rt*'.

6.3 On-Chip Diagnostics

The ZSSC3241 offers analog and digital self-test and sensor-diagnostic features to ensure robust system operation. If the part is programmed and operated with analog output (*cont_ANAoutn* = 0_{BIN} in the *SSF2* register; see Table 35), then diagnostic states are indicated by upper and lower levels at the AOUT pin; see Table 17. With the SPI, I2C, and OWI digital interfaces, the default status byte contains fault-diagnostics information. If further detailed diagnostic information is required, the *CHECK_DIAG* command $B0_{HEX}$ must be issued to retrieve the detailed diagnostics' results in the *diagnosticreg* output register. The content of *diagnosticreg* (see Table 18) is updated each time new respective diagnostic information becomes available. This is also the case with the default ZSSC3241 initialization after power-on-reset (POR) or if specific commands are triggered in order to perform diagnostic checks or influence *diagnosticreg*:

RESET_DIAG, $B1_{HEX}$	Resets the contents of *diagnosticreg.*
UPDATE_DIAG, $B2_{HEX}$	Performs all enabled diagnostic checks (selected via the *select_checks* bit field [9:0] in register 21_{HEX} in NVM; see Table 35) and default diagnostic checks including checksum validation of the NVM; results in complete update of *diagnosticreg.*
Connection Checks	These are scheduled connection checks in the Cyclic Mode setup. All enabled checks (as selected with *select_checks*) are performed, and *diagnosticreg* is updated accordingly.

The analog signalization of diagnostic states at the AOUT pin for the different analog output options can be enabled/disabled via the *diagouten* bit in the *SSF2* register 04$_{\text{HEX}}$ in the NVM (see Table 35). In Cyclic Mode, the analog signalization of a diagnostic state is present with the *SSC Calculation and Output Update* phase of the same measurement slot; see section 6.5.2. In Command Mode (with enabled analog output at AOUT pin), the diagnostic state at AOUT will be present with completion of the next SSC-conversion command, i.e. AA$_{\text{HEX}}$ or AC$_{\text{HEX}}$ to AF$_{\text{HEX}}$; see Table 34).

Table 17. Diagnostic Signalization Options with ZSSC3241

Detected Fault	Analog Ratiometric Diagnostic Level, AOUT [a]	Analog Absolute Diagnostic Level, AOUT [a]	OWI, SPI, I2C Status Byte [7:0]	Comments
No Error / Fault	2.5% to 97.5%	0.125 to 4.875 V [b] 0.025 to 0.975 V [c]	01XX X000$_{\text{BIN}}$	Status after “reset.”
Memory Error	Lower	0 to 0.125 V [b] 0 to 0.025 V [c]	0XXX X**1**XX$_{\text{BIN}}$	Checksum failure of NVM.
Loss of INP Connection, INP Open [d]	Upper	4.875 V to VDD [b] 0.975 to 1.0 V [c]	0XXX XX**1**X$_{\text{BIN}}$	A detailed, digital decoding of the respective connection check fault can be fetched using the B0$_{\text{HEX}}$ *CHECK_DIAG* command, which returns the *diagnosticreg* register content.
Loss of INN Connection, INN Open [d]	Upper	4.875 V to VDD [b] 0.975 to 1.0 V [c]		
INN or INP Signals Out of Range [d]	Upper	4.875 V to VDD [b] 0.975 to 1.0 V [c]		
Bridge/Sensor Short (INN=INP)	Upper	4.875 V to VDD [b] 0.975 to 1.0 V [c]		
T_ext Pin Open [d]	Lower	0 to 0.125 V [b] 0 to 0.025 V [c]		
T_ext Pin Out of Range [d]	Lower	0 to 0.125 V [b] 0 to 0.025 V [c]		
T_ext Pin Short to INP	Lower	0 to 0.125 V [b] 0 to 0.025 V [c]		
T_ext Pin Short to INN	Lower	0 to 0.125 V [b] 0 to 0.025 V [c]		
Die Crack / Chipping Check	Upper	4.875 V to VDD [b] 0.975 to 1.0 V [c]		
SSC Calculation Unit Saturation	Upper (extra)	4.875 V to VDD [b] 0.975 to 1.0 V [c]	0XXX XXX**1**$_{\text{BIN}}$	

[a] Only signalized if *diagouten* = 1$_{\text{BIN}}$.

[b] With VDD = 5V ±10%, for 0 to 5V absolute analog out.

[c] With any VDD, for 0 to 1V absolute analog out.

[d] Do not enable if the IC is connected to an absolute voltage source sensor, for example, Thermopile (*sensor_sup* = 10$_{\text{BIN}}$) with typical internal resistances >60kΩ.

If multiple failures are detected leading to analog outputs that would be contradictory to each other, the high signal is always provided. The effective absolute, analog diagnostic-output level is constant for lower and upper diagnostic signal output. This absolute level may vary from IC to IC slightly. Hence, the effective lower and upper level for the absolute AOUT signal in the event of a valid diagnostic and failure event, respectively, are not influenced by any diagnostic-related setup in NVM nor by calibration coefficients, etc., per the *Aout_setup* bit field in register 04$_{\text{HEX}}$ in NVM (see Table 35). However, the threshold (i.e., the sensor-signal-valid maximum for the upper and minimum for the lower diagnostic band) can be programmed and adjusted via proper calibration and the *diagouten* bit in register 04$_{\text{HEX}}$.

Table 18. Information Assignment for *CHECK_DIAG* Command: Output Register *diagnosticreg* [15:0]

Meaning	Connection Check Content	DAC Output	Bit-Number															
			15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
No Error / Fault	Yes	From SSC	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Fault information improved since last status information	Yes	–	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Loss of sensor positive connection, INP	Yes	$2^{dacres} - 1$	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
Loss of sensor negative connection, INN	Yes	$2^{dacres} - 1$	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Signal at INP pin out of range (leaking / short to VSS or VDDB)	Yes	$2^{dacres} - 1$	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Signal at INN pin out of range (leaking / short to VSS or VDDB)	Yes	$2^{dacres} - 1$	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Sensor short (INN = INP)	Yes	$2^{dacres} - 1$	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
TEXT pin open	Yes	0007_{HEX}	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
Signal at TEXT pin out of range (leaking / short to VSS or VDDB)	Yes	0007_{HEX}	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
TEXT pin short to INN	Yes	0007_{HEX}	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
SSC Calculation Unit saturation	No	$2^{dacres} - 1$	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Memory error, checksum-check failure	No	0007_{HEX}	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
TEXT pin short to INP	Yes	0007_{HEX}	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
Die crack / chipping check failure	No	$2^{dacres} - 1$	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

If a bit reset, i.e. a change from 1_{BIN} (FAULT) back to 0_{BIN} (NO-FAULT), for any bit occurs, *diagnosticreg*[0] is set in order to signal an improvement of fault states during the ZSSC3241 operation. This is especially relevant for Cyclic Mode and Continuous Analog-Output Mode operation.

The *select_checks* bit field in NVM register 21_{HEX} [1] can be programed to select which (analog) checks are executed and/or signalized when the *UPDATE_DIAG* command is triggered or when a connection check is performed during Cyclic Mode operation. Checks that are not selected do not result in *diagnosticreg* register updates and are not signalized at the DAC and AOUT output.

6.4 Digital Interfaces

The ZSSC3241 supports three different digital interface protocols: SPI, I2C, and OWI. The implementation of the interfaces is such that the available commands (section 6.6.1) and request codes for the ZSSC3241 are the same regardless on the interface type used.

The selection of whether the ZSSC3241 operates with SPI, I2C, or OWI interface is determined in the start-up phase after power-on. Initially all interface relevant parameters are loaded from address 02_{HEX} in the NVM (slave address, SPI configuration). If the first command after power-on is a valid and properly formatted I2C request including the correct slave address, the interface is fixed as an I2C slave. If, instead, there is an active signal at the SS pin as the first valid activity, then the IC is fixed as an SPI slave. Alternatively, a valid OWI start (within the start-up window) will fix the interface as OWI. Once the interface is established and fixed, a change of the interface can only be done by means of a power-on-reset; applying signals or protocol of the assumed-inactive interfaces must not happen.
Note: When the active interface is I2C and an active SS-signal (for example, SS==0, when “active low” is configured with *SS_polarity*=0_{BIN}) is applied, the IC can become unresponsive, which can be only resolved by an IC-reset.

The status byte defined in Table 19 is common for all supported interface types, and it is part of the ZSSC3241’s digital response to read requests.

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[1] Recommendation for current loop applications: To minimize the effect of varying current draw in current loop applications, do not perform short-connection checks (*sens_short_check*, *text_inn_short_check*, *text_inp_short_check*).

Table 19. General Status Byte

Bit-Number	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Meaning	0	Powered?	Busy?	Mode		Memory Error?	Connection Check Fault?	Math Saturation

Table 20. Mode Status

Status[4:3]	**Mode**
00	Command Mode
01	Cyclic Mode
10	Sleep Mode
11	Renesas reserved

Note: If the latest command request is a mode change (for example, START_CM) and the previous activity was an SSC-measurement (for example, in Cyclic Mode) in which a *Math Saturation* occurred, then bit[0] of the status byte can still be 1_{BIN} for the response to the mode change command.

6.4.1. SPI

The SPI interface mode is available if the first interface activity after ZSSC3241 power-up is an active signal at the SS pin. The polarity and phase of the SPI clock are programmable via the *CKP_CKE* setting in bits [11:10] in address 02_{HEX} as described in Table 35. *CKP_CKE* is two bits: *CPHA (*bit 10), which selects which edge of SCLK latches data, and *CPOL* (bit 11), which indicates whether SCLK is high or low when it is idle. The polarity of the SS signal and pin are programmable via the *SS_polarity* setting (bit 9).

The different combinations of polarity and phase are illustrated in Figure 6 and Figure 7. See Table 21 for the timing parameters.

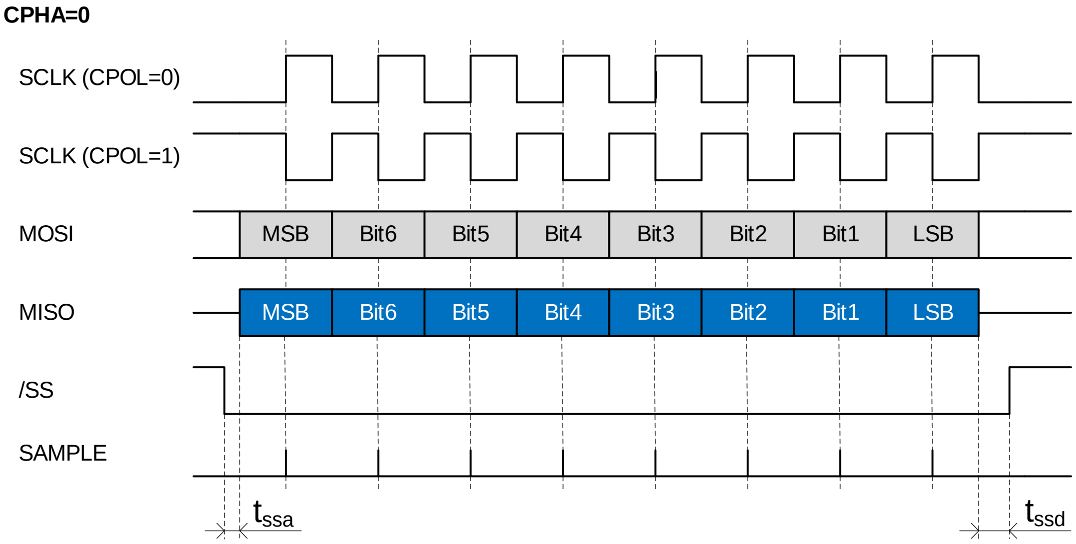


Figure 6. SPI Configuration CPHA=0

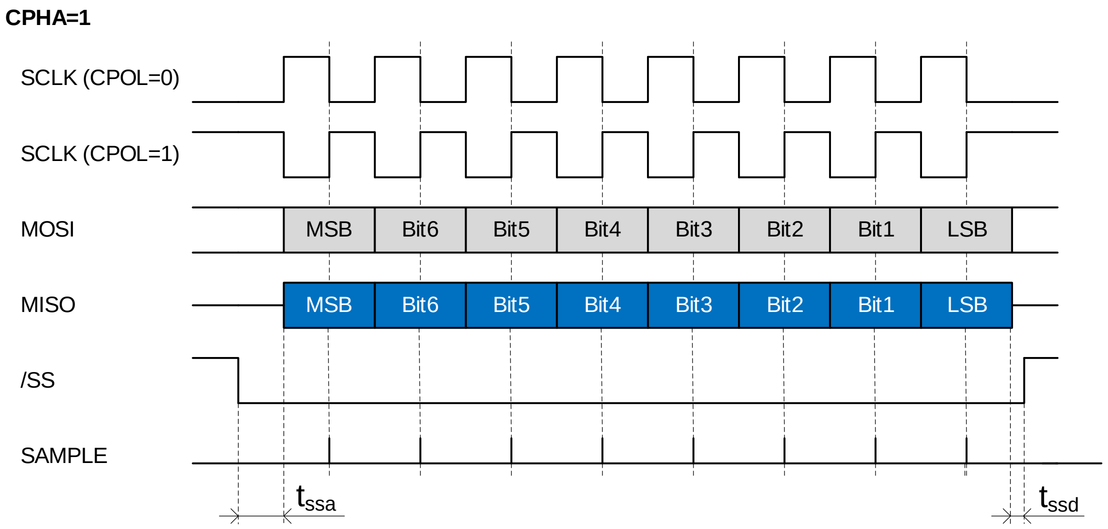
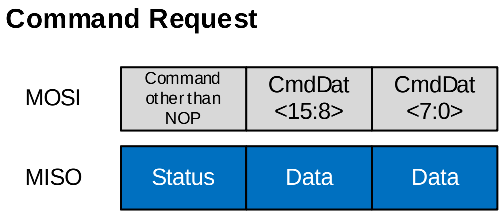


Figure 7. SPI Configuration CPHA=1

In SPI Mode, each command except NOP is started as shown in Figure 8. After the execution of a command (busy = 0), the expected data can be read as illustrated in Figure 9 or if no data are returned by the command, the next command can be sent. The status can be read at any time with the *NOP* command (see Figure 10).

Note: If SS and SCLK do not end after one complete read-response cycle, but continue for any reason, the ZSSC3241 will start repeating; e.g. the measurement result data would repeat in the following sequence (comparable to the OWI response shown in Figure 18):

Status → SensorData [23:16] → SensorData [15:8] → SensorData [7:0] → TempData[23:16] → TempData[15:8] → TempData[7:0] → SensorData [23:16] → SensorData [15:8] →...



Command Request

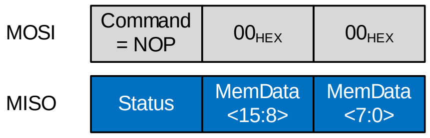
MOSI	Command other than NOP	CmdDat <15:8>	CmdDat <7:0>
MISO	Status	Data	Data

Note: A command request always consists of 3 bytes. If the command is shorter, then it must be completed with 0's. The data on MISO depend on the preceding command.

Figure 8. SPI Command Request

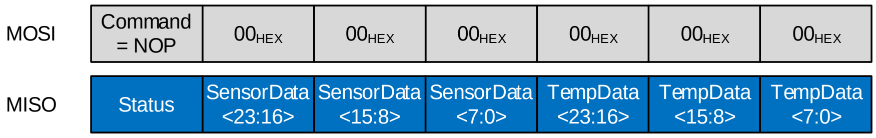
Read Data

(a) Example: after the completion of a *Memory Read* command



MOSI	Command = NOP	00_{HEX}	00_{HEX}
MISO	Status	MemData <15:8>	MemData <7:0>

(b) Example: after the completion of a *Measure* command (AA_{HEX})



MOSI	Command = NOP	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}	00_{HEX}
MISO	Status	SensorData <23:16>	SensorData <15:8>	SensorData <7:0>	TempData <23:16>	TempData <15:8>	TempData <7:0>

Figure 9. SPI Read Data

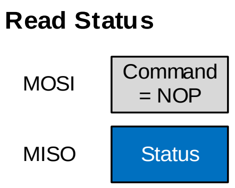


Figure 10. SPI Read Status

Table 21. SPI Interface Parameter

Note: See important table notes at the end of the table.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{SCLK}	Interface clock		0.05	1	12	MHz
D_{SPI}	Duty cycle		40	50	60	%
$V_{high,SPI}$	Input high level voltage	Referenced to external supply voltage V_{DD} (maximum 5.5V)	-	V_{DD} - 0.7	-	V
$V_{low,SPI}$	Input low level voltage		-	0.7	-	V
SR_{SPI}	Input rising and falling edge slew rate		0.26	–	1	V/ns
t_{ssa}	Delay time [a] between SS-activation edge and first edge of SLCK, MOSI or MISO	"Typical" is for f_{SCLK} ≤ 3.4MHz operation	170	300	–	ns
t_{ssd}	Delay time [a] between SS-deactivation edge and last edge of SLCK, MOSI or MISO		1	50	–	ns
t_{ss}	Delay between SS-deactivation edge of last command and of SS-activation edge for next command		10	–	–	µs
I_{MISO}	Driving current of SPI output (peak)		–	40	180	mA

[a] Typical: For conditions with no clocks prior and after the command and data bytes, the maximum values for t_{ssa} and t_{ssd} are not relevant.

6.4.2. I2C

I2C Mode is selected if the first interface activity after the ZSSC3241 power-up is an I2C command with valid slave address. In I2C Mode, each command is started as shown in Figure 11. Only the number of bytes that are needed for the command must be sent. An exception is the I2C High Speed Mode where 3 bytes must always be sent as in SPI Mode. After the execution of a command (busy = 0), the expected data can be read as illustrated in Figure 12 or if no data are returned by the command, the next command can be sent. The status can be read at any time as described in Figure 13.

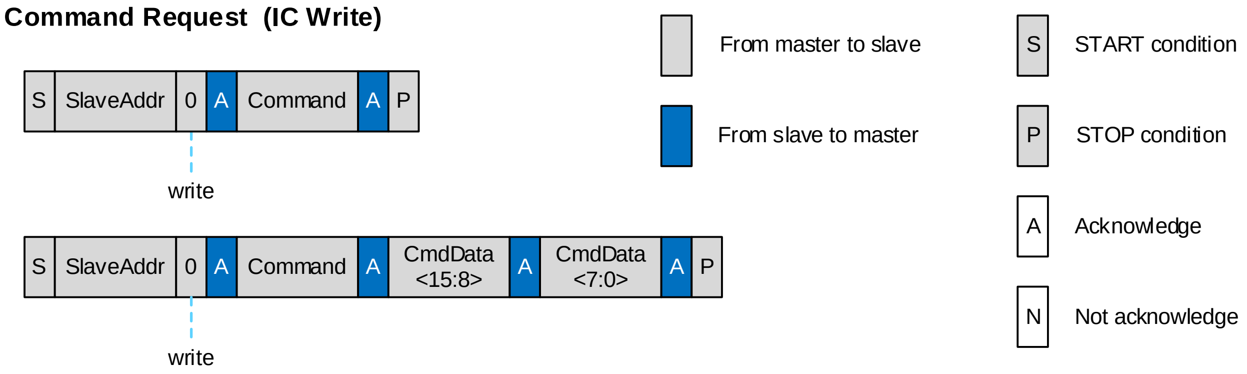
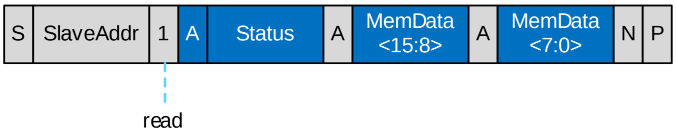


Figure 11. I2C Command Request

Read Data (I2C Read)

(a) Example: after the completion of a Memory Read command



(b) Example: after the completion of a ***Measure*** command (AA_{HEX})

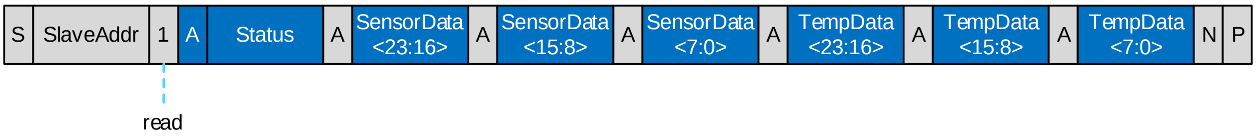


Figure 12. I2C Read Data

Read Status (I2C Read)

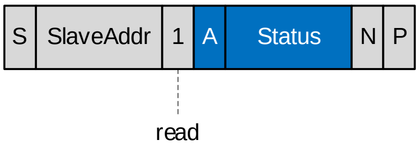


Figure 13. I2C Read Status

Table 22. I2C Interface Parameter

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
f_{SCL}	Interface clock		0.1	–	3.4	MHz
D_{SPI}	Duty cycle		33	–	50	%
$V_{high,I2C}$	Input high level voltage	Referenced to external supply voltage $V_{DD.}$	-	V_{DD} - 0.7	-	V
$V_{low,I2C}$	Input low level voltage		-	0.7	-	V
C_{SDA}	Capacitive load at input pin, SDA	100pF: maximum for Standard and Fast Mode; in HS Mode $f_{SCL,max}$ = 3.4MHz 400pF: only in HS Mode; $f_{SCL,max}$ = 1.7MHz	–	100	400	pF
I_{OL}	Low level output current	V_{SDA}=0.4V; Standard and Fast Mode with 400kHz; 400pF load	3	6	40	mA

Details for timing and protocol of the ZSSC3241-supported I2C communication in Standard Mode, Fast Mode, and High-Speed Mode are given in *I2C-Bus Specification, Rev.6, UM10204*.

6.4.3. One-Wire-Interface, OWI

The ZSSC3241 employs a one-wire digital interface concept (OWI). It combines a simple and easy protocol adaptation with a cost-saving pin sharing. The communication principle of the OWI interface is derived from the I2C protocol.

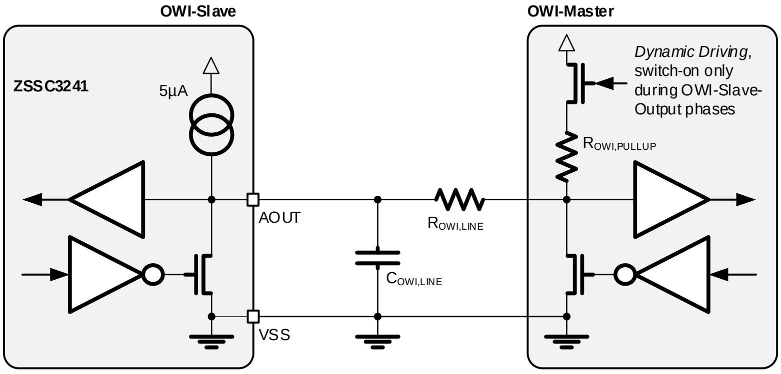


Figure 14. General Block Schematic of the OWI Interface

Both the analog output signal and the digital OWI interface use the same pin, AOUT. An advantage of the OWI is that it enables “end of line” calibration – no additional pins are required to digitally calibrate a finished assembly. Although the OWI is integrated mainly for calibration, it can also be used to read out the calibrated sensor signal continuously or retrieve diagnostic detail information.

The OWI protocol is defined as follows:

- **Idle State:** During inactivity of the bus, the OWI line is pulled up to the supply voltage V_{DD} by an external resistor.
- **Start Condition:** When the OWI line is in idle mode, a low pulse with a minimum width of $t_{OWI,START} \geq 10\mu s$ and then a return to high indicates a start condition. Every request must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
- **Valid Data:** Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from low to high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, $t_{OWI,BIT}$ in Figure 15). A duty ratio greater than 1/8 and less than 3/8 is detected as 0; a duty ratio greater than 5/8 and less than 7/8 is detected as 1. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period because a stop condition is detected in this case.

The length of the OWI-line and the size of $R_{OWI,PULL}$ (if it is statically connected to AOUT), and consequently the resistive and capacitive load influence the maximum possible interface speed and minimum Bit period, respectively. Further, it can be beneficial for harsh EMC conditions to intentionally add capacitance to the OWI1 (AOUT) line in order to improve RF disturbance robustness. Table 23 shows some practical OWI-interface dimensioning examples and the resulting maximum signal frequencies (minimum possible Bit periods). The complete ZSSC3241’s OWI interface properties and timing capabilities are given in Table 24.

Table 23. OWI Dimensioning Examples

$R_{OWI,PULL}$ (+ $R_{OWI,LOAD}$) $C_{OWI,LOAD}$ [a]	1.8 kΩ	2.5 kΩ	3.3 kΩ	5.5 kΩ	10.0 kΩ
1nF	20µs	20µs	21µs	35µs	63µs
10nF	113µs	157µs	207µs	345µs	628µs
22nF	249µs	345µs	456µs	760µs	1381µs
33nF	373µs	518µs	684µs	1140µs	2070µs
44nF	497µs	691µs	912µs	1520µs	2762µs
51nF	576µs	801µs	1057µs	1760µs	3205µs

[a] Examples are shown with statically connected $R_{OWI,PULL}$, and with minimum bit period: $t_{OWI,BIT}$.

OWI protocol timing and parameters are specified in Figure 15, Figure 16, and Table 24.

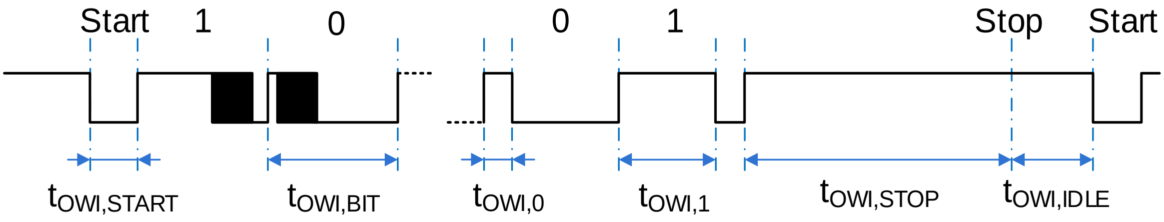


Figure 15. OWI Timing Diagram

Note: Configuration for *SSF1* register 03$_{HEX}$ in NVM (see Table 35) to allow continuous OWI and concurrent analog output: *owi_off* = 0, *cont_ANAoutn* = 0, *owi_su_case* = 1.

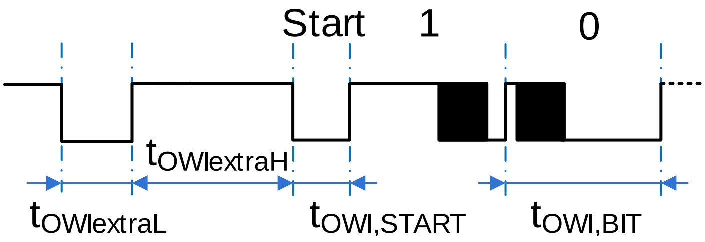


Figure 16. OWI Extra (Activation) Pulse for Concurrent OWI and Analog Output Configuration

Table 24. OWI Interface Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$t_{SUlength}$	OWI start-up “listening” window	Programmable window length , see *owi_su_length,* bit[2] in *SSF1* register	–	–	50	ms
$t_{OWI,IDLE}$	Bus free time between START and STOP condition	For Cyclic and Command Mode operation	1	30	–	µs
		Minimum in ZSSC3241 Sleep Mode operation	20			
$t_{OWI,START}$	Hold time for START condition		20µs	0.5 × t_{OWI_BIT}	–	µs
$t_{OWI,BIT}$	Bit period, bit time	Robust operation with: $t_{OWI,BIT} \geq 10 \cdot R_{OWI,PULL} \cdot C_{OWI,LOAD}$	20	40	3000	µs
$t_{OWI,0}$	Duty ratio bit ‘0’		0.125	0.25	0.375	t_{OWI_BIT}
$t_{OWI,1}$	Duty ratio bit ‘1’		0.625	0.75	0.875	t_{OWI_BIT}
$t_{OWI,STOP}$	Hold time STOP condition	$t_{OWI\_BIT\_L}$ is the bit period of the last valid bit	1.5	3		$t_{OWI\_BIT\_L}$
$t_{OWI\_BIT\_DEV}$	Bit time deviation	Duration of most recent bit versus previous bit duration	0.55	1.0	1.45	t_{OWI_BIT}
$t_{OWIextraL}$	Length of extra pulse [a]	OWI configuration to allow continuous OWI and concurrent analog output; see Figure 16.	43.5	–	49.5	µs
$t_{OWIextraH}$	Duration of HIGH after Aout-to-OWI extra pulse		43.5	–	–	µs
$C_{OWI,LOAD}$	Capacitive load at OWI line	Minimize $C_{OWI,LOAD}$ if ratiometric DAC-output, *Aout_setup* = 001$_{BIN}$ is configured for AOUT/OWI1	0.05	2.2	66	nF
$R_{OWI,PULL}$	Pull-up resistance – master [b]	If $R_{OWI,PULL}$ values greater than 3.3kΩ were applied, the shortest $t_{OWI,BIT}$ times cannot be achieved anymore.	1.8	2.5	3.3	kΩ
$R_{OWI,LOAD}$	Resistive OWI line load	If $R_{OWI,LOAD}$>35Ω, OWI-timing parameter ($t_{OWI,*}$) low-limits, i.e. highest speeds are not guaranteed.	0	0.01 x $R_{OWI,PULL}$	–	Ω
$V_{OWI,inL}$	Voltage level LOW		–	0.1	0.25	VDD
$V_{OWI,inH}$	Voltage level HIGH		0.80	0.9	–	VDD

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V_{OWI\text{-}S,LOW}$	Slave output level LOW	Open drain output at AOUT pin, max. allowed current draw 5mA, otherwise: $V_{OWI\text{-}S,LOW}$ >0.1*VDD	–	–	0.1	VDD

[a] To switch from analog output to "OWI listen" at AOUT pin.

[b] For the selection of $R_{OWI,PULL}$, the minimum current limit of the AOUT buffer and maximal VDD supply must take into account if OWI and analog output voltage mode are set up to work concurrently; that is *owi_off* = 0, *cont_ANAoutn* = 0, and *owi_su_case* = 1. If the current limitation condition (I_{OUTmax}, see Table 4) is exceeded, it is recommended to use the Dynamic Driving Approach for $R_{OWI,PULL}$ at the OWI-master, and only switch the $R_{OWI,PULL}$ to AOUT when the OWI-master starts communication. This setting is specifically recommended for the phases when the OWI-master listens to the AOUT-line, and the OWI-slave (the ZSSC3241) has to respond, respectively.

The effective OWI properties depend on the load conditions at the OWI1 pin. Additional to Table 23, some further applicable configurations are as follows:

- For maximum operation speed (50kHz) of OWI1, the capacitive load, $C_{OWI,LOAD}$ can be up to 1nF and the maximum $R_{OWI,PULL}$ is 2.5kΩ.
- For high operation speed (10kHz) of OWI1, the capacitive load, $C_{OWI,LOAD}$ can be up to 4.7nF and $R_{OWI,PULL}$ must be ≤ 3.3kΩ.
- For an equivalent frequency of 1kHz of OWI1, it should be ensured that $C_{OWI,LOAD} \leq$ 22nF and $R_{OWI,PULL}$ ≤ 7kΩ, or for example that $C_{OWI,LOAD} \leq$ 66nF combined with $R_{OWI,PULL}$ ≤ 4.5kΩ.

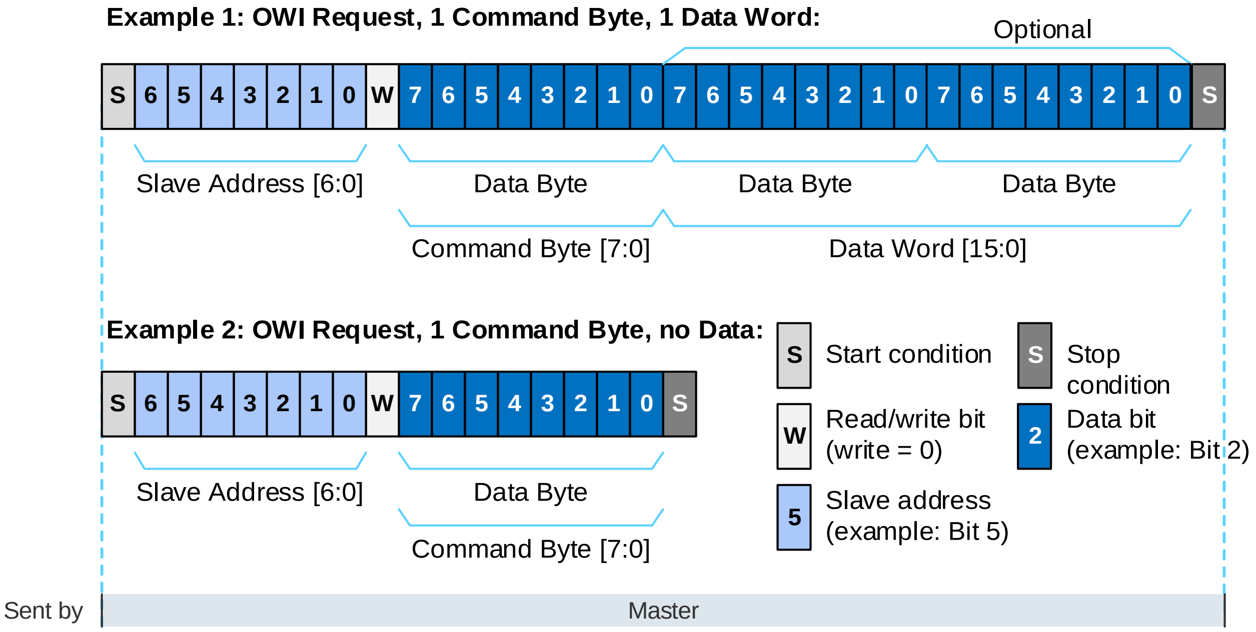


Figure 17. OWI Command Request

Example: OWI Read Operation, Status Byte (+n) Data Bytes*:

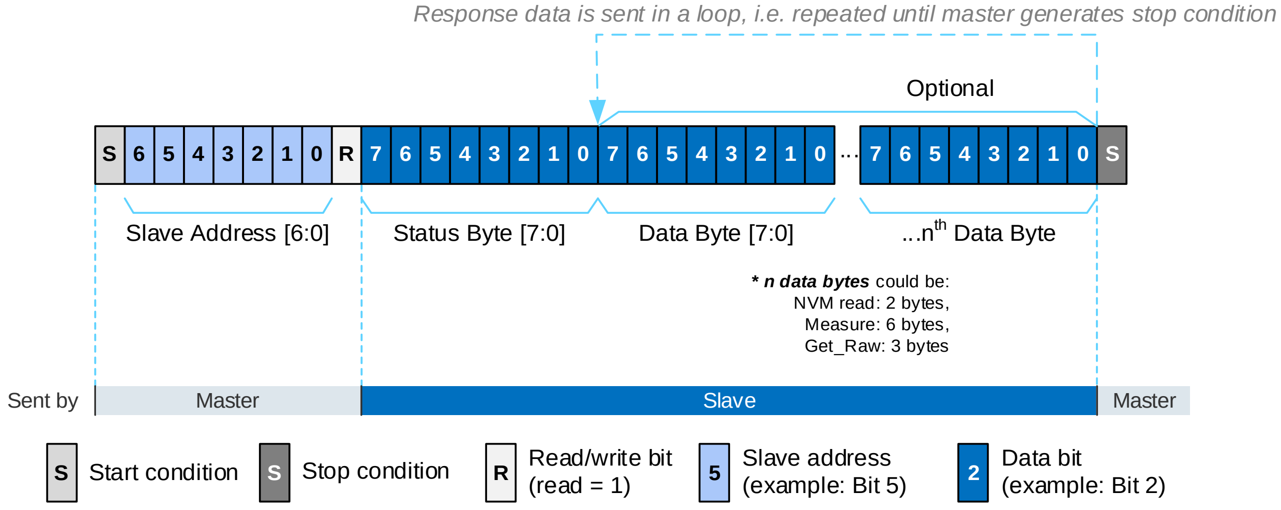


Figure 18. OWI Response by ZSSC3241

The ZSSC3241 allows utilization of the OWI interface in different application configurations:

- **OWI Disable:** The OWI interface can be deactivated by *owi_off* = 1 (bit[13] in *SSF1* register 03_{HEX}). For example, this could be applied in cases when an analog-output smart sensor is configured and calibrated using the OWI interface and the OWI will not be available after calibration and final setup/programming.
- **OWI Only (no analog output)**: With the NVM configuration *owi_off* = 0 and *cont_ANAoutn* = 1, the AOUT will not provide any analog outputs and is only used as the OWI pin. There is no startup window limitation (*owi_su_length* is ignored by the ZSSC3241). If the first (valid) digital interface activity is the *Startup OWI* ($D2_{HEX}$) command, the ZSSC3241's interface type will be fixed as OWI communication (SPI and I2C will be disabled/ignored).
- **OWI with Startup Window and Analog Output:** The OWI startup window followed by subsequent activation of the analog output is possible with *owi_off* = 0, *cont_ANAoutn* = 0, and *owi_su_case* = 0. AOUT works as a (listening) OWI signal pin after power-up until the selected startup window (*owi_su_length*) has elapsed. If the *Startup OWI* ($D2_{HEX}$) command is received within the startup window, AOUT persists as the OWI communication pin until a power-on reset occurs. If the ZSSC3241 does not receive the *Startup OWI* command ($D2_{HEX}$) during the startup window, the OWI interface will be disabled and AOUT starts functioning as an analog output.
- **Continuous OWI and Analog Output:** The configuration *owi_off* = 0, *cont_ANAoutn* = 0, and *owi_su_case* = 1 results in AOUT providing analog output levels as soon as they are available after power-up (in Cyclic Mode). Concurrently, the OWI listens to the AOUT [1] pin in order to check for valid OWI commands. The OWI still needs to be enabled by means of the *Startup OWI* command. The physical protocol in this configuration requires an extra pulse (see Figure 16) prior the *Startup OWI* command. After the release of the extra OWI initialization pulse, the analog output is switched off [2] and AOUT becomes the OWI I/O pin until the OWI startup window (according to *owi_su_length*) has elapsed.
  The OWI-master implements *Dynamic Driving* to avoid dynamic currents (due to DAC-output level changes) causing unwanted pull-up signal generation (via $R_{OWI,PULL}$). When *Dynamic Driving Approach* is not applied in this configuration, set the constantly connected OWI-master pull-up resistances ($R_{OWI,PULL}$) to ≥5.5kΩ to prevent erroneous OWI-start detections that can be triggered by changing DAC-output levels. Limit the interface speed to slower values with the proper setting, such as longer bit period.

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[1] Dependent on *Aout_setup*, OWI2 is the alternative input pin, e.g., in the case of the current loop setup, i.e. the *Aout_setup* bit field = 000 in register 04_{HEX}.

[2] The DAC switch-off time point is variable and depends on the activity status in the measurement cycle, measurement execution, etc. It can be anytime between the extra-pulse and a received, completed *Startup OWI* command.

6.5 Measurement and Output Options

Sensor or diagnostic measurement results of the ZSSC3241 can be provided in both domains, digital and analog. Any of the supported digital interfaces and output options can be used as the only active interaction path, or it can be combined with any of the analog output configurations. For digital communication, only one interface type can be active and supported (see section 6.4).

Digital communication via SPI and I2C are fully independent of the configuration and application of the ZSSC3241's analog outputs. For digital OWI communication combined with analog output, special application circuits and constraints might have to be considered, as the OWI interface and the analog outputs use the same pin, AOUT.

6.5.1. Single Measurements, Digital Raw Results, and SSC Results

The IC generates digital raw values, which are processed by the ZSSC3241 internal main math core generating the SSC-corrected (linearized, temperature-compensated) output signal. See section 6.6.3 for details about the SSC math, etc. In addition to the SSC-corrected digital measurement results, the ZSSC3241 can provide raw values without SSC correction for evaluation and/or calibration purposes. The respective results are provided at the digital interface as a 24-bit wide data word. Raw values and SSC results are MSB-aligned. Raw values are formatted as two's-complement, whereas SSC results are formatted as unsigned absolute value.

Table 25. Data Format of Raw ADC Readings

Bit-Number	23	22	21	20	…	2	1	0
Meaning, Weighting	-2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

Table 26. Data Format of Corrected, SSC Results (*S* and *T*)

Bit-Number	23	22	21	20	…	2	1	0
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

The ZSSC3241 can process and digitize the following signals:

- *SM:* Direct sensor signal inputs; i.e., perform sensor measurements
- *AZS:* Auto-zero signals for the sensor channel
- *TM:* Direct temperature signal inputs, i.e. perform temperature measurements
- *AZT:* Auto-zero signals for the temperature channel

The internal sequence (in time) of A2D-conversions with both auto-zero measurements enabled is: first is *AZS*, second is *SM*, third is *AZT*, and forth is *TM*. The utilization of auto-zero measurements allows further optimization and reduction of the noise level for the sensor signal in combination with the inherent compensation of the residual offsets of the analog sensor front-end. If an auto-zero measurement is enabled, then the sensor signal remains the input for the auto-zero measurement with the gain and ADC set up as for the original signal measurement, but with swapped inputs and offset configurations of the PGA and ADC such that the following holds for the resulting raw value:

- Sensor raw value with auto-zero: $S\_raw = 0.5 \cdot (SM - AZS)$
- Temperature raw value with auto-zero: $T\_raw = 0.5 \cdot (TM - AZT)$

The application benefits with enabled auto-zero measurements are

- ZSSC3241 front-end offset cancellation – residual signal degradation[1] or drift for the application is eliminated
- Improvement of the signal-to-noise ratio for the raw or SSC-corrected output signal

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[1] Worst-case IC-offset drift is < 2ppm/day at 125°C.

On the other hand, the default application benefit without auto-zero measurements is an approximately 50% faster output update rate compared to an equivalent configuration with enabled auto-zero measurements.

Recommendations: For applications where a faster update rate is the priority, disable and not apply the auto-zero measurements. For applications where a better signal-to-noise level and maximum signal quality are the priority, enable and apply the auto-zero measurements.

The NVM configuration and measurement-request commands can be used to select which measurements are performed, processed, and provided at the digital interface. See Table 34 for command details.

Examples of options for a single measurement request and output:

- SSC-corrected sensor readings (requested by the *Measure* command AA$_{HEX}$) generating an output of SSC-corrected, 24-bit sensor data followed by SSC-corrected, 24-bit temperature data.
- Raw sensor measurement with or without auto-zero correction (requested by the *Raw Sensor Measure* command A2$_{HEX}$) generating an output of raw 24-bit sensor data.
- Raw temperature measurement with or without auto-zero correction (requested by the *Raw Temperature Measure* command, A4$_{HEX}$) generating an output of raw 24-bit temperature data.

The auto-zero measurements can be disabled/enabled via the *AZMs_on* and *AZMt_on* bits in NVM registers 04$_{HEX}$ (see Table 35).

Table 27 and Table 28 provide some exemplary, typical conversion times and noise performance values for the ZSSC3241's Front-End (PGA and ADC) in order provide some guidance for understanding effects and signal-quality-related consequences while defining an application setup.

Table 27. Typical Conversion Times for Complete SSC Sensor Measurements: SM, TM

ADC Resolution (Main) Sensor	ADC Resolution Temperature Sensor	Typical Measurement Duration [ms] [a]
12	12 (external temperature sensor)	0.40
14	13 (internal temperature sensor)	0.49
14	14 (external temperature sensor)	0.55
16	14 (external temperature sensor)	0.69
16	16 (external temperature sensor)	0.82
18	18 (external temperature sensor)	1.42
24	24 (external temperature sensor)	9.49

[a] The time from the end of the SSC-measurement command request AA$_{HEX}$ to signalization for the end-of-conversion at the EOC pin with the ZSSC3241 in Command Mode; *INT_setup* bit field = 00$_{BIN}$ in register 02$_{HEX}$ (see Table 35); 25°C; V_{DD}=5V; *AZMs_on* = 0$_{BIN}$; and *AZMt_on* = 0$_{BIN}$.
The data is shown with ZSSC3241 default NVM configuration.

Table 28. Typical Conversion Times and Noise Performance for Complete SSC Measurements

ADC Resolution: External Sensor [Bits]	Reference Source for External Sensor (*sel_ref1*)	Typical 3-sigma Noise for SSC-Corrected (Digital) Output [b], *S*, *T*	Typical Measurement[a] Duration [c] [ms]
12	Absolute, *sel_ref1*=0	5 LSB$_{12Bit}$	0.8
12	Ratiometric, *sel_ref1*=1	7 LSB$_{12Bit}$	
16	Absolute, *sel_ref1*=0	26 LSB$_{16Bit}$	1.3
16	Ratiometric, *sel_ref1*=1	51 LSB$_{16Bit}$	
20	Absolute, *sel_ref1*=0	182 LSB$_{20Bit}$	2.9
20	Ratiometric, *sel_ref1*=1	270 LSB$_{20Bit}$	
24	Absolute, *sel_ref1*=0	1122 LSB$_{24Bit}$	9.8
24	Ratiometric, *sel_ref1*=1	1354 LSB$_{24Bit}$	

[a] Measurements including AZS, SM, AZT, TM with internal temperature measurement.

[b] Reference noise values normalized to the respective external sensor's ADC resolution, obtained with the following setup: 10kΩ sensor bridge, 25°C, Gain=28, VDD=3.3V, *ioffsc*=00000 for *sel_ref1*=1, *ioffsc*=01111 for *sel_ref1*=0, *adc_en_shift*=0, *pga_en_shift*=0, *sensor_sup*=00, *cp_off*=0.

[c] The time from the end of the SSC-measurement command request AA$_{HEX}$ to signalization for the end-of-conversion at the EOC pin with the ZSSC3241 in Command Mode; *INT_setup* bit field = 00$_{BIN}$ in register 02$_{HEX}$ (see Table 35).

6.5.2. Cyclic, Continuous, Repeated Measurements – Measurement Scheduler

In addition to single measurement requests, such as AA_{HEX}, or the *Oversample-x Measure* requests (AC_{HEX} to AF_{HEX}; see Table 34), the ZSSC3241 can be configured for cyclic measurement sequences. The continuously running measurement sequence consists of individual measurement slots in which all or a selectable subset of measurements and checks can be scheduled and allocated including sensor measurement (S), auto-zero measurement for the sensor (AZS), temperature measurement (T), auto-zero measurement for temperature (AZT), and diagnostic checks (see section 6.3). If AZS is enabled (*AZMs_on* = 1_{BIN} in register 04_{HEX}; see Table 35 for details for registers), the sensor measurement (S) and auto-zero measurement for the sensor (AZS) must be scheduled to always occur together for correct signal processing; i.e., these settings are required: *slots_S* = *slots_AZS* in register $1F_{HEX}$ and *startS_wfirstn* = *startAZS_wfirstn* in register $1E_{HEX}$. If AZT is enabled (*AZMt_on* = 1_{BIN} in register 04_{HEX}), the temperature measurement (T) and auto-zero measurement for temperature (AZT) must be scheduled to always occur together for correct signal processing; i.e., these settings are required: *slots_T* = *slots_AZT* and *startT_wfirstn* = *startAZT_wfirstn* (see registers $1E_{HEX}$ and $1F_{HEX}$). For applications where obtaining the fastest possible update rate is the highest priority, disabling the auto-zero measurements is recommended, i.e., *AZM*_on* = 0_{BIN}, for which slot scheduling is user programmable without constraints.

The automatically, continuously running measurement sequence is executed in Cyclic Mode, which is either entered as the default main operating mode after power-on or entered by means of the *START_CYC* command, AB_{HEX}.

Figure 19 shows an example of the measurement sequence configurability. During the pauses in the sequence, the ZSSC3241 signals that it is not busy (i.e., the *Busy?* bit = 0_{BIN} in the general status byte; see Table 19). The available measurement results are updated at the end of each SSC calculation and output operation and are kept valid at the digital interface or DAC output until the next SSC calculation and output operation.

The configuration of the measurement scheduler is done in the NVM registers $1E_{HEX}$ to 20_{HEX}.

Measurement example with the following requirements:

- S every slot, start with first
- No AZS (*AZMs_on* = 0_{BIN})
- T every 7 slots, start with first
- AZT every 7 slots, start with first
- Sensor Connection Check every 10 slots, no start with first slot

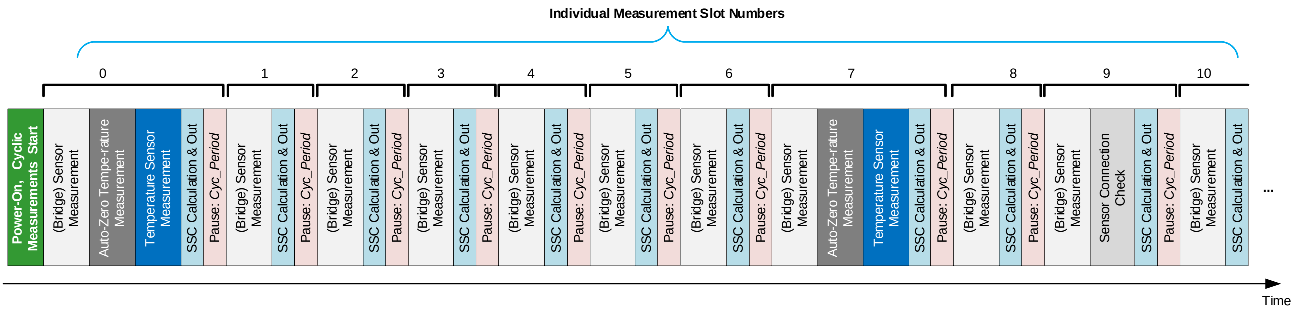


Figure 19. Example Configuration for the Measurement Scheduling and Cyclic Mode Operation

A slot denotes all measurements that are conducted and updated before the next SSC calculation. There can be pauses from one slot to the start of the next slot. The first slot has the slot number 0.

If the digital interface clock speed is too slow or contains long no-read pauses related to the SSC output update rate in Cyclic Mode, intermediate results can be lost.

In Cyclic Mode, the present data word (measurement result) at the interface output is always the latest data . See Figure 20 for relatively slow interface polling compared to the internal measurement data update rate in Cyclic Mode.

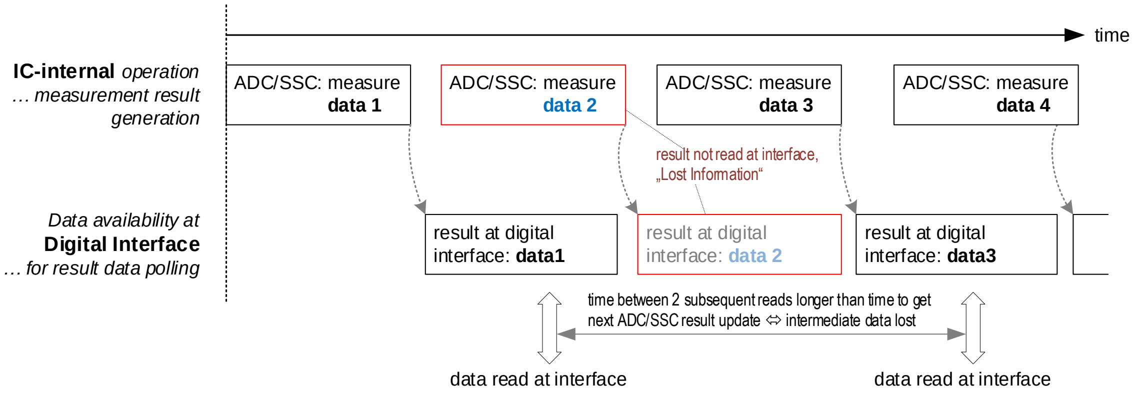


Figure 20. Measurement Result Output Update in Cyclic Operation (with “Slow” Interface Polling)

Note: When a mode change request (START_CM, START_SLEEP) is received relatively close to the IC internal output register update in Cyclic Mode, the request is acknowledged and the latest measurement result generated during the cyclic operation may not be present at the interface. It is recommended to read out the last measurement result directly before the mode change.

6.5.3. Analog Outputs: Digital-to-Analog Converter (DAC)

The integrated, programmable digital-to-analog converter (DAC) generates an IC-internal analog signal that can be output at AOUT as an absolute voltage, V_{DD}-ratiometric voltage, or control signal for an externally connected current loop circuit. The analog output must be configured by *Aout_setup* in the *SSF2* register, 04_{HEX}.

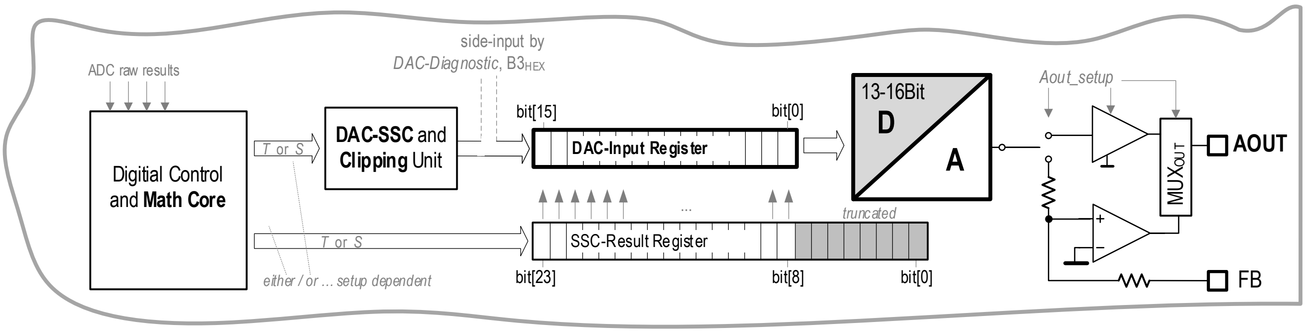


Figure 21. DAC and Analog Output Topology

The ZSSC3241 provides only analog outputs for signals that are processed by the SSC calculation unit (see section 6.6.3), that are post-processed by the DAC-SSC correction and Clipping unit, or that are directly transferred (via the digital command, *DAC-Diagnostic*, $B3_{HEX}$; see Table 34) as input to the DAC; e.g., for test or calibration purposes. The setup parameter *dacouttype*, bit[3] of the *SSF2* register, 04_{HEX} defines if either the SSC-corrected sensor value, *S*, or the SSC-corrected temperature value, *T*, is provided at AOUT; see Figure 21.

Table 29. DAC Configurations

dacres		Applied DAC Resolution	Maximum DAC Output Voltage $t_{DACsettle}$ Settling Time [a]
bit[1]	**bit[0]**		
0	0	13-Bit	150µs
0	1	14-Bit	160µs
1	0	15-Bit	180µs
1	1	16-Bit	200µs

[a] $t_{DACsettle}$ is the step-response time for the DAC and analog output stage (only); i.e., the time to reach 99% of the new analog output level after a DAC input change. For analog-output smart-sensor step-response time, the time for generating a new SSC-result as input to the DAC must also be considered.

For the suppression of spuriously emitted tones in the analog output signal, dithering within the DAC operation can be enabled/disabled via the *dither_off* bit in the *SSF2* register. If spurious tone emission is irrelevant in the application, dithering can be switched off in order to improve the analog output signal's noise level.

For analog diagnostic level signalization, enabled by the *diagouten* bit = 1_{BIN} in the *SSF2* register (see Table 17), the ZSSC3241 directly ties the analog output signal to 0% or 100% with the selected output stage, supported by digital pre-scaling to reserve approximately 1.5%-wide signal bands for diagnostic outputs. Strong recommendation: If the ZSSC3241 provides diagnostic levels, activate analog signalization of diagnostic levels before sensor calibration.

6.5.3.1. Programmable Clipping Limits for the Digital-to-Analog Converter

The DAC allows programming a lower and upper clipping limit (*Low_Clip_Lim* and *Up_Clip_Lim* bit fields respectively; see Table 35) for the output signal. The main SSC-corrected output value (sensor signal *S* or temperature signal *T* – selectable by *dacouttype* bit) is compared against the 16-bit value formed by {*Up_Clip_Lim*[15:0],00000000_{BIN}} for the upper limit and against {*Low_Clip_Lim*[15:0],00000000_{BIN}} for the lower limit. If the calculated bridge value is higher than the upper limit or less than the lower limit, the analog output value is clipped to this limit value, see Figure 21.

The high/low-clipping functions can be enabled by the *clipping_on* bit field in the NVM-register 24_{HEX}.

The enabled clipping function is not applied (regardless on the setup in *clipping_on*) in the following cases:

- if the DAC-Diagnostic command $B3_{HEX}$ is used to force a certain DAC-output
- if enabled diagnostic checks (*diagouten*=1_{BIN}) detected a Diagnostic State, that is signalized at the AOUT pin, see Table 17.

The clipping is performed in the same sub-block of the IC as the separate correction of the Digital-to-Analog converter characteristic (DAC-SSC), see section 6.6.3.3. DAC-SSC can be applied to allow for post-main-SSC correction of a gain and offset factor allowing the compensation of the typical DAC-characteristic. A digital output signal that covers the complete dynamic range can be mapped to a lower DAC output dynamic range by the DAC-SSC function, for example, to reserve low and upper DAC output voltage bands for diagnostic state signalization.

6.5.3.2. Voltage Outputs

The ZSSC3241 can provide one of three direct voltage outputs at the AOUT pin. The *Aout_setup* bit field in the *SSF2* register (bits [7:5]; see Table 35) is used to configure the ZSSC3241 and select the analog voltage output stage as defined in Table 30. It is also possible to set up the analog voltage output for 0V to 10V systems using additional external components.

Table 30. Direct Voltage Outputs

Aout_setup			**Voltage Output (Range/Type)** [a]	**Comments**
bit[2]	**bit[1]**	**bit[0]**		
0	0	0	–	Current loop; see section 6.5.3.4
0	0	1	0 to V_{DD}, ratiometric	Typical 0 to 5V; with V_{DD} > 5V, rail-to-rail output
0	1	0	0 to 1V, absolute	Any (valid) V_{DD}
0	1	1	0 to 5V, absolute	Requires V_{DD} > 5.01V
1	0	0	–	Not assigned
1	0	1	0 to V_{DD}, ratiometric	Typical 0 to 5V; with V_{DD} > 5V, rail-to-rail output, $OWI2_{in}$ enabled as OWI input pin
1	1	0	0 to 1V, absolute	Any (valid) $V_{DD,}$ $OWI2_{in}$ enabled as OWI input
1	1	1	0 to 5V, absolute	Requires V_{DD} > 5.01V, $OWI2_{in}$ enabled as OWI input

[a] The voltage outputs listed are directly supported, requiring minimal (for ratiometric output) or no (for absolute voltage output) additional external devices.

Table 31. Recommended Operating Conditions for Voltage Output

Symbol	Parameter	Typical Value	Unit	Comments
R_{Lout}	External, resistive load at AOUT	1	kΩ	For 1kHz to 5kHz output bandwidth, as RC low-pass filter configuration.
C_{Lout}	External, capacitive load at AOUT	10	nF	

6.5.3.3. Accuracy and Calibration of the DAC-Output

The 16-bit-DAC of ZSSC3241 is optimized from design prospective for high stability. Low drift over operational conditions can be achieved with minimal additional effort during the calibration phase, by compensating absolute errors/mismatches with mathematical adaptation of sensor calibration coefficients.

The functional, analog main-components of the ZSSC3241's DAC come with some residual level of IC-to-IC variation for DAC-characteristic's offset and gain. It is recommended to calibrate the DAC-characteristic and consider the linearity IC-to-IC-variation of the DAC at the IC's calibration, especially for applications with high requirements for absolute accuracy of the output voltage. For analog output configurations, the SSC coefficients can be derived such that the digital SSC-results and hence the DAC's digital input (*S* or *T*) is pre-shaped in order to compensate the residual DAC's (non-)linearity variation.

To avoid taking analog measurement values during the smart sensors' calibration procedure, the ZSSC3241 provides two high-precision DAC-calibration point measurement results in the NVM, *DAC10RM5V* and *DAC90RM5V* in the NVM registers 22_{HEX} and 23_{HEX}, see Table 35. Using these two high-precision DAC calibration points for the determination of the SSC-coefficients, the ZSSC3241 achieves a low residual, absolute DAC-output error of less than ±0.15% over the device specified temperature range, and over the DAC output swinging from 1% to 100% of the specified range. This approach can be also interpreted as mapping of the digital SSC-outputs (*S* or *T*) to an IC-to-IC-varying best fit straight-line characteristic of the DAC. The residual DAC-error is typically higher in the signal range 0% to 1%, as the ZSSC3241's does not provide exactly 0V for zero-value digital DAC-inputs, *S* or *T*.

If more than two DAC-calibration points are considered, absolute accuracies below ±0.15% become possible, down to the analog output (AOUT) line's noise-and-distortion level.

6.5.3.4. Current Loop Output

The analog current loop is a typical output signal configuration, especially for industrial sensors. Using only two wires, the sensor is supplied with power and transmits its output signal to the processing unit. With *Aout_setup* = 000_{BIN} (bits [7:5] in the *SSF2* register; see Table 35), the ZSSC3241 will generate a SSC-corrected sensor-signal-proportional control signal at AOUT that allows generating a related loop current according the application in Figure 22.

Table 32. ZSSC3241 Current-Loop-Specific Properties

Symbol	Parameter	Typical Value	Unit	Comments
R_1	Control feedback resistor, internal	120	kΩ	Combined with external R_{SENS}, defines the current-loop gain: R_1/R_{SENS} R_1-process-variation in the range of ±20%
R_{SENS}	External loop-sensing resistor	50	Ω	Using a low-TC resistor is recommended to minimize spurious temperature influence
β_{TLOOP}	Current gain of external-loop bipolar transistor, T_{LOOP}	100	Numeric	
BW_L	Transfer bandwidth of internal current loop op amp.	20	kHz	
$R_{SENSOR,MIN}$	External sensor element's minimum resistance	1.6	kΩ	With a ratiometric supply and resistances that are too low, the overall current consumption ($I_{Sensor} + I_{IC}$) at V_{DD} could exceed the 4mA low-limit for typical current loops (see Table 3 for I_{Sensor} specifications, and see Table 4 for I_{IC} specifications)
$I_{Loop,high}$	Loop-response current for logical-1; OWI over current-loop	20…24	mA	Effective current modulation when ZSSC3241 is OWI slave modulating the slave-to-master response via the

Symbol	Parameter	Typical Value	Unit	Comments
$I_{Loop,low}$	Loop-response current for logical-0; OWI over current-loop	7…11	mA	loop current (controlled by AOUT/OWI1), including IC-active-current draw, I_{IC} and (typ.) 1mA load through the sensor element, $R_{e,Tloop}$~150Ω

Strong recommendation: Use the Zener diode between FB and VDD to protect the V_{DD} line from positive over-voltage conditions and protect the FB input from negative over-voltages. The 100nF capacitor performs a low-pass-filter function for short/fast changes in the total current consumption for the sensor element plus the ZSSC3241 (I_{SENS} + I_{IC}), such that current consumption changes do not lead to short-term fluctuations of AOUT and the loop current.

An equivalent effect of slight loop current fluctuations might be observable if a sensor-connection check is sometimes executed between the normal sensor measurements. Here, the connected sensor element, e.g., a resistive bridge, will be unsupplied briefly in order to determine the electrical connection properties; whereas an overall load change (sensor measurements → sensor-connection check → sensor-measurement) at V_{DD} and hence in the current loop will be present. Therefore, diagnostic features should be carefully enabled and selected for current loop applications that have strong requirements for output signal quality under any circumstances.

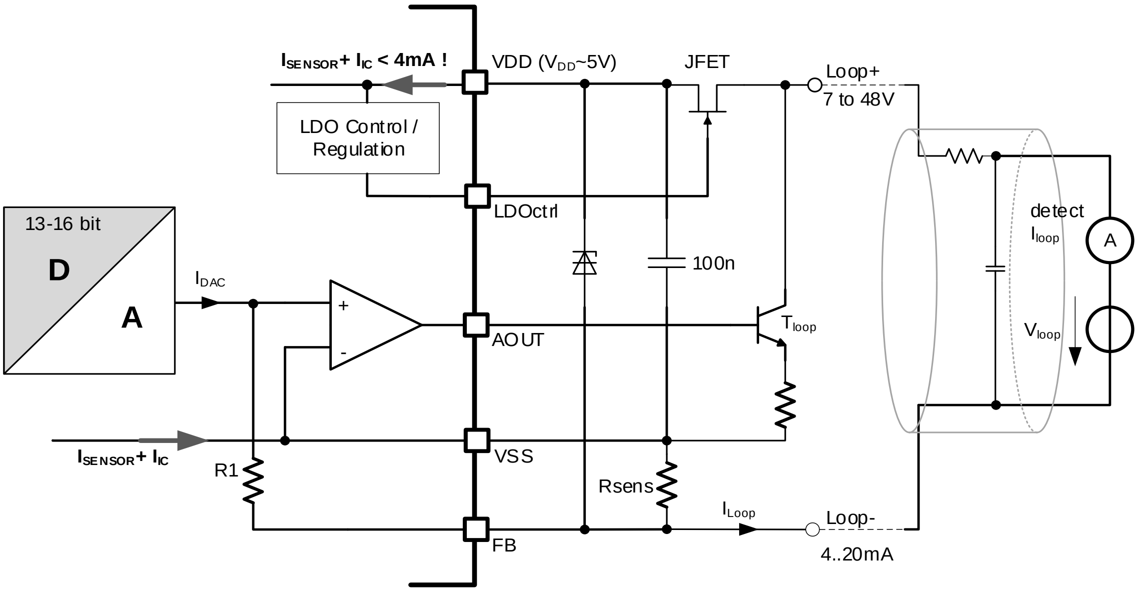


Figure 22. Current Loop Configuration

6.5.4. Output Interrupt Signaling

The EOC pin can be programmed to operate either as a simple “measurement busy” and end-of-conversion transducer or as a configurable interrupt transducer, which is configured using the *INT_setup*[1:0] bits in NVM register 02_{HEX}, bits[8:7]. Further, one or two 24-bit quantized thresholds without threshold-hysteresis (*eoc_hyst_on*=0_{BIN}) can be programmed via *TRSH1a* and *TRSH2a* (*Interrupt Level Setup* registers 18_{HEX}, 19_{HEX} and $1A_{HEX}$ in NVM; see Table 35). Depending on the *INT_setup* selection, the EOC pin provides a logic 1 or logic 0 (also dependent on the respective interface setup; e.g., SPI with either logic 0 = V_{DD} or logic 0 = V_{SS}, etc.) according to the SSC-corrected measurement result. The respective thresholds must be programmed left-aligned in the memory with the threshold’s MSB in the memory register’s MSB, etc. The LSBs of the 24-bit threshold in memory are ignored depending on the number of bits of the ADC resolution as selected with *adc_bits* (see Table 10).

The programmable pre-selection *eoc_hyst_on*=0_{BIN}, enables the consideration of further hysteresis thresholds: *TRSH1b* and *TRSH2b* which are programmed in the NVM-registers 27_{HEX}, 28_{HEX} and 29_{HEX}. The corresponding threshold consideration by the IC and the resulting EOC output behavior depend on the setup in *INT_setup*.

Figure 23 to Figure 26 illustrate the EOC behaviors and their respective selection setup based on *eoc_hyst_on*, *INT_setup*, *TRSH1a* and *TRSH2a*.

With *INT_setup* = 00_{BIN}, only the effective end-of-conversion is signalized. The EOC signal is a pulse of approximately 5µs (see Figure 23). The next command will be executed only after this EOC signaling period.

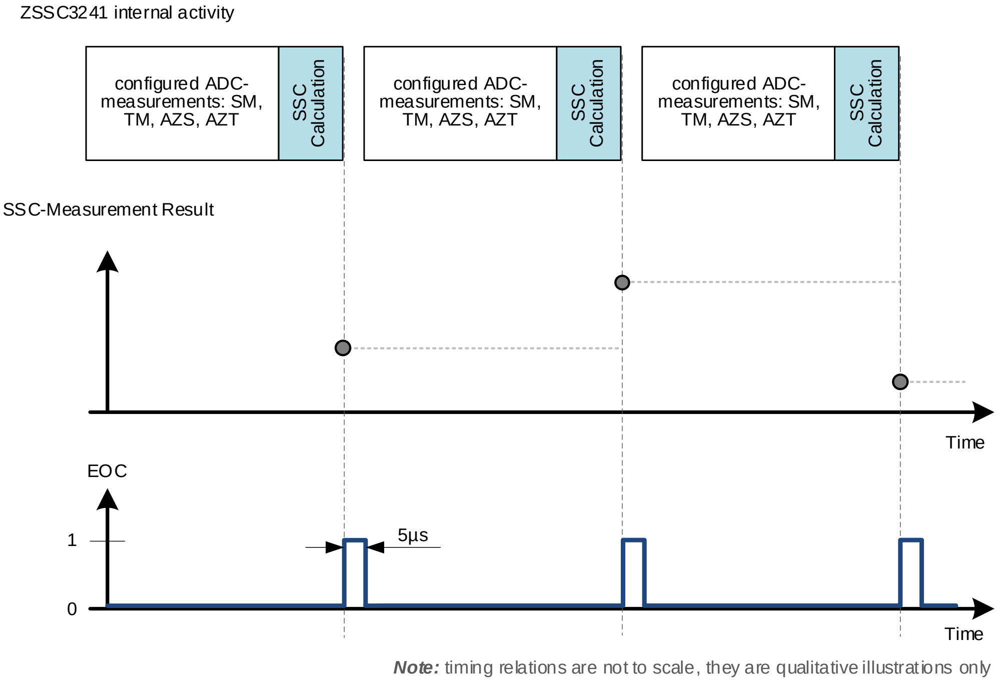


Figure 23. EOC-Behavior: Signalization of End-of-Conversion (*INT_setup* = 00_{BIN})

The interrupt functionality is only available for digital values from the SSC-calculation unit. The interrupt feature cannot monitor raw values. The encoding and data format of the interrupt thresholds is the same as for SSC-corrected measurement results (see Table 33).

Table 33. Data Format of Interrupt Thresholds (TRSH1a, TRSH1b, TRSH2a and TRSH2b)

Bit-Number	**23**	**22**	**21**	**20**	**…**	**2**	**1**	**0**
Meaning, Weighting	2^{0}	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

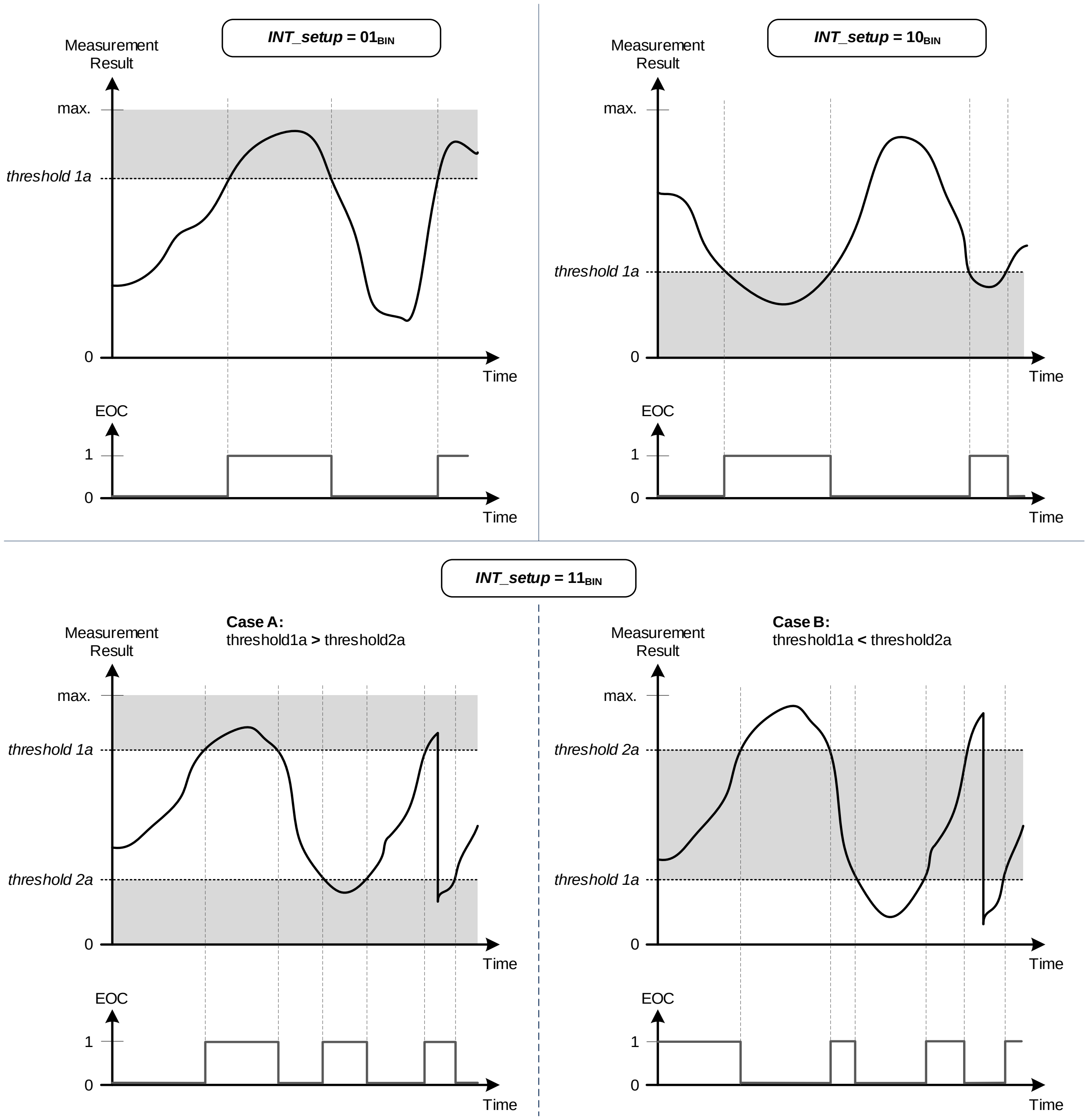
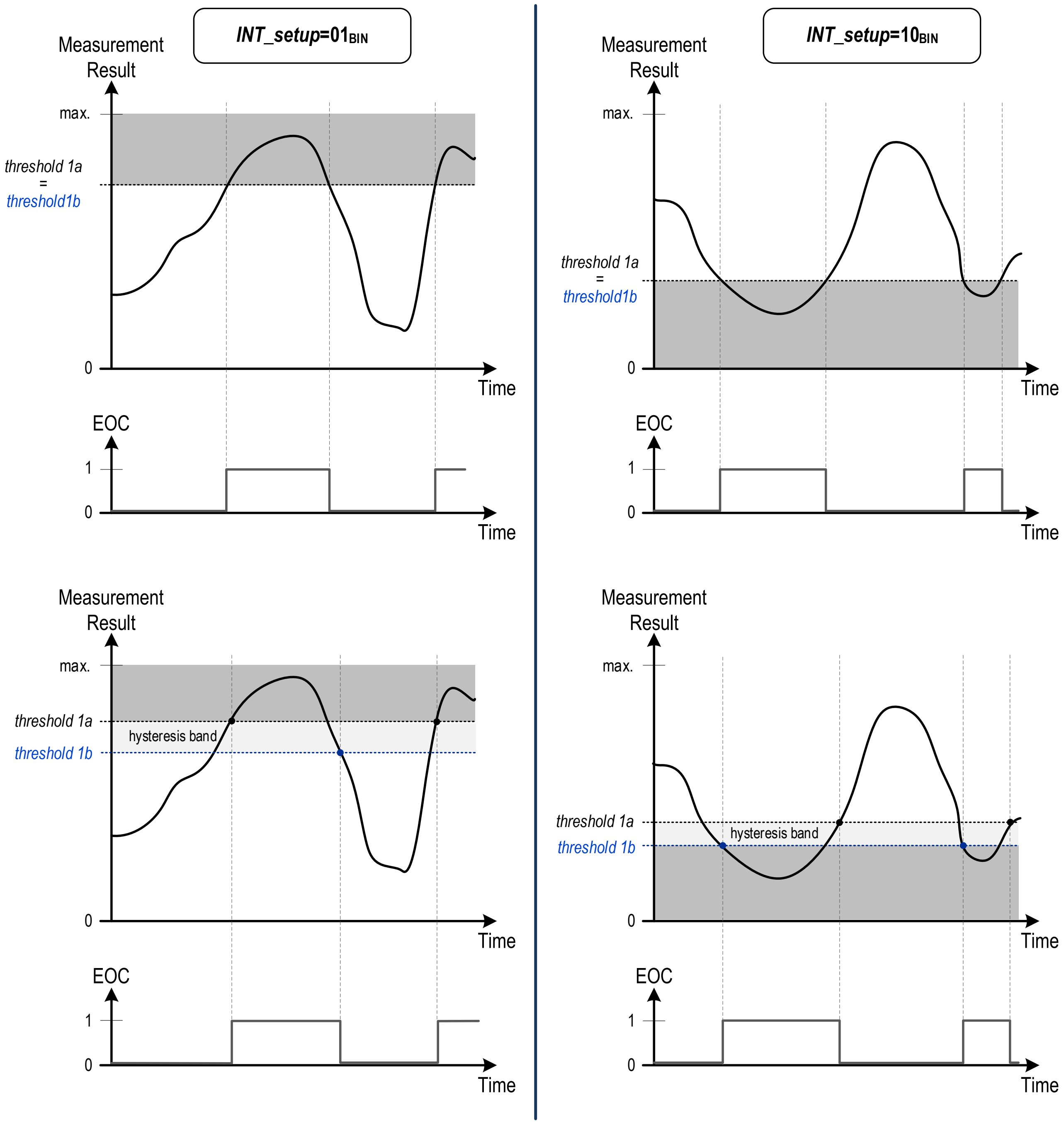
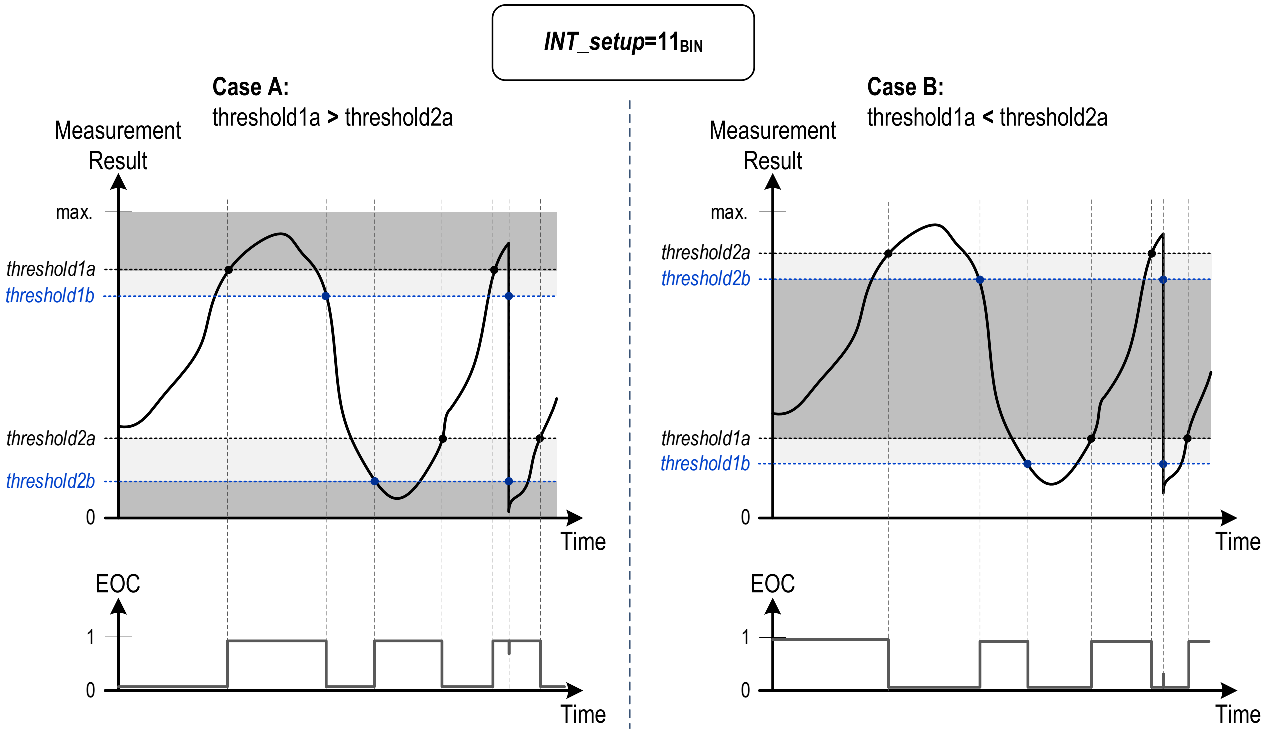


Figure 24. EOC and Interrupt Thresholds without Hysteresis (*eoc_hyst_on*=0_{BIN})



Always ensure that *threshold1b* ≤ *threshold1a*

Figure 25. EOC and Single-Interrupt Thresholds with Hysteresis (*eoc_hyst_on*=1_{BIN})



Always ensure that: *threshold1b* ≤ *threshold1a* and *threshold2b* ≤ *threshold2a*

Figure 26. EOC and Dual-Interrupt Thresholds with Hysteresis (*eoc_hyst_on*=1$_{BIN}$)

6.6 System Setup and Control

The digital blocks of the ZSSC3241 are organized functionally as shown in Figure 27. In addition to the central blocks, which are the “Interfaces,” “Digital Main Core,” and “Memory (NVM)” blocks, there is also the Shadow Registers block, which in most cases, is a direct copy of the NVM registers. The shadow registers are loaded from NVM during the power-up sequence and allow acceleration of command processing and NVM-independent configuration adaptability; e.g., during adaptive sensor setup, evaluation, or smart sensor test. For the main function of the ZSSC3241 to conduct a sensor measurement and ADC-conversion, the setups (for main Sensor or Temperature) are loaded or activated from the corresponding Shadow Registers in order to set all IC-internal configuration switches for sensor supply, PGA gain, offset compensation, reference voltage sources, etc. After a settling time for the analog signals and levels, the A2D conversion takes place. This course of activities is (re-)done for each individual measurement, i.e. once for SM, AZS, TM, AZT, with setups for SM and AZS according the Shadow Registers for *SM_config1* and *SM_config2*, and for TM, AZT from registers *extTemp_config1* and *extTemp_config2*. If the internal temperature sensor was selected as signal source for TM, AZT, the setups are loaded from a Renesas-preprogrammed register different to *extTemp_config1* and *extTemp_config2*.

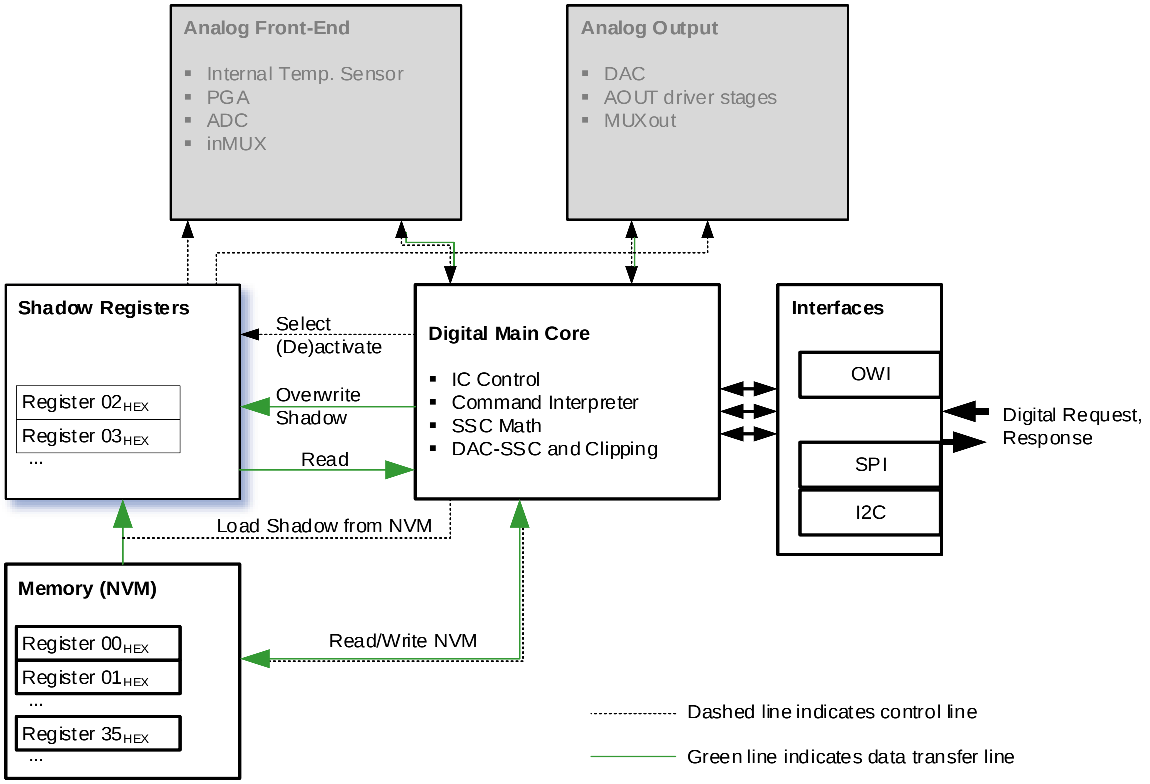


Figure 27. Digital IC Section Architecture

6.6.1. Digital Commands

The availability of commands depends on the active main operating mode: Command, Sleep, or Cyclic Mode.

Table 34. Command List

Note: See important table notes as the end of this table.

Command Code (Byte)	Return	Description	Available in Sleep Mode	Available in Command Mode	Available in Cyclic Mode
00_{HEX} to $3F_{HEX}$	16-bit data	**Memory Read** address 00_{HEX} to $3F_{HEX}$	Yes	Yes	No
40_{HEX} to 75_{HEX} followed by data (0000_{HEX} to $FFFF_{HEX}$)	–	**Memory Write** addresses 00_{HEX} to 35_{HEX} (NVM register address is command minus 40_{HEX}); if the NVM is locked, write requests are not acknowledged or are ignored	Yes	Yes	No
90_{HEX}	–	**Calculate NVM Checksum** and write it to the memory	Yes	Yes	No
$A2_{HEX}$	24-bit raw data	**Raw Sensor Measurement** [a] – Configuration is loaded in the controlling shadow registers from the *SM_config1* and *SM_config2* registers in NVM *Note:* auto-zero sensor measurement is performed if set up in the *AZMs_on* bit in the *SSF*2 register	Yes	Yes	No

Command Code (Byte)	Return	Description	Available in Sleep Mode	Available in Command Mode	Available in Cyclic Mode
A4$_{HEX}$	24-bit raw data	**Raw Temperature Measurement** [a] – Configuration is loaded in the controlling shadow registers from the *extTemp_Config1/2* or *T_config1/2* registers in NVM as well as the *SSF1/2* registers Note: Auto-zero correction will be performed if set up via the *AZMt_on* bit in the SSF2 register Note: If a raw data measurement with an external setup (different from the NVM content) will be performed, then pre-load the measurement configuration via the *Overwrite SSF1/2 Register* and *Overwrite T_config1/2 Shadow Register* commands. Note: The internal or external temperature measurement will be performed if set up via the *temp_source* bit field in the *SSF1* register	Yes	Yes	No
A8$_{HEX}$	–	**START_SLEEP** – Exit Command Mode or Cyclic Mode and transition to Sleep Mode Note: The response to *Start_Sleep* is only the status byte	No	Yes	Yes
A9$_{HEX}$	–	**START_CM** – Exit Sleep Mode or Cyclic Mode and transition to Command Mode	Yes	No	Yes
AA$_{HEX}$	24-bit SSC-corrected sensor data and 24-bit SSC-corrected temperature data	**Measure** – Trigger a full measurement (auto-zero-sensor, sensor, auto-zero-temperature, temperature) and perform SSC correction Note: Auto-zero correction is performed with this command if set up in the *AZMs_on* and *AZMt_on* bits in the *SSF2* register	Yes	Yes	No
AB$_{HEX}$	–	**START_CYC** – Enter the Cyclic Mode: continuous measurement cycles, SSC corrections, and automatic, continuous digital and/or analog output updates	Yes	Yes	No
AC$_{HEX}$	24-bit SSC-corrected sensor data and 24-bit SSC-corrected temperature data	**Oversample-2 Measure** [b] – Mean value generation; 2 full measurements (triggered similar to AA$_{HEX}$, not cyclic) are performed and the resulting mean value is provided as output Note: Auto-zero correction is performed with this command if set up in the *AZMs_on* and *AZMt_on* bits in the *SSF2* register	Yes	Yes	No
AD$_{HEX}$		**Oversample-4 Measure** [b] – Mean value generation; 4 full measurements (triggered similar to AA$_{HEX}$, not cyclic) are performed and the resulting mean value is provided as output Note: Auto-zero correction is performed with this command if set up in the *AZMs_on* and *AZMt_on* bits in the *SSF2* register	Yes	Yes	No
AE$_{HEX}$		**Oversample-8 Measure** [b] – Mean value generation; 8 full measurements (triggered similar to AA$_{HEX}$, not cyclic) are performed and the resulting mean value is provided as output Note: Auto-zero correction is performed with this command if set up in the *AZMs_on* and *AZMt_on* bits in the *SSF2* register	Yes	Yes	No
AF$_{HEX}$		**Oversample-16 Measure** [b] – Mean value generation; 16 full measurements (triggered similar to AA$_{HEX}$, not cyclic) are performed and the resulting mean value is provided as output Note: Auto-zero correction is performed with this command if set up in the *AZMs_on* and *AZMt_on* bits in the *SSF2* register	Yes	Yes	No
B0$_{HEX}$	16-bit diagnostic result data	**CHECK_DIAG** – The ZSSC3241 responds with the detailed fault-result status in the *diagnosticreg* register	Yes	Yes	No

Command Code (Byte)	Return	Description	Available in Sleep Mode	Available in Command Mode	Available in Cyclic Mode
B1$_{HEX}$	–	**RESET_DIAG** – Resets the contents of *diagnosticreg* to 00$_{HEX}$	Yes	Yes	No
B2$_{HEX}$	–	**Update_DIAG** – Causes a complete diagnostics check cycle including memory CRC calculation, etc., and results in a reset and update of *diagnosticreg* Note: If a measurement cycle is running concurrently, the diagnostic update happens after completion of the measurement cycle and SSC calculations (and might delay the next cyclic measurement cycle)	Yes	Yes	No
B3$_{HEX}$ followed by data (0000$_{HEX}$ to FFFF$_{HEX}$)	–	**DAC Diagnostic** – Set the DAC output register with the data in the command and enable/output the respective analog signal through AOUT (according to the *AOUT_setup*) Note: The DAC output can be switched off by the RESQ pin, POR, or a change in the main operating mode	No	Yes	No
B4$_{HEX}$ followed by 00XX$_{HEX}$	24-bit raw data	**Self-Diagnostic Measure** – The ADC performs a raw measurement with the setup from the *SM_config* registers, and the PGA input is disconnected from the external sensor and internally shorted (INN = INP = AGND). The ZSSC3241-internal setup, which is configured according to the *ioffsc* bit field in the *SM_config*2 register, is changed to XX$_{HEX}$ (transmitted with the command). The respective pseudo-offset signal becomes the input test signal to the PGA-ADC-path. The original *ioffsc* and *SM_config*2 contents are restored after the self-diagnostic measurement completion. *Note*: alternatively, also a changed setup (PGA, ADC) could be used by applying *Overwrite* commands prior to the self-diagnostic measurement.	No	Yes	No
D1$_{HEX}$ followed by XXXX$_{HEX}$	–	**Set Post-Calibration Offset** – Set recent SSC-output to expected value XXXX$_{HEX}$ in command by means of offset adjustment with coefficient *SENS_shift*	Yes	Yes	No
D2$_{HEX}$	–	**Startup OWI** – Initialization command to enter OWI interface operation; only valid for OWI (see section 6.4.3)	Yes	Yes	Yes
D6$_{HEX}$ followed by data (0000$_{HEX}$ to FFFF$_{HEX}$)	–	**Overwrite *SM_config*1 shadow register** – Content (originally from NVM register 14$_{HEX}$) in the digital shadow register for *SM_config1* is directly overwritten with the command data [c]	No	Yes	No
D7$_{HEX}$ followed by data (0000$_{HEX}$ to FFFF$_{HEX}$)	–	**Overwrite *SM_config*2 shadow register** – Content (originally from NVM register 15$_{HEX}$) in the digital shadow register for *SM_config*2 is directly overwritten with the command data [c]	No	Yes	No
D8$_{HEX}$ followed by data (0000$_{HEX}$ to FFFF$_{HEX}$)	–	**Overwrite *T_config*1 shadow register** – Content (originally from NVM register 16$_{HEX}$ or 3C$_{HEX}$) in the digital shadow register for the temperature measurement is directly overwritten with the command data [c]	No	Yes	No
D9$_{HEX}$ followed by data (0000$_{HEX}$ to FFFF$_{HEX}$)	–	**Overwrite *T_config*2 shadow register** – Content (originally from NVM register 17$_{HEX}$ or 3D$_{HEX}$) in the digital shadow register for the temperature measurement is directly overwritten with the command data [c]	No	Yes	No

Command Code (Byte)	Return	Description	Available in Sleep Mode	Available in Command Mode	Available in Cyclic Mode
DA_{HEX} followed by data (0000_{HEX} to $FFFF_{HEX}$)	-	**Overwrite *SSF1* shadow register** – Content (originally from NVM register 03_{HEX}) n the digital shadow register for *SSF1* is directly overwritten with the command data [c] Note: transferred bits[1:0] and bits[15:13] are ignored; i.e., are not overwritten in the shadow register	No	Yes	No
DB_{HEX} followed by data (0000_{HEX} to $FFFF_{HEX}$)	-	**Overwrite *SSF*2 shadow register** – Content (originally from NVM register 04_{HEX}) the digital shadow register for *SSF*2 is directly overwritten with the command data [c]	No	Yes	No
FX_{HEX}	Status followed by last 24-bit data	**NOP** – Output of read results; only valid for SPI (see section 6.4.1)	Yes	Yes	Yes

[a] These commands can be used to conduct a measurement without an SSC correction; e.g., during the smart sensor calibration procedure. No digital correction is performed on the measurement result. The setup and configuration for the raw measurement is the content in the shadow registers that can be pre-loaded (automatically loaded during power-on) from the NVM or by means of the *Overwrite* commands, $D6_{HEX}$ to DB_{HEX}.

[b] Use *Oversample* measurements to obtain noise-minimized measurement results in Sleep or Command Mode. With higher oversampling factors, the command execution time increases proportionally.

[c] *Overwrite* commands can be used to optimize evaluation and test routine execution time for analog front-end setup or to configure self-diagnostic measurement setups without needing to change the ZSSC3241's NVM content. The content and effects from *Overwrite* commands are cleared and reset with the ZSSC3241 reset via the RESQ pin or POR.

6.6.2. Nonvolatile Memory (NVM)

In the ZSSC3241, the memory is organized in 16-bit wide registers and can be programmed multiple times (approximately 10000). There are 54 × 16-bit registers available for customer use. Each register can be re-programmed.

Basically, there are two NVM content sectors:

- Customer Use: Accessible via regular write operations: 40_{HEX} to 75_{HEX}. This sector contains the customer ID, interface setup data, measurement setup information, calibration coefficients, analog output configuration, etc.
- Renesas Use: Only accessible for write operations by Renesas. This sector (36_{HEX} to $3F_{HEX}$) contains specific trim information and is programmed during manufacturing test by Renesas, e.g. setups for the internal temperature sensor are stored there.

The whole NVM can be locked by programming *lock* = 1_{BIN} in the *SSF1* register, NVM address 03_{HEX}, bit[14]. No change of the NVM content is possible once the NVM lock has been activated.

Recommendations when using the NVM lock:

- Write all required setups, configurations, and SSC coefficients to the NVM first.
- Then write the *SSF1* register content with the *lock* bit set.
- Then trigger the generation and writing of the CRC via the *Calculate NVM Checksum* command, 90_{HEX}.

The NVM lock will be effective after a ZSSC3241 reset with POR or RESQ.

6.6.2.1. Memory Contents

Table 35. Memory (NVM) Content Assignments

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
00_{HEX}	15:0	0000_{HEX}	Cust_ID0	Customer ID byte 0 (combines with memory word 01_{HEX} to form customer ID)[a]
01_{HEX}	15:0	0000_{HEX}	Cust_ID1	Customer ID byte 1 (combines with memory word 00_{HEX} to form customer ID).
Interface Configuration				
02_{HEX}	6:0	000 0000_{BIN}	Slave_Addr	I2C and OWI slave address; valid range: 00_{HEX} to $7F_{HEX}$ (default: 00_{HEX}). Note: address codes 04_{HEX} to 07_{HEX} are reserved for entering the I2C High Speed Mode.
	8:7	00_{BIN}	INT_setup	Interrupt configuration, EOC pin functionality (clipping_on = 00_{BIN}): 00 = End-of-conversion signal 01 = 0 to 1 transition if threshold1a (*TRSH1a*) is exceeded and 1 to 0 transition if threshold1a is underrun again 10 = 0 to 1 transition if threshold1a is underrun and 1 to 0 transition if threshold1a is exceeded again 11 = EOC is determined by threshold settings (see section 6.5.4): • If (*TRSH1a* > *TRSH2a*) then EOC/INT (interrupt level) = 0 if (*TRSH1a* > MEAS ≥ *TRSH2a*) where MEAS is the conditioned measurement result. Otherwise EOC/INT = 1. • If (*TRSH1a* ≤ *TRSH2a*) then EOC = 1 if (*TRSH1a* ≤ MEAS < *TRSH2a*). Otherwise EOC = 0.
	9	0_{BIN}	SS_polarity	Determines the polarity of the Slave Select pin (SS) for SPI operation: 0 = Slave Select is active low (SPI and ZSSC3241 are active if SS==0) 1 = Slave Select is active high (SPI and ZSSC3241 are active if SS==1)
	11:10	00_{BIN}	CKP_CKE	Clock polarity and clock-edge select. *CKP_CKE* determines polarity and phase of SPI interface clock with the following modes: 00 = SCLK is low in idle state; data latch with rising edge and data output with falling edge 01 = SCLK is low in idle state; data latch with falling edge and data output with rising edge 10 = SCLK is high in idle state; data latch with falling edge and data output with rising edge 11 = SCLK is high in idle state; data latch with rising edge and data output with falling edge
	14:12	000_{BIN}	CYC_period	Update period in cyclic operation: 000 = 0.0ms 001 = 0.1ms 010 = 1.0ms 011 = 2.5ms 100 = 5.0ms 101 = 10ms 110 = 50ms 111 = 87.5ms Note: A slower measurement rate, i.e., a higher *CYC_period,* can improve the analog output signal quality due to lower system bandwidth.
	15	0_{BIN}	SOT_curve	Type/shape of second-order curve correction for the sensor signal: 0 = Parabolic curve 1 = S-shaped curve
Smart Sensor Feature Configuration Register 1 (SSF1)				
03_{HEX}	1:0	00_{BIN}	default_mode	Defines the default operating mode that is automatically entered after power-on: 00 = Command Mode 01 = Cyclic Mode 10 = Sleep Mode 11 = Not assigned

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
	2	0_{BIN}	owi_su_length	Defines the length of the OWI startup window, during which the OWI interface can be activated if analog output through the AOUT pin is also set up via *cont_ANAoutn* = 0_{BIN} (see register 04_{HEX}). OWI_ListenTime: 0 = 50ms 1 = 3ms
	3	0_{BIN}	owi_su_case	Defines the activation level for the analog output at AOUT with or without concurrent OWI1 I/O behavior (see section 6.4.3 for OWI application cases): 0 = Regular, separate Startup Window for OWI first, then switch over to AOUT behavior 1 = Direct start with output of analog signal at AOUT
	6:4	000_{BIN}	temp_source	Selection of utilized temperature sensor source: 000 = Integrated PTAT temperature sensor (no extra setup required) 001 = Bridge as temperature sensor with internal *Rt* in Current Mode[b] 010 = Current Mode through T_{EXT} [b]: bridge as the temperature sensor with external *Rt* at T_{EXT} and internal bottom-*Rt*' 011 = Current Mode operation for diode or PTC between T_{EXT} and VSSB [b] with internal *Rt* and *Rt*' 100 = Current Mode operation for diode or PTC between T_{EXT} and VSSB [b] with internal bottom-Rt' 101 = Ratiometric supply for the sensor (bridge) as the temperature sensor with the internal *Rt* and *Rt'* [b] 110 = Ratiometric supply for sensor (bridge) as the temperature sensor with the external *Rt* between sensor (bridge) top and T_{EXT} pin[b] 111 = Not assigned
	8:7	00_{BIN}	sensor_sup	Front-end operation and supply setup for main measurand sensor measurements: 00 = Ratiometric supply at VDDB 01 = Current Mode out of VDDB from Tbias (see section 6.2) 10 = Absolute voltage (Thermopile) 11 = Not assigned Note: if *temp_source* = 100 (temperature application T3.2) is also set up, *sensor_sup* = 01 must be configured in order to get ratiometric main sensor supply at VDDB.
	11:9	000_{BIN}	internal_rt	Top resistance set up for "Bridge as temperature sensor" configuration (see Table 16). Selection of resistance value (internal *Rt*) for re-using the sensor (bridge) as the temperature sensor with internal *Rt* (*temp_source* = 001 or 101). Selected *Rt* value is as follows: 000 = 1.34kΩ 100 = 15kΩ 001 = 4kΩ 101 = 20kΩ 010 = 8kΩ 110 = 30kΩ 011 = 10kΩ 111 = 40kΩ Note: the same value is selected for the bottom *Rt*', if *extra_rt* = 1_{BIN} is selected
	12	0_{BIN}	extra_rt	Bottom resistance setup for the "Bridge as temperature sensor" configuration. Defines whether an internal bottom resistor *Rt*' equivalent to the *internal_rt* value selection is placed between VSSB and PGA negative input: 0 = Use internal *Rt*' 1 = Do not apply internal *Rt*'

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
	13	0_{BIN}	owi_off	Setup bit to disable OWI interface: 0 = OWI is enabled and usable 1 = OWI is disabled and cannot be used Note: This setting has no effect on SPI or I2C operation
	14	0_{BIN}	lock	Lock bit: no further NVM writing is possible if this bit is set. 0 = NVM write allowed 1 = NVM locked Note: Once this bit is set to 1, the lock becomes effective after the next IC reset.
	15	0_{BIN}	cp_off	Switch off the charge pump for the internal regulators: 0 = Charge pump on (recommended setting for better PSRR, or when external VDD<4.3V) 1 = Charge pump off (less current consumption and lower distortion risks, e.g. coupling to VSS); this might be needed to ensure the 4mA low-limit in current loop applications (default setting for pre-configured Current-Loop application products: ZSSC3241DL*) Note: Switch off the charge pump only if V_{DD} > 4.3V is ensured
Smart Sensor Feature Configuration Register 2 (SSF2):				
04_{HEX}	1:0	00_{BIN}	dacres	Setup of DAC output resolution: 00 = 13-bit 01 = 14-bit 10 = 15-bit 11 = 16-bit
	2	1_{BIN}	dither_off	Switch on/off the dithering function for the DAC: 0 = Dither is applied for DAC outputs 1 = Dither is switched off
	3	0_{BIN}	dacouttype	Defines if the SSC-corrected sensor(bridge) signal S or the temperature signal T is the output at the DAC: 0 = Sensor signal S is output at the DAC 1 = Temperature signal T is output at DAC
	4	0_{BIN}	cont_ANAoutn	Selects whether the ZSSC3241 provides analog output in general: 0 = Analog (DAC) output is enabled 1 = No analog output (cyclic operation with digital outputs is still possible) Note: If *cont_ANAoutn* is set to 1, then *Aout_setup* is ignored; there is no analog output in Sleep Mode in general
	7:5	001_{BIN} (000_{BIN})	Aout_setup	Definition of the basic AOUT pin behavior: 000 = Current loop enabled, output through error amplifier for current loop[c], OWI listens to both the $OWI2_{in}$ and OWI1 pins concurrently (default setting for pre-configured Current-Loop application products: ZSSC3241DL*) 001 = External V_{DD}-ratiometric, rail-to-rail out 010 = 0V to 1.0V absolute output 011 = 0V to 5V absolute output 100 = not assigned 101 = External V_{DD}-ratiometric, rail-to-rail out ($OWI2_{in}$ enabled) 110 = 0V to 1.0V absolute output ($OWI2_{in}$ enabled) 111 = 0V to 5V absolute output ($OWI2_{in}$ enabled) Note: if lower and upper band are reserved for signalizing diagnostic states, proper output calibration and/or DAC clipping is required together with *diagouten*=1_{BIN}
	8	0_{BIN}	diagouten	Enable diagnostic level output mode 0 = No analog signalization 1 = Analog diagnostic signaling is enabled

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
	9	0_{BIN}	disable_ldoctrl	Switch off the internal output regulator circuit running the LDOctrl pin if no external supply transistor (such as JFET) is used; this reduces current consumption, etc. 0 = LDOctrl output is switched/kept on 1 = LDOctrl output switched off Note: If enabled (= 0), then the charge-pump can be off (the *cp_off* bit = 1 in register 03_{HEX})
	11:10	10_{BIN}	VDD_ldoctrl _target	Set point for regulated V_{DD} using external supply transistor JFET or depletion MOSFET: 00 = V_{DD} = 4.8V 01 = V_{DD} = 5.0V 10 = V_{DD} = 5.2V 11 = V_{DD} = 5.4V
	12	0_{BIN}	AZMs_on	Enable/disable for auto-zero measurement for (bridge) sensor measurement: 0 = No auto-zero measurements for sensor signal 1 = Auto-zero measurement of sensor bridge is performed and processed Note: This setup is ignored for raw data measurements with setup via the interface, i.e. command $A2_{HEX}$
	13	0_{BIN}	AZMt_on	Enable/disable for auto-zero measurement for temperature measurement: 0 = No auto-zero measurements for temperature signal 1 = Auto-zero measurement for temperature signal performed and processed
	15:14	00_{BIN}	oversamp_cyc	Selection for applied digital oversampling in Cyclic Mode operation: 00 = No oversampling 01 = Oversample-4: Results of 4 SSC cycles per last *meas_scheduler* sequence 10 = Oversample-8: Results of 8 SSC cycles per last *meas_scheduler* sequence 11 = Oversample-16: Results of 16 SSC cycles per last *meas_scheduler* sequence *Note:* This setup is ignored for any measurement in Command and Sleep Mode
Signal Conditioning Parameters				
05_{HEX}	15:0	0000_{HEX}	Offset_S[15:0]	Bits [15:0] of the 24-bit-wide sensor offset correction coefficient *Offset_S.* The MSBs including sign are *Offset_S*[23:16], which is [15:8] in register $0F_{HEX}$.
06_{HEX}	15:0	0000_{HEX}	Gain_S[15:0]	Bits [15:0] of the 24-bit-wide value of the sensor gain coefficient *Gain_S*. The MSBs including sign are *Gain_S*[23:16], which is [7:0] in register $0F_{HEX}$.
07_{HEX}	15:0	0000_{HEX}	Tcg[15:0]	Bits [15:0] of the 24-bit-wide coefficient *Tcg* for the temperature correction of the sensor gain. The MSBs including sign are *Tcg*[23:16], which is bits [15:8] in register 10_{HEX}.
08_{HEX}	15:0	0000_{HEX}	Tco[15:0]	Bits [15:0] of the 24-bit-wide coefficient *Tco* for temperature correction of the sensor offset. The MSBs with sign are *Tco*[23:16], which is bits [7:0] in register 10_{HEX}.
09_{HEX}	15:0	0000_{HEX}	SOT_tco[15:0]	Bits [15:0] of the 24-bit-wide 2nd order term *SOT_tco* applied to *Tco*. The MSBs of this term including sign are *SOT_tco*[23:16], which is bits [15:8] in register 11_{HEX}.
$0A_{HEX}$	15:0	0000_{HEX}	SOT_tcg[15:0]	Bits [15:0] of the 24-bit-wide 2nd order term *SOT_tcg* applied to *Tcg*. The MSBs of this term including sign are *SOT_tcg*[23:16], which is bits[7:0] in register 11_{HEX}.
$0B_{HEX}$	15:0	0000_{HEX}	SOT_sens[15:0]	Bits [15:0] of the 24-bit-wide 2nd order term *SOT_sens* applied to the sensor readout. The MSBs of this term including sign are *SOT_sens*[23:16], which is bits[15:8] in register 12_{HEX}.

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
0C$_{\text{HEX}}$	15:0	0000$_{\text{HEX}}$	Offset_T[15:0]	Bits [15:0] of the 24-bit-wide temperature offset correction coefficient *Offset_T*. The MSBs of this coefficient including sign are *Offset_T*[23:16], which is bits[7:0] in register 12$_{\text{HEX}}$.
0D$_{\text{HEX}}$	15:0	0000$_{\text{HEX}}$	Gain_T[15:0]	Bits [15:0] of the 24-bit-wide absolute value of the temperature gain coefficient *Gain_T*. The MSBs including sign are *Gain_T*[23:16], which is bits[15:8] in register 13$_{\text{HEX}}$.
0E$_{\text{HEX}}$	15:0	0000$_{\text{HEX}}$	SOT_T[15:0]	Bits [15:0] of the 24-bit-wide 2$^{\text{nd}}$-order term *SOT_T* applied to the temperature reading. The MSBs including sign are *SOT_T*[23:16], which is bit[7:0] in register 13$_{\text{HEX}}$.
0F$_{\text{HEX}}$	7:0	20$_{\text{HEX}}$	Gain_S[23:16]	Bits [23:16] including sign for the 24-bit-wide sensor gain correction coefficient *Gain_S*. The LSBs of this coefficient are *Gain_S*[15:0] in register 06$_{\text{HEX}}$.
	15:8	00$_{\text{HEX}}$	Offset_S[23:16]	Bits [23:16] including sign for the 24-bit-wide sensor offset correction coefficient *Offset_S*. The LSBs are *Offset_S*[15:0] in register 05$_{\text{HEX}}$.
10$_{\text{HEX}}$	7:0	00$_{\text{HEX}}$	Tco[23:16]	Bits [23:16] including sign for the 24-bit-wide coefficient *Tco* for temperature correction for the sensor offset. The LSBs are *Tco*[15:0] in register 08$_{\text{HEX}}$.
	15:8	00$_{\text{HEX}}$	Tcg[23:16]	Bits [23:16] including sign for the 24-bit-wide coefficient *Tcg* for the temperature correction of the sensor gain. The LSBs are *Tcg*[15:0] in register 07$_{\text{HEX}}$.
11$_{\text{HEX}}$	7:0	00$_{\text{HEX}}$	SOT_tcg[23:16]	Bits [23:16] including sign for the 24-bit-wide 2$^{\text{nd}}$ order term *SOT_tcg* applied to Tcg. The LSBs are *SOT_tcg*[15:0] in register 0A$_{\text{HEX}}$.
	15:8	00$_{\text{HEX}}$	SOT_tco[23:16]	Bits [23:16] including sign for the 24-bit-wide 2$^{\text{nd}}$ order term *SOT_tco* applied to Tco. The LSBs are *SOT_tco*[15:0] in register 09$_{\text{HEX}}$.
12$_{\text{HEX}}$	7:0	00$_{\text{HEX}}$	Offset_T[23:16]	Bits [23:16] including sign for the 24-bit-wide temperature offset correction coefficient *Offset_T*. The LSBs are *Offset_T*[15:0] in register 0C$_{\text{HEX}}$.
	15:8	00$_{\text{HEX}}$	SOT_sens[23:16]	Bits [23:16] including sign for the 24-bit-wide 2$^{\text{nd}}$ order term *SOT_sens* applied to the sensor readout. The LSBs are *SOT_sens*[15:0] in register 0B$_{\text{HEX}}$.
13$_{\text{HEX}}$	7:0	00$_{\text{HEX}}$	SOT_T[23:16]	Bits [23:16] including sign for the 24-bit-wide 2$^{\text{nd}}$-order term *SOT_T* applied to the temperature reading. The LSBs are *SOT_T*[15:0] in register 0E$_{\text{HEX}}$.
	15:8	20$_{\text{HEX}}$	Gain_T[23:16]	Bits [23:16] including sign for the 24-bit-wide absolute value of the temperature gain coefficient *Gain_T*. The LSBs are *Gain_T*[15:0] in register 0D$_{\text{HEX}}$.
Measurement Configuration Register 1 (*SM_config1*)				
14$_{\text{HEX}}$	3:0	0111$_{\text{BIN}}$	Gain_stage1	Gain setting for the 1$^{\text{st}}$ PGA stage with *Gain_stage1*[3:0]: Parameters are valid for Gain$_{\text{PGA}}$ ≤ 192: 0000 = 1.2 0001 = 2 0010 = 4 0011 = 6 0100 = 12 0101 = 20 0110 = 30 0111 = 40 1000 = 60 1001 = 80 1010 = 120 Parameters are limited for Gain$_{\text{PGA}}$ > 192: 1011 = 150 1100 = 200 1101 = 240 1110 = 300 1111 = Not assigned
	6:4	001$_{\text{BIN}}$	Gain_stage2	Gain setting for the 2$^{\text{nd}}$ PGA stage with *Gain_stage2*[1:0]: 000 = 1.1 001 = 1.2 010 = 1.3 011 = 1.4 100 = 1.5 101 = 1.6 110 = 1.7 111 = 1.8
	7	0$_{\text{BIN}}$	Gain_polarity	Set up the polarity of the sensor bridge's gain (invert chopper 1): 0 = positive (no polarity change) 1 = negative (180° polarity change)

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
	11:8	0100_{BIN}	adc_bits	Resolution, i.e. absolute number of bits for the ADC with *adc_bits*[3:0]: 0000 = 12 0001 = 13 0010 = 14 0011 = 15 0100 = 16 (default) 0101 = 17 0110 = 18 0111 = 19 1000 = 20 1001 = 21 1010 = 22 1011 = 23 1100 = 24 1101 to 1111 = Not assigned
	14:12	000_{BIN}	adc_offset	Differential signal's offset shift in the ADC including gain x2; compensation of x% signal offset: 000 = 0%, no offset compensation 001 = 6.25% offset 010 = 12.50% offset 011 = 18.75% offset 100 = 25.00% offset 101 = 31.25% offset 110 = 37.50% offset 111 = 44.00% offset
	15	1_{BIN}	sel_ref1	Reference source for main sensor measurement: 0 = Absolute (internal) bandgap is the reference 1 = Ratiometric reference; recommended for ratiometrically supplied sensors
Measurement Configuration Register 2 (*SM_config2*)				
15_{HEX}	4:0	$0\ 0000_{BIN}$	ioffsc	Absolute voltage input shift for input signals to the PG, e.g. INP-INN The input signal is shifted by the following voltages: 00000 = 0mV, no shift 00001 = -1mV 00010 = -2mV 00011 = -3mV … 01110 = -14mV 01111 = -15mV 10000 = 0mV, no shift 10001 = +1mV 10010 = +2mV … 11110 = +14mV 11111 = +15mV
	7:5	000_{BIN}	Tbiasout	Current Mode sensor bias selection; nominal sensor supply current I_{sup} (if *sensor_sup* = 01): 000 = 5µA 001 = 10µA 010 = 20µA 011 = 39µA 100 = 79µA 101 = 157µA 110 = 196µA 111 = 494µA
	8	0_{BIN}	adc_en_shift	General disable/enable of the ADC feature to apply the extra gain x2 and signal offset compensation *adc_offset* in register 14_{HEX}: 0 = Gain: ×2 and signal offset compensation off 1 = Gain: ×2 and signal offset compensation on
	9	1_{BIN}	pga_en_shift	Automatic common mode adjust feature, which allows automatically, optimally adapting the sensor-input common mode to AGND at the PGA output.[d] 0 = Automatic common mode adjustment off 1 = Automatic common mode adjustment on
	15:10	$00\ 0000_{BIN}$	–	Not assigned

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
External Temperature Measurement Configuration Register 1 (*extTemp_config1*)				
16_{HEX}	3:0	0000_{BIN}	Gain_stage1	Gain setting for the 1st PGA stage with *Gain_stage1*[3:0] for external temperature measurements: Parameters are valid for $Gain_{PGA} \leq 192$: 0000 = 1.2 0110 = 30 0001 = 2 0111 = 40 0010 = 4 1000 = 60 0011 = 6 1001 = 80 0100 = 12 1010 = 120 0101 = 20 Parameters are limited for $Gain_{PGA} > 192$: 1011 = 150 1100 = 200 1101 = 240 1110 = 300 1111 = Not assigned
	6:4	000_{BIN}	Gain_stage2	Gain setting for the 2nd PGA stage with *Gain_stage2*[1:0] for external temperature measurements: 000 = 1.1 100 = 1.5 001 = 1.2 101 = 1.6 010 = 1.3 110 = 1.7 011 = 1.4 111 = 1.8
	7	0_{BIN}	Gain_polarity	Set up the polarity of the temperature sensor gain (invert input) with: 0 = Positive (no polarity change) 1 = Negative (180° polarity change)
	11:8	0100_{BIN}	adc_bits	Resolution, i.e. absolute number of bits for the ADC for external temperature measurements with adc_bits[3:0]: 0000 = 12 0111 = 19 0001 = 13 1000 = 20 0010 = 14 1001 = 21 0011 = 15 1010 = 22 0100 = 16 (default) 1011 = 23 0101 = 17 1100 = 24 0110 = 18 1101 to 1111 = Not assigned
	14:12	000_{BIN}	adc_offset	Differential signal's offset shift in ADC including gain x2 for external temperature measurements; compensation of x% signal offset: 000 = 0%, no offset compensation 001 = 6.25% offset 010 = 12.50% offset 011 = 18.75% offset 100 = 25.00% offset 101 = 31.25% offset 110 = 37.50% offset 111 = 44.00% offset
	15	0_{BIN}	sel_ref2	Reference source for external temperature sensing and conversion: 0 = Absolute (internal) bandgap is reference 1 = Ratiometric reference; recommended for ratiometrically supplied sensors

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
External Temperature Measurement Configuration Register 2 (*extTemp_config2*)				
17_{HEX}	4:0	0 0000_{BIN}	ioffsc	Absolute voltage input shift for input signals for external temperature measurements to the PG, e.g. INP-INN The input signal is shifted by the following voltages: 00000 = 0mV, no shift 00001 = -1mV 00010 = -2mV 00011 = -3mV … 01110 = -14mV 01111 = -15mV 10000 = 0mV, no shift 10001 = +1mV 10010 = +2mV … 11110 = +14mV 11111 = +15mV
	7:5	000_{BIN}	Tbiasout	Current Mode sensor bias selection for external temperature measurements; nominal sensor supply current (if *temp_source* ϵ {001_{BIN}, 010_{BIN}, 011_{BIN}, 100_{BIN}}): 000 = 5µA 001 = 10µA 010 = 20µA 011 = 39µA 100 = 79µA 101 = 157µA 110 = 196µA 111 = 494µA
	8	0_{BIN}	adc_en_shift	General disenable/enable of the ADC feature for external temperature measurements to apply the extra gain x2 and signal offset compensation *adc_offset* in register 16_{HEX}: 0 = Gain: x2 and signal offset compensation off 1 = Gain: x2 and signal offset compensation on
	9	0_{BIN}	pga_en_shift	Automatic common mode adjust feature, which allows automatically, optimally adapting the sensor-input common mode to AGND at the PGA output for external temperature measurements.[d] 0 = Automatic common mode adjustment off 1 = Automatic common mode adjustment on
	15:10	00 0000_{BIN}	–	Not assigned
Interrupt Level Setup and Post-Calibration (Digital) Offset Calibration				
18_{HEX}	15:0	0000_{HEX}	TRSH1a[15:0]	Bits [15:0] of the 24-bit-wide interrupt threshold1a, *TRSH1a.* (The MSBs for this threshold are TRSH1a[23:16], which is bits [7:0] of register $1A_{HEX}$.)
19_{HEX}	15:0	0000_{HEX}	TRSH2a[15:0]	Bits [15:0] of the 24-bit-wide interrupt threshold2a, *TRSH2a*. (The MSBs for this threshold are TRSH2a[23:16], which is bits[15:8] of register $1A_{HEX}$.)
$1A_{HEX}$	7:0	00_{HEX}	TRSH1a[23:16]	Bits [23:16] of the 24-bit-wide interrupt threshold1a, *TRSH1a*. (The LSBs for this threshold are TRSH1a[15:0], which is bits[15:0] of register 18_{HEX}.)
	15:8	00_{HEX}	TRSH2a[23:16]	Bits [23:16] of the 24-bit-wide interrupt threshold2a, *TRSH2a.* (The LSBs for this threshold are TRSH2a[15:0], which is bits[15:0] of register 19_{HEX}.)
$1B_{HEX}$	15:0	0000_{HEX}	SENS_Shift[15:0]	Bits [15:0] of the post-calibration sensor offset shift coefficient *SENS_Shift.* (The MSBs of *SENS_Shift* are bits [15:8] of register $1D_{HEX}$.)
$1C_{HEX}$	15:0	0000_{HEX}	T_Shift[15:0]	Bits [15:0] of the post-calibration temperature offset shift coefficient *T_Shift.* (The MSBs of *T_Shift* are bits [7:0] of register $1D_{HEX}$.)
$1D_{HEX}$	7:0	00_{HEX}	T_Shift[23:16]	Bits [23:16] of the post-calibration temperature offset shift coefficient *T_Shift*. (The LSBs of *T_Shift* are in register $1C_{HEX}$.)

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
	15:8	00_{HEX}	SENS_Shift[23:16]	Bits [23:16] of the post-calibration sensor offset shift coefficient *SENS_Shift*. (The LSBs of *SENS_Shift* are in register $1B_{HEX}$.)
Measurement Scheduler (Cyclic Operation Sequence)				
$1E_{HEX}$	0	0_{BIN}	cycwsn	Cyclic measurement operation is performed with / including the sensor measurement: 0 = Sensor measurement is performed 1 = Sensor measurement is not performed Note: Whether AZS is to be performed in the cyclic measurement sequence is set up with *AZMs_on* (see register 04_{HEX})
	1	0_{BIN}	cycwtn	Cyclic measurement operation is performed with the temperature measurement: 0 = Temperature measurement is performed 1 = Temperature measurement is not performed Note: whether AZT is to be performed in the cyclic measurement sequence is set up with *AZMt_on* (see register 04_{HEX})
	2	0_{BIN}	-	Not assigned
	3	1_{BIN}	cycwscn	Cyclic measurement operation is performed with / including the sensor-connection check: 0 = Sensor connection check is performed 1 = Sensor connection check is not performed
$1E_{HEX}$ (continued)	The bits [9:4] in the $1E_{HEX}$ register define whether the cycle measurement sequence performs the respective measurement type in the first slot or only after respective *slots_X* have been completed for the first time. Note: The SSC and analog output will only become valid after the sensor, temperature, and related auto-zero measurements have already been conducted for the first time. The first output signals maybe invalid until this condition is reached.			
	4	0_{BIN}	startS_wfirstn	0 = Perform the sensor measurement in the first slot 1 = Do not perform the sensor measurement in the first slot
	5	0_{BIN}	startAZS_wfirstn	0 = Perform the auto-zero sensor measurement in the first slot 1 = Do not perform the auto-zero sensor measurement in the first slot Note: The *startAZS_wfirstn* bit is ignored for the cyclic operation if the *AZMs_on* = 0 = “off.”
	6	0_{BIN}	startT_wfirstn	0 = Perform the temperature measurement in the first slot 1 = Do not perform the temperature measurement in the first slot
	7	0_{BIN}	startAZT_wfirstn	0 = Perform the auto-zero temperature measurement in the first slot 1 = Do not perform the auto-zero temperature measurement in the first slot Note: The *startAZT_wfirstn* bit is ignored for the cyclic operation if the *AZMt_on* = 0 = “off.”
	8	0_{BIN}	–	Not assigned
	9	0_{BIN}	startSC_wfirstn	Diagnostics: sensor connection checks: 0 = Perform sensor connection checks in the first slot 1 = Do not perform sensor connection checks in the first slot
	15:10	$00\ 0000_{BIN}$	slots_T	Defines the number of pause slots between two subsequent temperature measurements: 0 = No pause, measure temperature at each slot 1_{DEC} to 63_{DEC}= Pause slots after the slot with the temperature measurement Note: Set *slots_T* = *slots_AZT* for correct Cyclic Operation.

NVM Address	Word / Bit Range	Default Setting	Description	Notes / Explanations
$1F_{HEX}$	5:0	$00\ 0000_{BIN}$	slots_AZT	Defines the number of pause slots between two subsequent auto-zero temperature (AZT) measurements: 0 = No pause, measure AZT at each slot 1 to 63_{DEC} = Number of pause slots after the slot with the AZT measurement Note: If *AZMt_on* = 0, no auto-zero temperature measurement will be performed.
	9:6	0000_{BIN}	slots_S	Defines the number of pause slots between two subsequent sensor / bridge measurements: 0 = No pause, measure sensor at each slot 1_{DEC} to 15_{DEC}= Number of pause slots after the slot with the sensor measurement Note: Set *slots_S* = *slots_AZS* for correct Cyclic Operation.
	13:10	0000_{BIN}	slots_AZS	Defines the number of pause slots between two subsequent auto-zero sensor (AZS) measurements: 0 = No pause, measure AZS at each slot 1_{DEC} to 15_{DEC}= Number of pause slots after the slot with sensor measurement Note: If *AZMs_on* = 0, no auto-zero sensor measurement is performed.
	15:14	00_{BIN}	–	These bits must be 00_{BIN} to ensure proper Cyclic Operation
20_{HEX}	5:0	$00\ 0000_{BIN}$	–	Not assigned.
	15:6	$00\ 0000\ 0000_{BIN}$	slots_SC	Defines the number of pause slots between two subsequent sensor connection check runs: 0 = No pause, always check sensor connection 1_{DEC} to 1023_{DEC}= Number of pause-slots after slot with Sensor-Connection check
Selection of (Sensor) Connection Checks to be Conducted				
21_{HEX}	The first 10 bits of register 21_{HEX} are the *select_checks[9:0]* bit field:			
	0	0_{BIN}	inp_check	Loss of sensor positive connection, INP [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	1	0_{BIN}	inn_check	Loss of bridge/sensor negative connection, INN [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	2	0_{BIN}	inp_range_check	Signal at pin INP out of range (leaking / short to VSS or VDDB) [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	3	0_{BIN}	inn_range_check	Signal at pin INN out of range (leaking / short to VSS or VDDB) [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	4	0_{BIN}	sens_short _check	Sensor short (INN = INP) 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	5	0_{BIN}	text_open_check	T_{EXT} pin open [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	6	0_{BIN}	text_range_check	Signal at pin T_{EXT} out of range (leaking / short to VSS or VDDB) [e] 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	7	0_{BIN}	text_inn_short _check	T_{EXT} pin short to INN 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
	8	0_{BIN}	text_inp_short _check	T_{EXT} pin short to INP 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	9	0_{BIN}	crack_check	Broken-chip check / chipping check 0 = Check is not performed; result is not signalized 1 = Check is performed; result is signalized
	15:10	00 0000_{BIN}	–	Not assigned
DAC (Output Calibration Data)				
22_{HEX}	15:0	$XXXX_{HEX}$	DAC10RM5V	Encoded, 16bit-quantized measurement value of DAC-output at V_{DD}=5V with 10%-DAC-excitation, digital code ($199A_{HEX}$). Programmed at Renesas' device test. The measured DAC-voltage[f] can be derived as: $V_{DAC10,AOUT}$[V] := DAC10RM5V[dec] / 296000 + 0.39
23_{HEX}	15:0	$XXXX_{HEX}$	DAC90RM5V	Encoded, 16bit-quantized measurement value of DAC-output at V_{DD}=5V with 90%-DAC-excitation, digital code ($E666_{HEX}$). Programmed at Renesas' device test. The measured DAC-voltage[f] can be derived as: $V_{DAC90,AOUT}$[V] := DAC90RM5V[dec] / 284000 + 4.45
Enhanced Output Features				
24_{HEX}	1:0	00_{BIN}	clipping_on	DAC Clipping function, i.e. consideration of DAC clipping limits (*Up_Clip_Lim*, *Low_Clip_Lim*) for the AOUT signal: 00 = DAC clipping disabled 01 = upper limit DAC clipping disabled, lower limit DAC clipping enabled 10 = upper limit DAC clipping enabled, lower limit DAC clipping disabled 11 = upper and lower limit DAC clipping enabled
	2	0_{BIN}	eoc_hyst_on	Enable second EOC interrupt extra threshold set *threshold1b* and *threshold2b*: 0 = usage of extra thresholds disabled 1 = usage of extra thresholds enabled
	3	0_{BIN}	dac_ssc_enable	Enable bit for the additional DAC-SSC pre-distortion for DAC output linearization (via *Gain_DAC*, *Offset_DAC*): 0 = usage of DAC-SSC correction disabled/bypassed 1 = usage of DAC-SSC correction enabled
	15:4	000_{HEX}	-	Not assigned
25_{HEX}	15:0	0000_{HEX}	Up_Clip_Lim	Upper DAC output clipping limit. If the calculated value (T or S per selection in *dacouttype*) is higher than this limit, the analog output value is clipped to this value. Note: if diagnostic checks are enabled (by means of *diagouten*), clipping is not applied
26_{HEX}	15:0	0000_{HEX}	Low_Clip_Lim	Lower DAC output clipping limit. If the calculated value (T or S per selection in *dacouttype*) is lower than this limit, the analog output value is clipped to this value. Note: if diagnostic checks are enabled (by means of *diagouten*), clipping is not applied
27_{HEX}	15:0	0000_{HEX}	TRSH1b[15:0]	Bits [15:0] of the 24-bit-wide interrupt *TRSH1b.* (The MSBs for this threshold are TRSH1b[23:16], which is bits [7:0] of register 29_{HEX}.)
28_{HEX}	15:0	0000_{HEX}	TRSH2b[15:0]	Bits [15:0] of the 24-bit-wide interrupt *TRSH2b.* (The MSBs for this threshold are TRSH2b[23:16], which is bits[15:8] of register 29_{HEX}.)
29_{HEX}	7:0	00_{HEX}	TRSH1b[23:16]	Bits [23:16] of the 24-bit-wide interrupt *TRSH1b*. (The LSBs for this threshold are TRSH1b[15:0], which is bits[15:0] of register 27_{HEX}.)
	15:8	00_{HEX}	TRSH2b[23:16]	Bits [23:16] of the 24-bit-wide interrupt *TRSH2b.* (The LSBs for this threshold are TRSH2b[15:0], which is bits[15:0] of register 28_{HEX}.)
$2A_{HEX}$	15:0	0000_{HEX}	Gain_DAC	Gain correction coefficient for DAC-SSC math, see section 6.6.3.3

NVM Address	Word/Bit Range	Default Setting	Description	Notes/Explanations
$2B_{HEX}$	15:0	0000_{HEX}	Offset_DAC	Offset correction coefficient for DAC-SSC math, see section 6.6.3.3
Free Memory (Available for Customer Use)				
$2C_{HEX}$	15:0	0000_{HEX}	–	Not assigned (e.g., can be used for Cust_IDx customer identification number)
…			–	Not assigned (e.g., can be used for Cust_IDx customer identification number)
34_{HEX}	15:0	0000_{HEX}	–	Not assigned (e.g., can be used for Cust_IDx customer identification number)
35_{HEX}	15:0	-	Checksum	Generated (checksum) for the entire memory through a linear feedback shift register (LFSR); signature is checked on power-up to ensure memory content integrity

[a] For I3C operation, this should contain the Legacy Virtual Register (LVR) information: $1X_{HEX}$ to Index 0. Fast-Mode is supported.

[b] Use the *extTemp_config1* and *extTemp_config2* registers for temperature sensor related front-end configuration.

[c] In Current Loop Operation Mode, it must be ensured that a sufficient external V_{DD}-level > 4.8V is present (e.g., with external supply transistor, such as JFET or depletion MOSFET, and extra LDO-control option).

[d] If *pga_en_shift* is enabled, the ZSSC3241 current consumption increases by approximately 100µA. Usage is recommended for optimizing the analog front-end setup.

[e] Do not enable (set to 0_{BIN}) if the IC is connected to an absolute voltage source sensor, for example, Thermopile (*sensor_sup* = 10_{BIN}).

[f] The IC provides the originally measured DAC-output voltage $V_{DAC*0,AOUT}$[V] with V_{DD}=5V, *Aout_setup*=(001_{BIN} or 101_{BIN}) as reaction on $B3_{HEX}$ command, see Table 34.

The NVM-consistence checksum is calculated (internally by the ZSSC3241 for the whole NVM) using the polynomial: $x^{16} + x^{15} + x^2 + 1$. The checksum verification is only realized directly after V_{DD} power-on. If the checksum is successfully verified, then the “Memory Error” status bit is set to 0_{BIN}.

6.6.3. Digital Sensor-Signal-Conditioning Mathematics

The saturation check (signalized by *SSC Calculation Unit Saturation*, see Table 17) in the ZSSC3241 detects saturation effects of the internal calculation steps, allowing the final correction output to be determined despite the saturation. It is possible to get potentially useful signal conditioning results that have had an intermediate saturation during the calculations. These cases are detectable; e.g., by observing the status bit[0] for each measurement result. Details about the saturation limits and the valid ranges for values are provided in the equations in the following sections.

The calibration math description assumes a calculation with integer numbers. The description is numerically correct concerning values, dynamic range, and resolution.

6.6.3.1. Main Sensor Signal Correction (Main SSC Math)

The configuration parameter *SOT_curve* in NVM register 02_{HEX} selects whether second-order equations compensate for sensor nonlinearity with a parabolic or S-shaped curve. The parabolic compensation is recommended for most sensor types.

The following equations describe the available SSC capabilities. The equation terms are as follows:

S	Corrected sensor reading output via I2C, OWI, or SPI; range [0_{HEX} to $FFFFFF_{HEX}$]
S_Raw	Raw sensor reading from ADC (after AZ correction, if selected); range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
Gain_S	Sensor gain term; range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
Offset_S	Sensor offset term; range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
Tcg	Temperature coefficient gain term; range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
Tco	Temperature coefficient offset term; range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
T_Raw	Raw temperature reading (after AZ correction); range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
SOT_tcg	Second-order term for Tcg non-linearity; range [-$7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

SOT_tco	Second-order term for Tco non-linearity; range [-7FFFFF$_{HEX}$ to 7FFFFF$_{HEX}$]
SOT_sens	Second-order term for sensor non-linearity; range [-7FFFFF$_{HEX}$ to 7FFFFF$_{HEX}$]
SENS_shift	Post-calibration, post-assembly offset shift; range [-7FFFFF$_{HEX}$ to 7FFFFF$_{HEX}$]
$\left\|\ldots\right\|$	Absolute value
$[\ldots]_{ll}^{ul}$	Bound/saturation number range from ll to ul, overflow/underflow is reported as saturation in the status byte

The correction formula for the differential signal reading is represented as a two-step process depending on the *SOT_curve* setting.

Table 36. Data Format of 24-bit SSC Coefficients

Bit-Number:	**23**	**22**	**21**	**20**	**…**	**2**	**1**	**0**
Meaning, Weighting	0 = positive 1 = negative	2^1	2^0	2^{-1}	…	2^{-19}	2^{-20}	2^{-21}

Table 37. Data Format of Corrected, SSC Results (*S* and *T)*

Bit-Number:	**23**	**22**	**21**	**20**	**…**	**2**	**1**	**0**
Meaning, Weighting	2^0	2^{-1}	2^{-2}	2^{-3}	…	2^{-21}	2^{-22}	2^{-23}

Equations for the parabolic *SOT_curve* setting (*SOT_curve* = 0):

Simplified*:*

$$K_1 = 2^{23} + \frac{T\_Raw}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_tcg}{2^{23}} \cdot T_{Raw} + 4 \cdot Tcg \right) \qquad \textbf{Equation 7}$$

$$K_2 = 4 \cdot Offset\_S + S\_raw + \frac{T\_Raw}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_tco}{2^{23}} \cdot T_{Raw} + 4 \cdot Tco \right) \qquad \textbf{Equation 8}$$

$$Z_{SP} = \frac{4 \cdot Gain\_S}{2^{23}} \cdot \frac{K_1}{2^{23}} \cdot K_2 + 2^{23} \quad \text{(delimited to positive number range)} \qquad \textbf{Equation 9}$$

$$S = \frac{Z_{SP}}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_sens}{2^{23}} \cdot Z_{SP} + 2^{23} \right) + SENS\_shift \quad \text{(delimited to positive number range)} \qquad \textbf{Equation 10}$$

Complete*:*

$$K_1 = \left[2^{23} + \left[\frac{T\_Raw}{2^{23}} \cdot \left[\left[\frac{SOT\_tcg}{2^{21}} \cdot T_{Raw} \right]_{-2^{25}}^{2^{25}-1} + 4 \cdot Tcg \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \qquad \textbf{Equation 11}$$

$$K_2 = \left[4 \cdot Offset\_S + \left[S\_raw + \left[\frac{T\_Raw}{2^{23}} \cdot \left[\left[\frac{SOT\_tco}{2^{21}} \cdot T_{Raw} \right]_{-2^{25}}^{2^{25}-1} + 4 \cdot Tco \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} \qquad \textbf{Equation 12}$$

$$Z_{SP} = \left[\left[\frac{Gain\_S}{2^{21}} \cdot \left[\frac{K_1}{2^{23}} \cdot K_2 \right]_{-2^{25}}^{2^{25}-1} \right]_{-2^{25}}^{2^{25}-1} + 2^{23} \right]_{0}^{2^{25}-1} \qquad \textbf{Equation 13}$$

$$S = \Bigg[\Bigg[\bigg[\frac{Z_{SP}}{2^{23}} \cdot \Bigg[\bigg[\frac{SOT\_sens}{2^{21}} \cdot Z_{SP}\bigg]_{-2^{25}}^{2^{25}-1} + 2^{23}\Bigg]_{-2^{25}}^{2^{25}-1}\Bigg]_{-2^{25}}^{2^{25}-1} + SENS\_shift\Bigg]_{0}^{2^{24}-1} \qquad \textbf{Equation 14}$$

Equations for the S-shaped SOT_curve setting (SOT_curve = 1):

Simplified:

$$Z_{SS} = \frac{4 \cdot Gain\_S}{2^{23}} \cdot \frac{K_1}{2^{23}} \cdot K_2 \qquad \text{(} K_1 \text{ and } K_2 \text{ according to Equation 7 and Equation 8)} \qquad \textbf{Equation 15}$$

$$S = \frac{Z_{SS}}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_sens}{2^{23}} \cdot |Z_{SS}| + 2^{23}\right) + 2^{23} + SENS\_shift \qquad \text{(delimited to positive number range)} \qquad \textbf{Equation 16}$$

Complete:

$$Z_{SS} = \Bigg[\Bigg[\bigg[\frac{Gain\_S}{2^{21}} \cdot \bigg[\frac{K_1}{2^{23}} \cdot K_2\bigg]_{-2^{25}}^{2^{25}-1}\Bigg]_{-2^{25}}^{2^{25}-1}\Bigg]_{-2^{25}}^{2^{25}-1} \qquad \textbf{Equation 17}$$

$$S = \Bigg[\Bigg[\bigg[\frac{Z_{SS}}{2^{23}} \cdot \Bigg[\bigg[\frac{SOT\_sens}{2^{21}} \cdot |Z_{SS}|\bigg]_{-2^{25}}^{2^{25}-1} + 2^{23}\Bigg]_{-2^{25}}^{2^{25}-1}\Bigg]_{-2^{25}}^{2^{25}-1} + 2^{23} + SENS\_shift\Bigg]_{0}^{2^{24}-1} \qquad \textbf{Equation 18}$$

6.6.3.2. Main Temperature Signal Correction

Temperature is measured either internally by the ZSSC3241 or through an additional external element or by means of a combination of ZSSC3241-internal and external temperature sensing capabilities; see sections 6.2.3 and 6.2.4. Temperature correction contains both linear gain and offset terms as well as a second-order term to correct for any nonlinearities. For temperature, second-order compensation for nonlinearity is always parabolic.

The correction equation terms are as follows:

T	Corrected temperature sensor reading output via digital interface; range [0_{HEX} to $FFFFFF_{HEX}$]
Gain_T	Gain coefficient for temperature; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
T_Raw	Raw temperature reading after AZ correction; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
Offset_T	Offset coefficient for temperature; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
SOT_T	Second-order term for temperature source nonlinearity; range [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]
T_Shift	Shift for post-calibration/post-assembly offset compensation [$-7FFFFF_{HEX}$ to $7FFFFF_{HEX}$]

The correction formula is best represented as a two-step process as follows:

Simplified:

$$Z_T = \frac{4 \cdot Gain\_T}{2^{23}} \cdot (T\_Raw + 4 \cdot Offset\_T) + 2^{23} \qquad \text{(delimited to positive number range)} \qquad \textbf{Equation 19}$$

$$T = \frac{Z_T}{2^{23}} \cdot \left(\frac{4 \cdot SOT\_T}{2^{23}} \cdot Z_T + 2^{23}\right) + T\_shift \qquad \text{(delimited to positive number range)} \qquad \textbf{Equation 20}$$

Complete:

$$Z_T = \Bigg[\bigg[\frac{Gain\_T}{2^{21}} \cdot [T\_Raw + 4 \cdot Offset\_T\,]_{-2^{25}}^{2^{25}-1}\bigg]_{-2^{25}}^{2^{25}-1} + 2^{23}\Bigg]_{0}^{2^{25}-1} \qquad \textbf{Equation 21}$$

$$T = \left[\left[\frac{Z_T}{2^{23}} \cdot \left[\left[\frac{SOT\_T}{2^{21}} \cdot Z_T\right]_{-2^{25}}^{2^{25}-1} + 2^{23}\right]_{-2^{25}}^{2^{25}-1}\right]_{-2^{25}}^{2^{25}-1} + \text{T\_shift}\right]_{0}^{2^{24}-1}$$

Equation 22

6.6.3.3. Separate Correction of the Digital-to-Analog Converter Characteristic (DAC-SSC)

In applications that require both digital and analog outputs, the separate DAC output signal compensation unit can be applied. It temperature independently allows to compensate the ZSSC3241's DAC offset and DAC gain deviation (resulting from manufacturing process variation) from an ideal, linear characteristic.

Note: If only analog outputs need to be provided, the main SSC math can cover corrections for all sensor- and IC-characteristics including DAC offset and DAC gain without an extra DAC output signal compensation feature.

The DAC output signal compensation can be enabled by *dac_ssc_enable.* It is applied to main SSC corrected output signals for main sensor: *S* or temperature: *T* (to which of those is determined by the *dacouttype* selection). The processing width and coefficients of the DAC output signal compensation are 16Bit wide. *Gain_DAC* is formatted as 16bit-integer, the *Offset_DAC* is formatted as 16bit 2's-complement.

DAC output signal compensation contains both linear gain and offset terms as follows:

Gain_DAC:	Gain coefficient for DAC output correction; range [0_{HEX} to $FFFF_{HEX}$];
Offset_DAC:	Offset coefficient for DAC output correction; range [$-7FF0_{HEX}$ to $7FF0_{HEX}$];
DAC_in_orig:	DAC Digital input from main SSC math (T or S); range [0_{HEX} to $FFFFFF_{HEX}$];
DAC_in:	16 MSBs of digital input from main SSC math (T or S); range [0_{HEX} to $FFFF_{HEX}$];
DAC_out:	Corrected digital word to lead to the final output of the DAC; range [0_{HEX} to $FFFF_{HEX}$];

Simplified:

$$\text{DAC\_IN} = \text{DAC\_in\_orig} \gg 8\text{bit}$$

Equation 23

$$\text{DAC\_OUT} = \left(\frac{\text{GAIN\_DAC}}{2} + \frac{1}{2}\right) \cdot \text{DAC\_IN} + 2 \cdot \text{OFFSET\_DAC} + \frac{1}{4} \quad \text{(delimited to 16bit-MSB positive number range)}$$

Equation 24

Complete:

$$\text{DAC\_IN} = \text{DAC\_in\_orig} \gg 8\text{bit}$$

Equation 25

$$\text{DAC\_OUT} = \left[\left[\frac{\text{GAIN\_DAC} + 2^{15}}{2^{16}} \cdot \text{DAC\_IN}\right] + 2 \cdot \text{OFFSET\_DAC} + 2^{14}\right]_{0}^{2^{16}-1}$$

Equation 26

The DAC output signal correction is not applied and the corresponding digital value is used for generating the DAC output signal without correction in the following cases:

- the DAC Diagnostic command ($B3_{HEX}$) is used to force the DAC output
- DAC outputs of the sensor-diagnostic are enabled (*diagouten*) and a valid diagnostic and failure event (for example, Sensor connection check failure) is detected
- DAC clipping is enabled and the digital main sSC corrected signal (S or T) already reached a programmed clipping limit.

6.7 External, Extra LDO (LDOctrl) for Applications for > 5.5V

The ZSSC3241 has integrated voltage regulators that generate separate analog and digital ZSSC3241-internal voltages for any valid external supply voltage, V_{DD} (2.7V to 5.5V). For proper ZSSC3241 function, the directly applied supply voltage should not exceed the maximum V_{DD} limit.

The ZSSC3241 also supports applications with higher application-inherent supply voltages greater than 5.5V. The ZSSC3241 provides a voltage regulation signal at the LDOctrl pin and a programmable IC supply, i.e. V_{DD}-level regulation target level, *VDD_ldoctrl_target* in the SSF2 register. The use of an additional external regulator transistor (by means of, for example JFET, depletion MOSFET, or comparable) further improves the power-supply rejection ratio (PSRR); i.e., it reduces effects from the external supply voltage onto the sensor measurement results in addition to the ZSSC3241-internal regulator properties. If the external extra supply regulation is not used or needed, the respective feature should be disabled by *disable_ldoctrl* = 1_{BIN}.

Table 38. IC Supply, V_{DD} Target Level Selection with External Voltage Regulation, External LDO

VDD_ldoctrl_target		**V_{DD} Target Level**	**Notes**
Bit[1]	**Bit[0]**		
0	0	4.8V	
0	1	5.0V	
1	0	5.2V	Recommended, typical settings.
1	1	5.4V	

Recommendation: Use the clamping diode at V_{DD} (to FB for current-loop output configurations or to VSS in all other cases with external LDO as shown by gray dashed line in Figure 27) to ensure over-voltage protection at the initial application power-on. The external transistor, depicted as JFET[1] can be a real JFET type, or, for example, depletion MOSFET and comparable. It must be selected such that the drain-source voltage can be at least V_{DDext} – 5V.

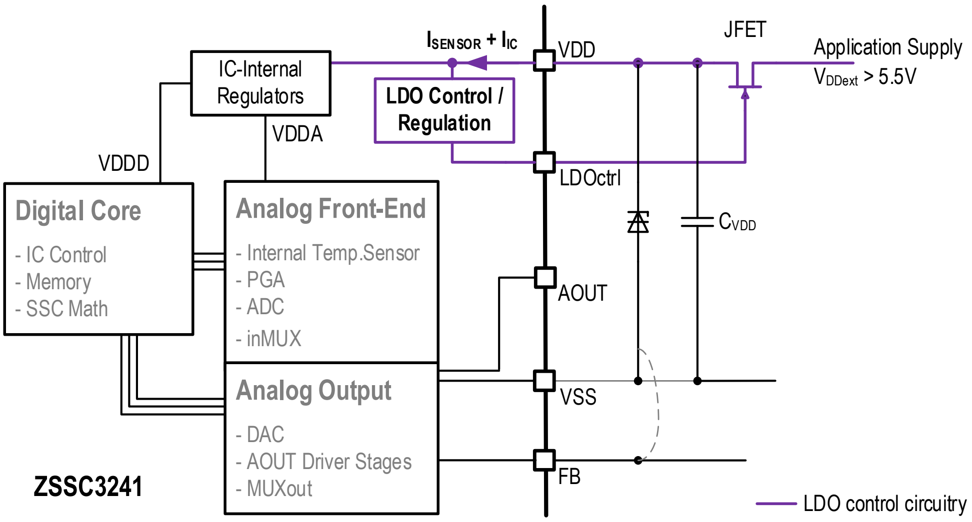


Figure 28. LDOctrl Application Topology

Table 39. External LDO Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
C_{ctrl}	Allowed parasitic capacitance at LDOctrl pin	–	150	500	pF
C_{VDD}	Buffer/filter capacitance between V_{DD} and VSS	80	100	120	nF

---

[1] Depending on the V_{DDext}>5.5V application main supply, different external transistors can be applied, for example BSS169 (Infineon), DN3545N8 (Microchip-Supertex), MMBF4392LT1G (Fairchild), etc.

7. Calibration

Calibration essentially involves collecting raw signal and temperature data from the sensor-ZSSC3241 system for different known sensor-element values (i.e., for a resistive bridge or an absolute voltage source) and temperatures. This raw data can then be processed by the calibration master (assumed to be the user's computer), and the calculated calibration coefficients can then be written to on-chip memory.

Brief overview of the three mains steps involved in calibrating the ZSSC3241:

1. *Assigning a unique identification to the ZSSC3241*. This identification is written to shadow RAM and programmed in NVM. This unique identification can be stored in the two 16-bit registers dedicated to the customer ID. It can be used as an index into a database stored on the calibration PC. This database will contain all the raw values of the connected sensor-element readings and temperature readings for that part, as well as the known sensor-element measurand conditions and temperature to which the sensor-element was exposed.
2. *Data collection.* Data collection involves getting uncorrected (raw) data from the external sensor at different known measurand values and temperatures. Then this data is stored on the calibration master using the unique identification of the device as the index to the database.
3. *Coefficient calculation and storage in NVM.* After enough data points have been collected to calculate all the desired coefficients, the coefficients can be calculated by the calibration master. Then the coefficients can be programmed to the memory.
4. *Result.* The sensor signal and the characteristic temperature effect on output will be linearized according to the setup-dependent maximum output range.

It is essential to perform the calibration with a fixed programming setup during the data collection phase.

Strong recommendation: To prevent any accidental misprocessing, keep the sensor front-end NVM setup (registers *SSF1, SSF2, SM_config1, SM_config2, extTemp_config1, extTemp_config2*) stable during the entire calibration process as well as in the subsequent operation.

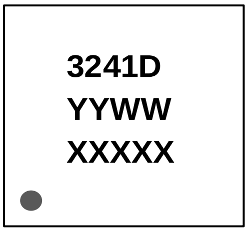
Note: A ZSSC3241 calibration only fits the setup used during its calibration. Changes of functional parameters after a successful calibration can decrease the precision and accuracy performance of the ZSSC3241 as well as of the entire application.

8. Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the links below. The package information is the most current data available.

- Generally valid summary information: https://www.renesas.com/eu/en/package/nlg24
- Specific package outline drawing: https://www.renesas.com/eu/en/document/psc/24-vfqfpn-package-outline-drawing-40-x-40-x-085-mm-body-050mm-pitch-epad-250-x-250-mm-wettable-flank?language=en&r=710

9. Marking Diagram



1. Line 1 is the truncated part number.
2. Line 2 – "YYWW" are the last two digits of the year and week that the part was assembled.
3. Line 3 – "XXXXX" denotes assembly lot number.

10. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
ZSSC3241DI1B	DICE on 304µm wafer no inking		Wafer Box	-40 to 125°C
ZSSC3241DI1C	Sawn DICE on frame, 304µm wafer, no inking		Wafer Box	-40 to 125°C
ZSSC3241DI5B	DICE on 304µm wafer with inking		Wafer Box	-40 to 125°C
ZSSC3241DI5C	Sawn DICE on frame, 304µm wafer, with inking		Wafer Box	-40 to 125°C
ZSSC3241DI3R	4 × 4 mm^2 24-QFN	MSL1	13 inch Reel	-40 to 125°C
ZSSC3241DI3W	4 × 4 mm^2 24-QFN	MSL1	7 inch Reel	-40 to 125°C
ZSSC3241DL1B	DICE on 304µm wafer no inking, pre-configured for Current-Loop		Wafer Box	-40 to 125°C
ZSSC3241DL1C	Sawn DICE on frame, 304µm wafer, no inking, pre-configured for Current-Loop		Wafer Box	-40 to 125°C
ZSSC3241DL5B	DICE on 304µm wafer with inking, pre-configured for Current-Loop		Wafer Box	-40 to 125°C
ZSSC3241DL5C	Sawn DICE on frame, 304µm wafer, with inking, pre-configured for Current-Loop		Wafer Box	-40 to 125°C
ZSSC3241DL3R	4 × 4 mm^2 24-QFN, pre-configured for Current-Loop	MSL1	13 inch Reel	-40 to 125°C
ZSSC3241DL3W	4 × 4 mm^2 24-QFN, pre-configured for Current-Loop	MSL1	7 inch Reel	-40 to 125°C
ZSSC3241KIT	Modular ZSSC3241 SSC Evaluation Kit including three interconnecting boards, five ZSSC3241 24-VFPQFN samples, and cable. Software is available for download on www.renesas.com/zssc3241KIT.			

11. Glossary

Term	Description
A2D	Analog-to-Digital
ACK	Acknowledge (interface's protocol indicator for successful data/command transfer)
ADC	Analog-to-Digital Converter or Conversion
AGND	Analog-Ground, ZSSC3241-internal … $VDDA_{int}/2$
AZ	Auto-Zero (unspecific)
AZS	Auto-Zero Measurement for (External) Sensor Path
AZT	Auto-Zero Measurement for (External or Internal) Temperature Path
CLK	Clock
DAC	Digital-to-Analog Converter or Conversion
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Immision (Immunity), i.e. immunity on spuriously coupled high-frequency disturbances
EOC	End of Conversion
FSO	Full Scale Output (value in percent relative to the ADC maximum output code; resolution dependent)
I2C	Inter-Integrated Circuit (I-Squared-C), asynchronous serial communication bus
LFSR	Linear Feedback Shift Register
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
NACK	Not Acknowledge (interface's protocol indicator for unsuccessful data/command transfer)
NVM	Nonvolatile Memory
Op amp	Operating Amplifier
PGA	Programmable Gain Amplifier
POR	Power-On Reset
PPT	Parts-per-Thousand, 1PPT=1/1000
PSRR	Power Supply (Disturbance) Rejection Ratio
PTC	Positive Temperature Coefficient (sensing element)
S	SSC-corrected Sensor Readout / Result
SM	Sensor Measurement
SOT	Second Order Term
SPI	Serial Peripheral Interface, synchronous serial communication interface

Term	Description
SSF	Smart-Sensor Function (specific NVM registers)
T	SSC-corrected (extra) Temperature Readout / Result
TC	Temperature Coefficient

12. Revision History

Revision Date	Description of Change
Mar.29.23	Initial release
Jul.14.23	Threshold value correction of $V_{high,I2C;}$ $V_{low,I2C}$ and $V_{high,SPI;}$ $V_{low,SPI}$