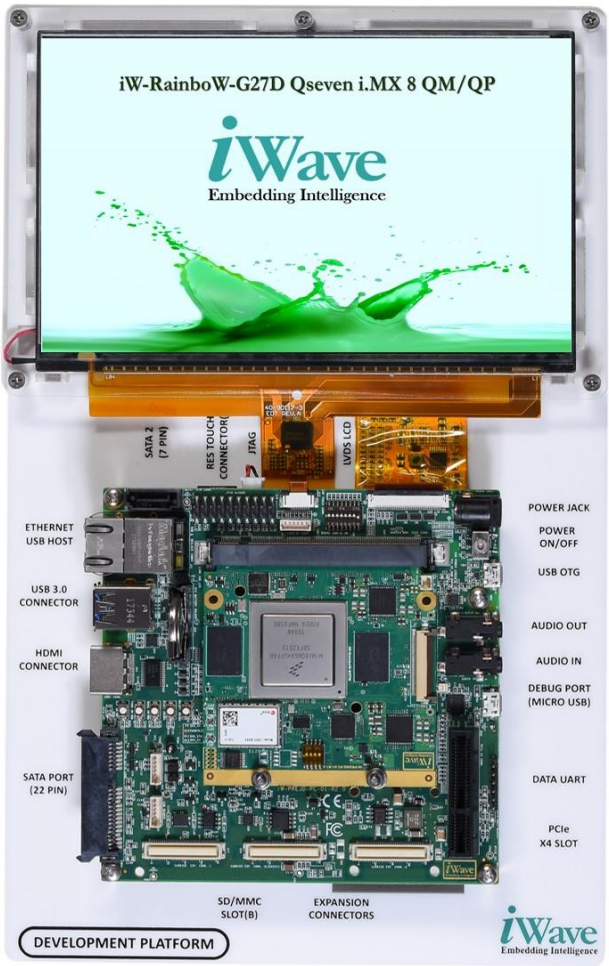
iW-RainboW-G27D
i.MX8 QuadMax/QuadPlus
Qseven Development Platform
Hardware User Guide



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Document Revision History

Document Number		iW-PREJD-UM-01-R2.0-REL1.0-Hardware-i.MX8-DevKit
Revision	**Date**	**Description**
0.1	24th Feb 2021	Draft version Release Version
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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX8 QM/QP Qseven V2.1 Development platform "iW-RainboW-G27D" based on the NXP's i.MX8 Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX8 QM/QP based Qseven development platform from a Hardware Systems perspective. Complete information about the i.MX8 QM/QP Qseven SOM is explained in another document "iW-RainboW-G27M_i.MX8QM_QP_Qseven_SOM-HardwareUserGuide".

1.2 Overview

The Qseven V2.1 concept is an off-the-shelf, multi-vendor, Computer-On-Module that integrates all the core components of a common PC and is mounted onto an application specific carrier board.

iW-RainboW-G27D Development Platform comes with Qseven V2.1 Generic Carrier, i.MX8 QM/QP based Qseven V2.1 SOM along with 7-inch Capacitive Touch Display. The development board can be used for quick prototyping of various applications targeted by the i.MX8 processor. With the 120mmx120mm Nano ITX size, Qseven carrier board is highly packed with all the necessary on-board connectors to validate the Qseven features of i.MX8 QM/QP Qseven SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CSI	Camera Serial Interface
DP	Display Port
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
Hz	Hertz
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IC	Integrated Circuit
LVDS	Low Voltage Differential Signalling

Acronyms	Abbreviations
MIPI	Mobile Industry Processor Interface
MLB	Media Local Bus
MXM	Mobile PCI Express Module
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SATA	Serial Advanced Technology Attachment
SD	Secure Digital
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
V	Voltage

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
LVDS	Low Voltage Differential Signal
GBE	Gigabit Ethernet Media Dependent Interface differential pair signals
USB HS	Universal Serial Bus High Speed differential pair signals
USB SS	Universal Serial Bus Super Speed differential pair signals
MIPI	Mobile Industry Processor Interface signals
HDMI	High-Definition Multimedia Interface Differential Signal
DP	Display Port Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On- Qseven *SOM.*

1.5 References

- IMX8QMAEC_Revx.pdf
- iMX8QM_RM_Rev_x.pdf
- Qseven® Specification Version 2.1
- Qseven® Design Guide 2.0

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the i.MX8 QM/QP Qseven SOM features and Hardware architecture with high level block diagram.

2.1 i.MX8 QM/QP Qseven Development Platform Block Diagram

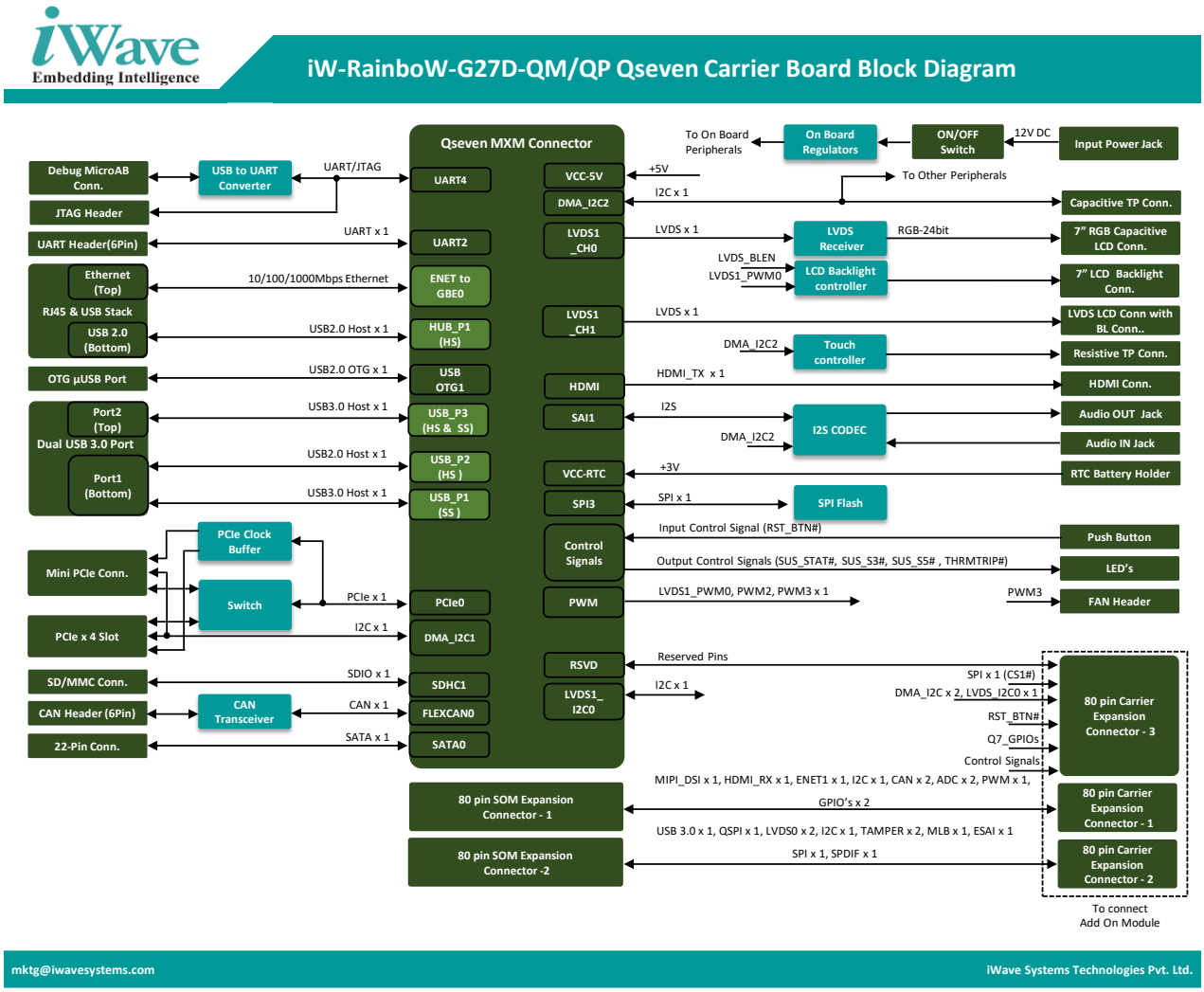

Figure 1: i.MX8 QM/QP Qseven Development Platform Block Diagram

2.2 i.MX8 QM/QP Qseven Development Platform Features

The NXP's i.MX8 QM/QP Qseven carrier board supports the following features to validate the NXP's i.MX8 QM/QP Qseven SOM Edge connector interface.

Serial Interface Features

- Debug UART through USB Micro AB Connector
- Data UART x 1 Port through Header

High Speed Interface Features

- PCIe x 1 Port through x4 connector or Mini-PCIe connector[1]
- SATA x 1 Port through 22pin SATA Connector
- USB 3.0 Host x 2 Port through USB 3.0 Type A Connector[2]

Communication Features

- 10/100/1000Mbps Ethernet through RJ45MagJack
- USB 2.0 Host x 1 Port through Type A Connector (Dual stack USB 3.0 - Top)
- USB 2.0 Host x 1 Port through Type A Connector
- USB 2.0 OTG x 1 Port through Micro AB Connector
- SDHC/SDIO (4bit) x 1 Port through Standard SD Connector
- CAN x 1 Port Through Header

Audio/Video Features

- I2S Audio Codec with 3.5mm Audio IN and OUT jack
- HDMI X 1 Port through Type A Connector
- 7'' RGB Display Connector through LVDS to RGB Transmitter with Capacitive Touch
- 2nd LVDS Port display Connector

Additional Features

- SPI Flash
- RTC Coin Cell holder
- Buzzer
- Fan Header
- 20 – Pin JTAG Header

On Board Switches

- Power ON/OFF Switch
- Board Configuration Switch
- Reset Switch

Carrier board Expansion Connectors

- SPI x 2 Port (1 is Optional - Shared with SPI Flash)
- QSPI/SPI x 1 Port
- HDMI Receiver x 1Port
- LVDS x 2 Channel
- MIPI DSI x 2 Channel
- ENET1 x 1
- CAN x 2 Port
- ADC x 2
- USB3.0 Host x 1 Ports (through On-SOM USB Hub)
- ESAI x 1 Port
- SPDIF x 1 Port
- MLB x 1 Port
- I2C x 3 Port
- TAMPER In & Out
- GPIOs & Power

General Specification

- Power Supply : 12V, 2A Power Input Jack
- Temperature Supported : 0°C to +60°C
- Form Factor : 120mm X 120mm Nano ITX

[1] PCIe Channel 0 can be connected to either Mini PCIe or PETp0 of PCIe X4 connector by using on Board Switches, whereas PCIe Channel 1 is directly connected to PETp1 of PCIe X4 connector.

[2] Either USB 2.0 in Mini PCIe connector or USB 3.0 Type A TOP connector can be supported at a time. Anyone can be selected using on Board Switches.

2.3 Qseven MXM Connector

The i.MX8 QM/QP Qseven carrier board supports 230Pin Qseven MXM Edge mating connector for Qseven SOM attachment. This standard 230-pin robust connector is capable of handling high-speed serialized signals and can be used for size constrained embedded applications. This Qseven MXM connector (J11) is physically located at the top of the board as shown below.

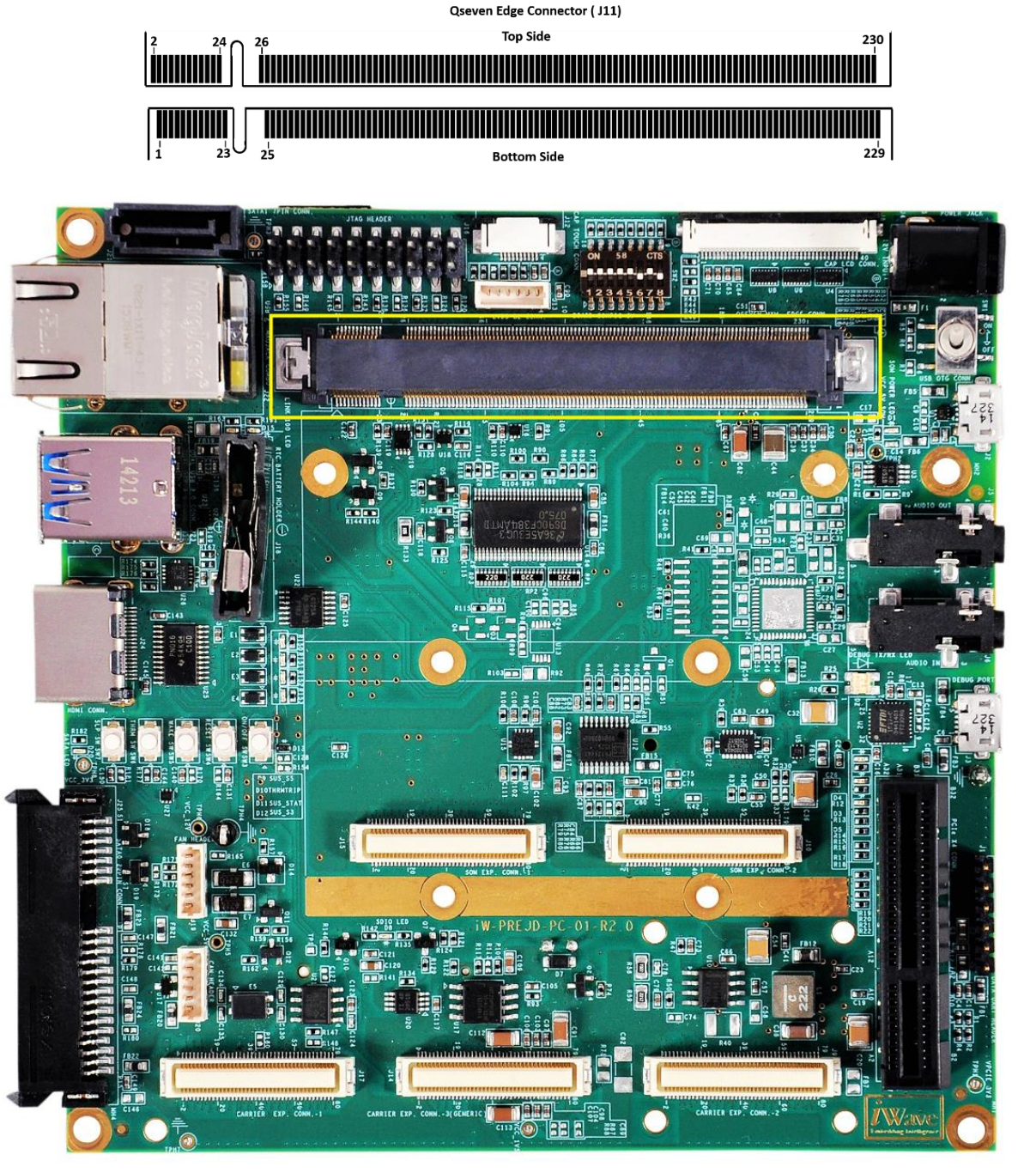

Figure 2: Qseven MXM Connector

2.3.1 Qseven PCB Edge Connector Pin Assignment

Table 3: Qseven PCB Edge Connector Pin Assignment

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	GND	GND	NA	Power	Ground.
2	GND	GND	NA	Power	Ground.
3	GBE_MDI3-	GBE0_MDI3-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 negative.
4	GBE_MDI2-	GBE0_MDI2-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 negative.
5	GBE_MDI3+	GBE0_MDI3+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 3 positive.
6	GBE_MDI2+	GBE0_MDI2+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 2 positive.
7	GBE_LINK100#	GBE0_LINK100#	NA	I, 3.3V CMOS	100Mbps Ethernet link status LED. *Note: This pin is connected to D15 Green LED.*
8	GBE_LINK1000#	GBE0_LINK1000#	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED. *Note: This pin is connected to D16 Green LED.*
9	GBE_MDI1-	GBE0_MDI1-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 negative.
10	GBE_MDI0-	GBE0_MDI0-	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 negative.
11	GBE_MDI1+	GBE0_MDI1+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 1 positive.
12	GBE_MDI0+	GBE0_MDI0+	NA	IO, DIFF	Gigabit Ethernet MDI differential pair 0 positive.
13	GBE_LINK#	GPHY_LINK_LED	NA	I, 3.3V CMOS	Gigabit Ethernet link status LED.
14	GBE_ACT#	GBE0_LINK_ACT#	NA	I, 3.3V CMOS	Gigabit Ethernet Activity status LED.
15	GBE_CTREF	VPHY0_DVDDL	NA	Power	Power for the Centre Tap of Mack Jack connector
16	SUS_S5#	SUS_S5_Q7	NA	I, 3.3V CMOS	S5 State. This pin is connected to indication LED D9. *Note: This pin is optionally connected to Expansion Connector3 (J14) 8th Pin.*
17	WAKE#	WAKE#(GPIO3_04)	SPI0_SDI/ BA5	O, 3.3V CMOS	This pin is connected to Push button (SW5) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: This pin is optionally connected to Expansion Connector3 (J14) 16th Pin.
18	SUS_S3#	SUS_S3_Q7	NA	I, 3.3V CMOS	S3 state. This pin is connected to indication LED D12. *Note: This pin is optionally connected to Expansion Connector3 (J14) 7th Pin.*
19	SUS_STAT#	SUS_STAT_Q7(GPIO2_05)	ESAI1_FST/ BF12	I, 3.3V CMOS	Suspend Status. This pin is connected to indication LED D10. *Note: This pin is optionally connected to Expansion Connector3 (J14) 10th Pin.*
20	PWRBTN#	PWRBTN#	ON_OFF_BUTTON/ BE47	O, 3.3V CMOS	Power Button output. This pin is connected to Push button (SW3) in the carrier board used for SOM On/Off control. *Note: This pin is optionally connected to Expansion Connector3 (J14) 24th Pin.*
21	SLP_BTN#	GPII_1(GPIO0_04)	LSIO.GPIO0.IO04/ AT48	O, 3.3V CMOS	This pin is connected to Push button (SW7) in carrier board. *Note: This pin is optionally connected to Expansion Connector3 (J14) 22nd Pin.*
22	LID_BTN#	GPII_0(GPIO3_03)	SPI0_SDO/ AY6	I, 3.3V CMOS	This pin is connected from 8bit DIP switch (SW2) 3rd position in carrier board. *Note: This pin is optionally connected to Expansion Connector3 (J14) 28th Pin.*
23	GND	GND	NA	Power	Ground.
24	GND	GND	NA	Power	Ground.
Key					
25	GND	GND	NA	Power	Ground.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
26	PWGIN	PWGIN	NA	O, 5V CMOS/ 10K PU	Power Good Output.
27	BATLOW#	GPII_2(GPIO0_05)	LSIO.GPIO0.IO05/ AP46	I, 3.3V CMOS	This pin is connected from 8bit DIP switch (SW2) 2nd position in carrier board. *Note: This pin is optionally connected to Expansion Connector3 (J14) 30th Pin.*
28	RSTBTN#	RSTBN	NA	O, 3.3V CMOS	Active low Reset button Output. This pin is connected to Push button SW4 in carrier board for reset generation. *Note: This pin is optionally connected to Expansion Connector3 (J14) 12th Pin.*
29	SATA0_TX+	PCIE_SATA0_TX0_P	PCIE_SATA0_TX0_P/ B16	I, SATA	This pin is connected to 22pin SATA Connector (J25) for SATA Channel0 Transmit differential pair positive.
30	SATA1_TX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
31	SATA0_TX-	PCIE_SATA0_TX0_N	PCIE_SATA0_TX0_N/ C17	I, SATA	This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Transmit differential pair negative.
32	SATA1_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
33	SATA_ACT#	GPIO_SATA_ACT#(GPIO1_18)	MIPI_DSI0_GPIO0_00/BD30	I, 3.3V CMOS	This pin connected from 22pin SATA Connector (J25) for SATA Channel0 command Activity line.
34	GND	GND	NA	Power	Ground.
35	SATA0_RX+	PCIE_SATA0_RX0_P	PCIE_SATA0_RX0_P/ A19	I, SATA	This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Receive differential pair positive.
36	SATA1_RX+	NC	NA	-	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
37	SATA0_RX-	PCIE_SATA0_RX0_N	PCIE_SATA0_RX0_N/ B20	I, SATA	NC in i.MX8 Qseven SOM. This pin connected to 22pin SATA Connector (J25) for SATA Channel0 Receive differential pair negative.
38	SATA1_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin connected to 7pin SATA Connector (J21) in carrier board.
39	GND	GND		Power	Ground.
40	GND	GND		Power	Ground.
41	BIOS_DISABLE#/ BOOT_ALT#	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected from 8bit DIP switch (SW2) 1st position in carrier board. *Note: This pin is optionally connected to Expansion Connector3 (J14) 32nd Pin.*
42	SDIO_CLK#	uSDHC1_CLK	USDHC1_CLK /J39	I, 3.3V CMOS	uSDHC1 Clock. This pin is connected to SD/MMC connector (J30).
43	SDIO_CD#	GPIO_SDC1_CD(GPIO1_23)	MIPI_DSI1_GPIO0_01 /BK24	O, 3.3V CMOS	uSDHC1 Card Detect. This pin is connected from SD/MMC connector (J30).
44	SDIO_LED	GPIO_SD1_LED(GPIO3_06)	SPI0_CS1/ BA3	I, 3.3V CMOS	SDIO LED. This pin is connected to D8 Green LED.
45	SDIO_CMD	uSDHC1_CMD	USDHC1_CMD /G41	IO,3.3VCMOS	uSDHC1 command. This pin is connected to SD/MMC connector (J30).
46	SDIO_WP	GPIO_SDC1_WP (GPIO1_22)	MIPI_DSI1_GPIO0_00/BM24	O, 3.3V CMOS	uSDHC1 Write Protect. This pin is connected to SD/MMC connector (J30).
47	SDIO_PWR#	GPIO_SDC1_PWR_EN(GPIO1_19)	MIPI_DSI0_GPIO0_01/BD28	I, 3.3V CMOS/ 10K PD	SD/MMC Interface Power Enable. This pin is used control the power input to the SD/MMC connector.
48	SDIO_DAT1	uSDHC1_DATA1	USDHC1_DATA1 /F38	IO, 3.3V CMOS	uSDHC1 Data1. This pin is connected to SD/MMC connector (J30).
49	SDIO_DAT0	uSDHC1_DATA0	USDHC1_DATA0 /E37	IO, 3.3V CMOS	uSDHC1 Data0.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to SD/MMC connector (J30).
50	SDIO_DAT3	uSDHC1_DATA3	USDHC1_DATA3 /F40	IO, 3.3V CMOS	uSDHC1 Data3. This pin is connected to SD/MMC connector (J30).
51	SDIO_DAT2	uSDHC1_DATA2	USDHC1_DATA2 /E39	IO, 3.3V CMOS	uSDHC1 Data2. This pin is connected to SD/MMC connector (J30).
52	SDIO_DAT5	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
53	SDIO_DAT4	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
54	SDIO_DAT7	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
55	SDIO_DAT6	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to SD/MMC connector (J30) in carrier board.
56	USB_DRIVE_VBUS	USB_OTG1_PWR(GPIO4_03)	USB_SS3_TC0/ J9	I, 3.3V CMOS	USB OTG Power enable.
57	GND	GND	NA	Power	Ground.
58	GND	GND	NA	Power	Ground.
59	HDA_SYNC/ I2S_WS	SAI1_TXFS	SAI1_TXFS/ AV2	I, 3.3V CMOS	SSI Audio transmit frame synchronization. This pin is connected to I2S audio codec.
60	SMB_CLK/ GP1_I2C_CLK	DMA_I2C1_SCL	DMA.I2C1.SCL/ AY52	I, 3.3V OD	I2C0 clock. This pin is connected to PCIe Clock buffer, PCIex4 connector, Mini PCIe connector and Expansion Connector3 (J14) 77th Pin.
61	HDA_RST#/ I2S_RST#	GPIO_RESET(GPIO1_05)	LVDS0_GPIO01/ BD40	I, 3.3V CMOS/ 10K PU	Audio Codec Reset. This pin is connected to Capacitive Touch Connector for touch reset & Expansion connector3 (J14) 42nd Pin.
62	SMB_DAT/ GP1_I2C_DAT	DMA_I2C1_SDA	DMA.I2C1.SDA/ AV52	IO, 3.3V OD	I2C0 Data. This pin is connected to PCIe Clock buffer, PCIex4 connector, Mini PCIe

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					connector and Expansion Connector3 (J14) 79th Pin.
63	HDA_BCLK/ I2S_CLK	SAI1_TXC	SAI1_TXC / AU5	O, 3.3V CMOS	SSI Audio transmit clock. This pin is connected from I2S audio codec.
64	SMB_ALERT#	SMBUS_ALERT(GPIO1_15)	LVDS1_I2C1_SDA/BN35	O, 3.3V CMOS	NC in i.MX8 Qseven SOM. This pin is connected to Expansion connector3 (J14) 11th Pin in carrier board.
65	HDA_SDI/ I2S_SDI	SAI1_RXD	SAI1_RXD/ AV4	O, 3.3V CMOS	SSI Audio Transmit Data. This pin is connected from I2S audio codec.
66	GP0_I2C_CLK	DMA_I2C2_SCL	DMA.I2C2.SCL /BA53	I, 3.3V OD	I2C2 clock. This pin is connected to I2S Audio Codec, Capacitive touch connector, Resistive touch connector, and Expansion Connector3 (J14) 78th Pin.
67	HDA_SDO/ I2S_SDO	SAI1_TXD	SAI1_TXD / AU1	I, 3.3V CMOS	SSI Audio Receive Data. This pin is connected to I2S audio codec.
68	GP0_I2C_DAT	DMA_I2C2_SDA	DMA.I2C2.SDA / AY50	IO, 3.3V OD	I2C2 Data. This pin is connected to I2S Audio Codec, Capacitive touch connector, Resistive touch connector, and Expansion Connector3 (J14) 80th Pin.
69	THRM#	THRM#	NA	I, 3.3V CMOS	This pin is connected from Push button (SW6) in carrier board. *Note: This pin is optionally connected to Expansion Connector3 (J14) 20th Pin.*
70	WDTRIG#	Q7_WDTRIG_B	NA	I, 3.3V CMOS	This pin is connected to Expansion connector3 (J14) 17th Pin in carrier board.
71	THRMTRIP#	GPIO_THRMTRIP_Q7(GPIO3_05)	SPI0_CS0 /BC1	O, 3.3V CMOS	Thermal trip. This pin is connected to indication LED D11 and Expansion connector3 (J14) 53rd Pin.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
72	WDOUT	Q7_WDOG_B	NA	O, 3.3V CMOS	This pin is connected to Expansion connector3 (J14) 15th Pin in carrier board.
73	GND	GND	NA	Power	Ground.
74	GND	GND	NA	Power	Ground.
75	USB_P7-/ USB_SSTX0-	USB3_HUB1_TXM	NA	I, USB SS	USB3.0 Host Port0 Transmit Differential pair negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
76	USB_P6-/ USB_SSRX0-	USB3_HUB1_RXM	NA	O, USB SS	USB3.0 Host Port0 Receive Differential pair negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
77	USB_P7+/ USB_SSTX0+	USB3_HUB1_TXP	NA	I, USB SS	USB3.0 Host Port0 Transmit Differential pair positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
78	USB_P6+/ USB_SSRX0+	USB3_HUB1_RXP	NA	O, USB SS	USB3.0 Host Port0 Receive Differential pair positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
79	USB_6_7_OC#	NC	NA	NA	NC in i.MX8 Qseven SOM. Over current sense signal for USB3.0 Host Port0. This pin is connected from USB3.0 Host Port0 Over current indicator.
80	USB_4_5_OC#	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to USB3.0 Host Port1 Over current indicator in carrier board.
81	USB_P5-/ USB_SSTX1-	USB3_HUB3_TXM	NA	I, USB SS	This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
82	USB_P4-/ USB_SSRX1-	USB3_HUB3_RXM	NA	O, USB SS	This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
83	USB_P5+/ USB_SSTX1+	USB3_HUB3_TXP	NA	I, USB SS	NC in I.MX8 Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
84	USB_P4+/ USB_SSRX1+	USB3_HUB3_RXP	NA	O, USB SS	NC in I.MX8 Qseven SOM. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board.
85	USB_2_3_OC#	USB_HUB3_OC/ USB_HUB2_OC	NA	O, 3.3V CMOS	Over current sense signal for USB Host Port2 and Port3. This pin is connected from USB Host Port2 Over current indicator.
86	USB_0_1_OC#	USB_UB1_OC/USB_OTG1_OC(GPIO0_03)	NA	O, 3.3V CMOS/ 10K PU	Over current sense signal for USB Host Port0 and OTG Port1. This pin is connected from Host Port0 and USB OTG Port1 Over current indicator.
87	USB_P3-	USB_HUB3OUT_DM	NA	IO, DIFF	USB 2.0 Host Port3 Data negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board (from the USB HUB output port2 of the I.MX8 SOM).
88	USB_P2-	USB_HUB2OUT_DM	NA	IO, DIFF	USB 2.0 Host Port2 Data negative. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
89	USB_P3+	USB_HUB3OUT_DP	NA	IO, DIFF	USB 2.0 Host Port3 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) top port in carrier board (from the USB HUB output port2 of the I.MX8 SOM).
90	USB_P2+	USB_HUB2OUT_DP	NA	IO, DIFF	USB 2.0 Host Port2 Data positive. This pin is connected to Dual stack USB3.0 TypeA connector (J23) bottom port.
91	USB_VBUS	VBUS_OTG1	USB_OTG1_VBUS/ A39	O, 5V Power	Reference voltage to USB controller.
92	USB_ID	USB_ID	USB_OTG1_ID/ A37	O, 3.3V CMOS	USB OTG ID.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected from Micro USB OTG connector (J2).
93	USB_P1-	USB_OTG1_DM	USB_OTG1_DM / C39	IO, DIFF	USB 2.0 OTG Port1 Data negative. This pin is connected to Micro USB OTG connector (J2).
94	USB_P0-	USB_HUB1OUT_DM	NA	IO, DIFF	USB 2.0 Host Port0 Data negative. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1 of the I.MX8 SOM).
95	USB_P1+	USB_OTG1_DP	USB_OTG1_DP / B40	IO, DIFF	USB 2.0 OTG Port1 Data positive. This pin is connected to Micro USB OTG connector (J2).
96	USB_P0+	USB_HUB1OUT_DP	NA	IO, DIFF	USB 2.0 Host Port0 Data positive. This pin is connected to USB TypeA combo connector (J22) (from the USB HUB output port1 of the I.MX8 SOM).
97	GND	GND	NA	Power	Ground.
98	GND	GND	NA	Power	Ground.
99	eDP0_TX0+/ LVDS_A0+	LVDS1_CH0_TX0_P	LVDS1_CH0_TX0_P/ BN37	LVDS, DIFF	LVDS primary channel differential pair0 positive. This pin is connected to LVDS Receiver.
100	eDP1_TX0+/ LVDS_B0+	LVDS1_CH1_TX0_P	LVDS1_CH1_TX0_P/ BN33	LVDS, DIFF	LVDS secondary channel differential pair0 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
101	eDP0_TX0-/ LVDS_A0-	LVDS1_CH0_TX0_N	LVDS1_CH0_TX0_N/ BL37	LVDS, DIFF	LVDS primary channel differential pair0 negative. This pin is connected to LVDS Receiver.
102	eDP1_TX0-/ LVDS_B0-	LVDS1_CH1_TX0_N	LVDS1_CH1_TX0_N/ BL33	LVDS, DIFF	LVDS secondary channel differential pair0 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
103	eDP0_TX1+/ LVDS_A1+	LVDS1_CH0_TX1_P	LVDS1_CH0_TX1_P/ BM38	LVDS, DIFF	LVDS primary channel differential pair1 positive. This pin is connected to LVDS Receiver.
104	eDP1_TX1+/ LVDS_B1+	LVDS1_CH1_TX1_P	LVDS1_CH1_TX1_P/ BM32	LVDS, DIFF	LVDS secondary channel differential pair1 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
105	eDP0_TX1-/ LVDS_A1-	LVDS1_CH0_TX1_N	LVDS1_CH0_TX1_N/ BK38	LVDS, DIFF	LVDS primary channel differential pair1 negative. This pin is connected to LVDS Receiver.
106	eDP1_TX1-/ LVDS_B1-	LVDS1_CH1_TX1_N	LVDS1_CH1_TX1_N/ BK32	LVDS, DIFF	LVDS secondary channel differential pair1 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
107	eDP0_TX2+/ LVDS_A2+	LVDS1_CH0_TX2_P	LVDS1_CH0_TX2_P/ BN39	LVDS, DIFF	LVDS primary channel differential pair2 positive. This pin is connected to LVDS Receiver.
108	eDP1_TX2+/ LVDS_B2+	LVDS1_CH1_TX2_P	LVDS1_CH1_TX2_P/ BN31	LVDS, DIFF	LVDS secondary channel differential pair2 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
109	eDP0_TX2-/ LVDS_A2-	LVDS1_CH0_TX2_N	LVDS1_CH0_TX2_N/ BL39	LVDS, DIFF	LVDS primary channel differential pair2 negative. This pin is connected to LVDS Receiver.
110	eDP1_TX2-/ LVDS_B2-	LVDS1_CH1_TX2_N	LVDS1_CH1_TX2_N/ BL31	LVDS, DIFF	LVDS secondary channel differential pair2 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
111	LVDS_PPEN	LCD1_VDD_EN(GPIO1_14)	LVDS1_I2C1_SCL/ BD32	I, 3.3V CMOS/ 10K PU	LCD Panel Power Enable.
112	LVDS_BLEN	LCD1_EN(GPIO1_09)	LVDS0_I2C1_SDA/	I, 3.3V CMOS/ 10K PU	LCD Panel Backlight Enable Control.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
			BE35		
113	eDP0_TX3+/ LVDS_A3+	LVDS1_CH0_TX3_P	LVDS1_CH0_TX3_P/ BM40	LVDS, DIFF	LVDS primary channel differential pair3 positive. This pin is connected to LVDS Receiver.
114	eDP1_TX3+/ LVDS_B3+	LVDS1_CH1_TX3_P	LVDS1_CH1_TX3_P/ BM30	LVDS, DIFF	LVDS secondary channel differential pair3 positive. This pin is connected to secondary LVDS connector (J27) in carrier board.
115	eDP0_TX3-/ LVDS_A3-	LVDS1_CH0_TX3_N	LVDS1_CH0_TX3_N/ BK40	LVDS, DIFF	LVDS primary channel differential pair3 negative. This pin is connected to LVDS Receiver.
116	eDP1_TX3-/ LVDS_B3-	LVDS1_CH1_TX3_N	LVDS1_CH1_TX3_N/ BK30	LVDS, DIFF	LVDS secondary channel differential pair3 negative. This pin is connected to secondary LVDS connector (J27) in carrier board.
117	GND	GND	NA	Power	Ground.
118	GND	GND	NA	Power	Ground.
119	eDP0_AUX+/ LVDS_A_CLK+	LVDS1_CH0_CLK_P	LVDS1_CH0_CLK_P/ BM36	LVDS, DIFF	LVDS primary channel differential Clock positive. This pin is connected to LVDS Receiver.
120	eDP1_AUX+/ LVDS_B_CLK+	LVDS1_CH1_CLK_P	LVDS1_CH1_CLK_P/ BM34	LVDS, DIFF	LVDS secondary channel differential Clock positive. This pin is connected to secondary LVDS connector in carrier board.
121	eDP0_AUX-/ LVDS_A_CLK-	LVDS1_CH0_CLK_N	LVDS1_CH0_CLK_N/ BK36	LVDS, DIFF	LVDS primary channel differential Clock negative. This pin is connected to LVDS Receiver.
122	eDP1_AUX-/ LVDS_B_CLK-	LVDS1_CH1_CLK_N	LVDS1_CH1_CLK_N/ BK34	LVDS, DIFF	LVDS secondary channel differential Clock negative. This pin is connected to secondary LVDS connector (J27) in carrier board.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
123	LVDS_BLT_CTRL /GP_PWM_OUT 0	LCD1_BL_PWM(GPIO1_10) [1]	LVDS1_GPIO00/ BD34	I, 3.3V CMOS/ 10K PU	RGB & LVDS LCD Panel Backlight Control.
124	GP_1-Wire_Bus	HDMI_TX0_CEC	HDMI_TX0_CEC / BJ1	O, 3.3V CMOS	This pin is connected to HDMI connector (J24) in carrier board.
125	GP2_I2C_DAT/L VDS_DID_DAT	LVDS1_I2C0_SD A	LVDS1_I2C0_SD A/E33	IO, 3.3V OD/	I2C3 Data. This pin is directly connected to Expansion Connector3 (J14) 35th Pin in carrier board.
126	eDP0_HPD# /LVDS_BLC_DAT	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is directly connected to Expansion Connector3 (J14) 19th Pin in carrier board.
127	GP2_I2C_CLK /LVDS_DID_CLK	LVDS1_I2C0_SC L	LVDS1_I2C0_SC L/BL35	I, 3.3V OD	I2C3 Clock. This pin is directly connected to Expansion Connector3 (J14) 37th Pin in carrier board.
128	eDP1_HPD# /LVDS_BLC_CLK	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is directly connected to Expansion Connector3 (J14) 21st Pin in carrier board.
129	CAN0_TX	FLEXCAN0_TX	FLEXCAN0_TX/H 6	I, 3.3V CMOS	Transmit input for CAN0 bus. This pin is connected to CAN0 Transceiver.
130	CAN0_RX	FLEXCAN0_RX	FLEXCAN0_RX/C 5	O, 3.3V CMOS	Receive output for CAN0 bus. This pin is connected from CAN0 Transceiver.
131	DP_LANE3+/ TMDS_CLK+	HDMI_TX0_CLK _P/EDP3_P	HDMI_TX0_CLK _EDP3_P/BL3	I, HDMI or EDP	HDMI differential data lane clock positive. This pin is connected to HDMI connector (J24) in carrier board.
132	RSVD	USB3_HUB2_TX M	NA	I, USB SS	*Note: This pin is directly connected to Expansion Connector3 (J14) 23rd Pin in carrier board.*
133	DP_LANE3-/ TMDS_CLK-	HDMI_TX0_CLK _N/EDP3_N	HDMI_TX0_CLK _EDP3_N/BK2	I, HDMI or EDP	HDMI differential data clock negative. This pin is connected to HDMI connector (J24) in carrier board.
134	RSVD	USB3_HUB2_TX P	NA	I, USB SS	*Note: This pin is directly connected to Expansion Connector3 (J14) 25th Pin in carrier board.*

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
135	GND	GND	NA	Power	Ground.
136	GND	GND	NA	Power	Ground.
137	DP_LANE1+/ TMDS_LANE1+	HDMI_TX0_DATA1_P/EDP1_P	HDMI_TX0_DATA1_EDP1_P /BL7	I, HDMI or EDP	HDMI differential data lane 1 positive. This pin is connected to HDMI connector (J24) in carrier board.
138	DP_AUX+	EDP_AUX_P	HDMI_TX0_AUX_P / BH2	I, EDP	Note: This pin is directly connected to Expansion Connector3 (J14) 52nd Pin in carrier board.
139	DP_LANE1-/ TMDS_LANE1-	HDMI_TX0_DATA1_N/EDP1_N	HDMI_TX0_DATA1_EDP1_N /BM6	I, HDMI or EDP	HDMI differential data lane 1 negative. This pin is connected to HDMI connector (J24) in carrier board.
140	DP_AUX-	EDP_AUX_N	HDMI_TX0_AUX_N / BG3	I, EDP	Note: This pin is directly connected to Expansion Connector3 (J14) 54th Pin in carrier board.
141	GND	GND	NA	Power	Ground.
142	GND	GND	NA	Power	Ground.
143	DP_LANE2+/ TMDS_LANE0+	HDMI_TX0_DATA0_P/EDP2_P	HDMI_TX0_DATA0_EDP2_P /BL5	I, HDMI or EDP	NC in I.MX8 Qseven SOM. HDMI differential data lane 0 positive. This pin is connected to HDMI connector (J24) in carrier board.
144	RSVD	USB3_HUB2_RXM	NA	O, USB SS	*Note: This pin is directly connected to Expansion Connector3 (J14) 29th Pin in carrier board.*
145	DP_LANE2-/ TMDS_LANE0-	HDMI_TX0_DATA0_N/EDP2_N	HDMI_TX0_DATA0_EDP2_N /BM4	I, HDMI or EDP	NC in I.MX8 Qseven SOM. HDMI differential data lane 0 negative. This pin is connected to HDMI connector (J24) in carrier board.
146	RSVD	USB3_HUB2_RXP	NA	O, USB SS	*Note: This pin is directly connected to Expansion Connector3 (J14) 31st Pin in carrier board.*
147	GND	GND	NA	Power	Ground.
148	GND	GND	NA	Power	Ground.
149	DP_LANE0+/ TMDS_LANE2+	HDMI_TX0_DATA2_P/EDP0_P	HDMI_TX0_DATA2_EDP0_P /BL9	I, HDMI or EDP	HDMI differential data lane 2 positive. This pin is connected to HDMI connector (J24) in carrier board.
150	HDMI_CTRL_DAT	HDMI_TX0_CTRL_DAT	HDMI_TX0_DDC_SDA/	IO, 3.3V CMOS	HDMI I2C Data.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
			BN5		This pin is connected to HDMI connector (J24) in carrier board.
151	DP_LANE0-/ TMDS_LANE2-	HDMI_TX0_DATA2_N/EDP0_N	HDMI_TX0_DATA2_EDP0_N /BM8	I, HDMI or EDP	HDMI differential data lane 2 negative. This pin is connected to HDMI connector (J24) in carrier board.
152	HDMI_CTRL_CLK	HDMI_TX0_CTRL_CLK	HDMI_TX0_DDC_SCL/ BG1	I, 3.3V CMOS	HDMI I2C Clock. This pin is connected to HDMI connector (J24) in carrier board.
153	DP_HDMI_HPD#	HDMI_TX_HPD	HDMI_TX0_HPD / BH8	O, 3.3V CMOS	HDMI hot plug detect. This pin is connected to HDMI connector (J24) in carrier board.
154	RSVD	NC	NA	NA	NC in i.MX8 Qseven SOM. Note: This pin is directly connected to Expansion Connector3 (J14) 39th Pin in carrier board.
155	PCIE_CLK_REF+	PCIE_A_REFCLK_P	NA	I, PCIe	PCIe differential reference clock positive. This pin is connected to PCIe clock buffer.
156	PCIE_WAKE#	PCIE_A_WAKE_B(GPIO4_28)	PCIE_CTRL0_WAKE_B/ A15	O, 3.3V CMOS/ 10K PU	PCIe wake event. This pin is connected to PCIe x 4 connector (J4) and Mini PCIe connector(J26).
157	PCIE_CLK_REF-	PCIE_A_REFCLK_N	NA	I, PCIe	PCIe differential reference clock negative. This pin is connected to PCIe clock buffer.
158	PCIE_RST#	PCIE_A_RST_B (GPIO4_29) [1]	PCIE_CTRL0_PERST_B/ D20	I, 3.3V CMOS	PCIe reset. This pin is connected to PCIe x 4 connector (J7) and Mini PCIe connector (J26).
159	GND	GND	NA	Power	Ground.
160	GND	GND	NA	Power	Ground.
161	PCIE3_TX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
162	PCIE3_RX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
163	PCIE3_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to PCIex4 connector (J4) in carrier board.
164	PCIE3_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
165	GND	GND	NA	Power	Ground.
166	GND	GND	NA	Power	Ground.
167	PCIE2_TX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
168	PCIE2_RX+	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
169	PCIE2_TX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
170	PCIE2_RX-	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to PCIex4 connector (J4) in carrier board.
171	UART0_TX	UART0_TX	UART0_TX /AV48	I, 3.3V CMOS	SCIFB2 interface serial data transmitter. This pin is connected to Data UART Header (J1) 05th Pin.
172	UART0_ RTS #	UART0_RTS_B	UART0_RTS_B /AU45	I, 3.3V CMOS	SCIFB2 interface ready to receive handshake signal. This pin is connected to Data UART Header (J1) 06th Pin.
173	PCIE1_TX+	PCIE1_B_TX0_P	PCIE1_TX0_P /B24	I, PCIe	This pin is connected to PCIex4 connector (J7) in carrier board.
174	PCIE1_RX+	PCIE1_B_RX0_P	PCIE1_RX0_P /A21	O, PCIe	This pin is connected to PCIex4 connector (J7) in carrier board.
175	PCIE1_TX-	PCIE1_B_TX0_N	PCIE1_TX0_N /C25	I, PCIe	This pin is connected to PCIex4 connector (J7) in carrier board.
176	PCIE1_RX-	PCIE1_B_RX0_N	PCIE1_RX0_N /B22	O, PCIe	This pin is connected to PCIex4 connector (J7) in carrier board.
177	UART0_RX	UART0_RX	UART0_RX /AV50	O, 3.3V CMOS	SCIFB2 interface serial data receiver. This pin is connected from Data UART Header (J1) 04th Pin.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
178	UART0_CTS#	UART0_CTS_B	UART0_CTS_B /AW49	O, 3.3V CMOS	SCIFB2 interface ready to send handshake signal. This pin is connected from Data UART Header (J1) 02nd Pin.
179	PCIE0_TX+	PCIE0_A_TX0_P	PCIE0_TX0_P /B26	I, DIFF	PCIe Channel0 Transmit data output positive. This pin is connected to PCIe x 4 connector (J7) or Mini PCIe connector (J26) through PCIe Switch.
180	PCIE0_RX+	PCIE0_A_RX0_P	PCIE0_RX0_P /A29	O, DIFF	PCIe Channel0 Receive data input positive. This pin is connected to PCIe x 4 connector (J7) or Mini PCIe connector (J26) through PCIe Switch.
181	PCIE0_TX-	PCIE0_A_TX0_N	PCIE0_TX0_N /C27	I, DIFF	PCIe Channel0 Transmit data output negative. This pin is connected to PCIe x 4 connector (J7) or Mini PCIe connector (J26) through PCIe Switch.
182	PCIE0_RX-	PCIE0_A_RX0_N	PCIE0_RX0_N /B30	O, DIFF	PCIe Channel0 Receive data input negative. This pin is connected to PCIe x 4 connector (J7) or Mini PCIe connector (J26) through PCIe Switch.
183	GND	GND	NA	Power	Ground.
184	GND	GND	NA	Power	Ground.
185	LPC_AD0/ GPIO0	Q7_GPIO_0(GPIO3_12)	SAI1_RXC/AV6	IO,3.3VCMOS/ 10K PU	General purpose Input/Output0. This GPIO is used for Touch Interrupt and connected from Capacitive Touch Connector or Resistive Touch Controller. *Note: This pin is also connected to* Expansion Connector3 (J14) *36th Pin through resistor and default populated.*
186	LPC_AD1/ GPIO1	Q7_GPIO_1(GPIO3_02)	SPI0_SCK/BB4	IO,3.3VCMOS/ 10K PU	General purpose Input/Output1.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					This pin is connected to Expansion Connector3 (J14) 34th Pin through resistor. *Note: This pin is also connected to Mini PCIe connector (J26) 20th Pin through resistor and default populated.*
187	LPC_AD2 / GPIO2	Q7_GPIO_2(GPIO3_14)	SAI1_RXFS/AU3	IO,3.3VCMOS/ 10K PU	General purpose Input/Output2. This GPIO is used for Mic Input Detect and connected from Audio IN Jack. *Note: This pin is also connected to Expansion connector3 (J14) 45th Pin through resistor and default populated.*
188	LPC_AD3/ GPIO3	Q7_GPIO_3(GPIO3_11)	SPI2_CS1/AY2	IO,3.3VCMOS/ 10K PU	General purpose Input/Output3. This GPIO is used for Headphone Detect and connected from Audio Out Jack. *Note: This pin is also connected to Expansion connector3 (J14) 41st Pin through resistor and default populated.*
189	LPC_CLK/ GPIO4	Q7_GPIO_4(GPIO1_08)	LVDS0_I2C1_SCL/BE37	IO, 3.3V CMOS	General purpose Input/Output4. This GPIO is used for CAN0 Transceiver Power down control and connected to CAN transceiver. *Note: This pin is also connected to Expansion connector3 (J14) 47th Pin.*
190	LPC_FRAME#/ GPIO5	Q7_GPIO_5(GPIO1_11)	LVDS1_GPIO01/ BH36	IO,3.3VCMOS/ 10K PU	LVDS LCD Panel Backlight Enable Control. *Note: Also, this pin is connected to Expansion Connector3 (J14) 44th Pin through resistor and default populated.*
191	SERIRQ / GPIO6	Q7_GPIO_6(GPIO5_00)	PCIE_CTRL1_PERST_B/G25	IO,3.3VCMOS/ 10K PU	LVDS LCD Panel Power Enable. *Note: Also, this pin is connected to Expansion Connector3 (J14) 40th Pin through resistor and default populated.*

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
192	LPC_LDRQ#/ GPIO7	Q7_GPIO_7(GPIO0_00)	LSIO.GPIO0.IO00/AL45	IO, 3.3V CMOS	General purpose Input/Output7. *Note: This pin is connected to Expansion Connector3 (J14) 09th Pin through resistor and default populated.*
193	VCC_RTC	VDD_RTC	NA	O, 3V Power	3V backup coin cell input for RTC.
194	SPKR/ GP_PWM_OUT2	PWM2(GPIO0_19) [1]	LSIO.GPIO0.IO19/ BA51	I, 3.3V CMOS	Buzzer control PWM input. This pin is connected to buzzer in carrier board. *Note: Also, this pin is used as a GPIO for LVDS LCD Backlight control through resistor and default populated.*
195	FAN_TACHOIN/ GP_TIMER_IN	Q7_FAN_TECHOIN(GPIO0_01)	LSIO.GPIO0.IO01/AP48	I, 3.3V CMOS	This pin is connected to Fan Header (J19) 04th Pin in carrier board.
196	FAN_PWMOUT/ GP_PWM_OUT1	PWM3(GPIO0_16) [1]	PWM3(GPIO0_16)/ AW53	I, 3.3V CMOS	Fan Control PWM input. This pin is connected to Fan Header (J19) 2nd Pin.
197	GND	GND	NA	Power	Ground.
198	GND	GND	NA	Power	Ground.
199	SPI_MOSI	SPI3_MOSI [1]	SPI3_MOSI/ BF2	I, 3.3V CMOS	SPI Master Out Slave In. This Pin is connected to SPI Flash. *Note: This pin is also connected to Expansion connector3 (J14) 48th Pin.*
200	SPI_CS0#	SPI3_CS0	SPI3_CS0/BG5	I, 3.3V CMOS/ 10K PU	SPI Chip Select1. This Pin is connected to SPI Flash.
201	SPI_MISO	SPI3_MISO	SPI3_MISO/BE5	O, 3.3V CMOS	SPI Master In Slave Out. This Pin is connected from SPI Flash. *Note: This pin is also connected to Expansion connector3 (J14) 46th Pin.*
202	SPI_CS1#	SPI3_CS1 [1]	SPI3_CS1/BD8	I, 3.3V CMOS	SPI Chip Select2. This pin is also connected to Expansion connector3 (J14) 49th Pin.
203	SPI_SCK	SPI3_SCLK	SPI3_SCLK/BF6	I, 3.3V CMOS	SPI Clock. This Pin is connected to SPI Flash. *Note: This pin is also connected to Expansion connector3 (J14) 51st Pin.*

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
204	MFG_NC4	NC	NA	NA	NC in i.MX8 Qseven SOM. JTAG Test Reset. This pin is connected from JTAG Header (J16) 03rd Pin through buffer.
205	VCC_5V_SB	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to 5V standby power supply in carrier board.
206	VCC_5V_SB	NC	NA	NA	NC in i.MX8 Qseven SOM. This pin is connected to 5V standby power supply in carrier board.
207	MFG_NC0	JTAG_TCK	JTAG_TCK/ BC51	O, 3.3V CMOS/ 10K PD	JTAG Test Clock. This pin is connected from JTAG Header (J16) 09th Pin through buffer.
208	MFG_NC2	UART4_RX/JTAG_TDI	DMA.UART4.RX /AR47 or JTAG_TDI/ BE51	O, 3.3V CMOS	SCIFA2 serial data receiver. This pin is connected from Serial to USB converter for Debug console. *Note: This pin is also connected to JTAG Header (J16) 05th Pin (JTAG_TDI) through buffer.*
209	MFG_NC1	UART4_TX/JTDO_UTX	DMA.UART4.TX/ AU53 or JTAG_TDO/BD52	I, 3.3V CMOS	SCIFA2 serial data transmitter. This pin is connected to Serial to USB converter for Debug console. *Note: This pin is also connected to JTAG Header (J16) 13th Pin (JTAG_TDO) through buffer.*
210	MFG_NC3	JTAG_TMS	JTAG_TMS/BA49	O, 3.3V CMOS/ 10K PU	JTAG Test Mode Select. This pin is connected from JTAG Header (J16) 07th Pin through buffer.
211	VCC	NC	NA	O, 5V Power	Supply Voltage.
212	VCC	NC	NA	O, 5V Power	Supply Voltage.
213	VCC	NC	NA	O, 5V Power	Supply Voltage.
214	VCC	NC	NA	O, 5V Power	Supply Voltage.
215	VCC	NC	NA	O, 5V Power	Supply Voltage.
216	VCC	NC	NA	O, 5V Power	Supply Voltage.
217	VCC	NC	NA	O, 5V Power	Supply Voltage.
218	VCC	NC	NA	O, 5V Power	Supply Voltage.
219	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
220	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.

Pin No.	Qseven MXM Connector Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
221	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
222	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
223	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
224	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
225	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
226	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
227	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
228	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
229	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.
230	VCC	VCC_5V	NA	O, 5V Power	Supply Voltage.

2.4 Serial Interface Features

2.4.1 Debug UART Interface

The i.MX8 QM/QP Qseven development board supports debug interface through i.MX8 CPU's UART4 interface. This UART4 signals from Qseven MXM connector is connected to UART to USB Convertor "FT232RQ" and connected to USB Micro AB Connector (J3). This USB Micro AB Connector can be used for Debug purpose which is physically located at the top of the board as shown below.

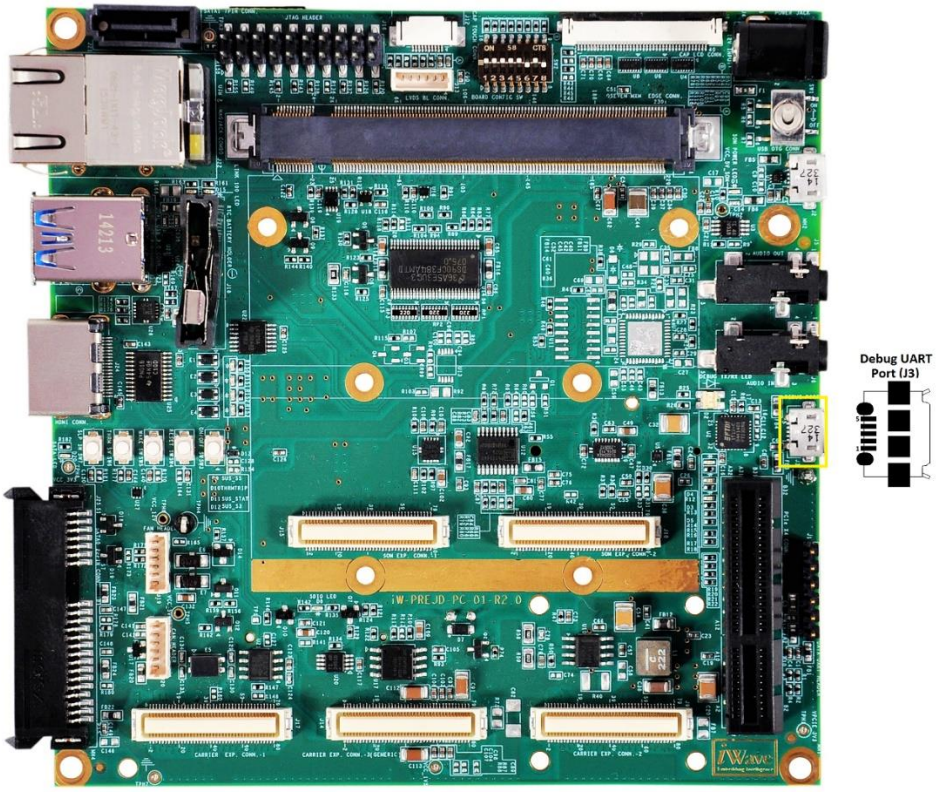

Figure 3: Debug UART Port

2.4.2 Data UART Interface

The i.MX8 QM/QP Qseven carrier board supports full functional Data UART interface through i.MX8 CPU's UART0 interface. This UART0 signals from Qseven MXM connector is connected to 6pin Header (J1) for easy accessibilty. This Data UART header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 5-146280-6 from TE Connectivity

Mating Connector : 534237-4 from TE Connectivity

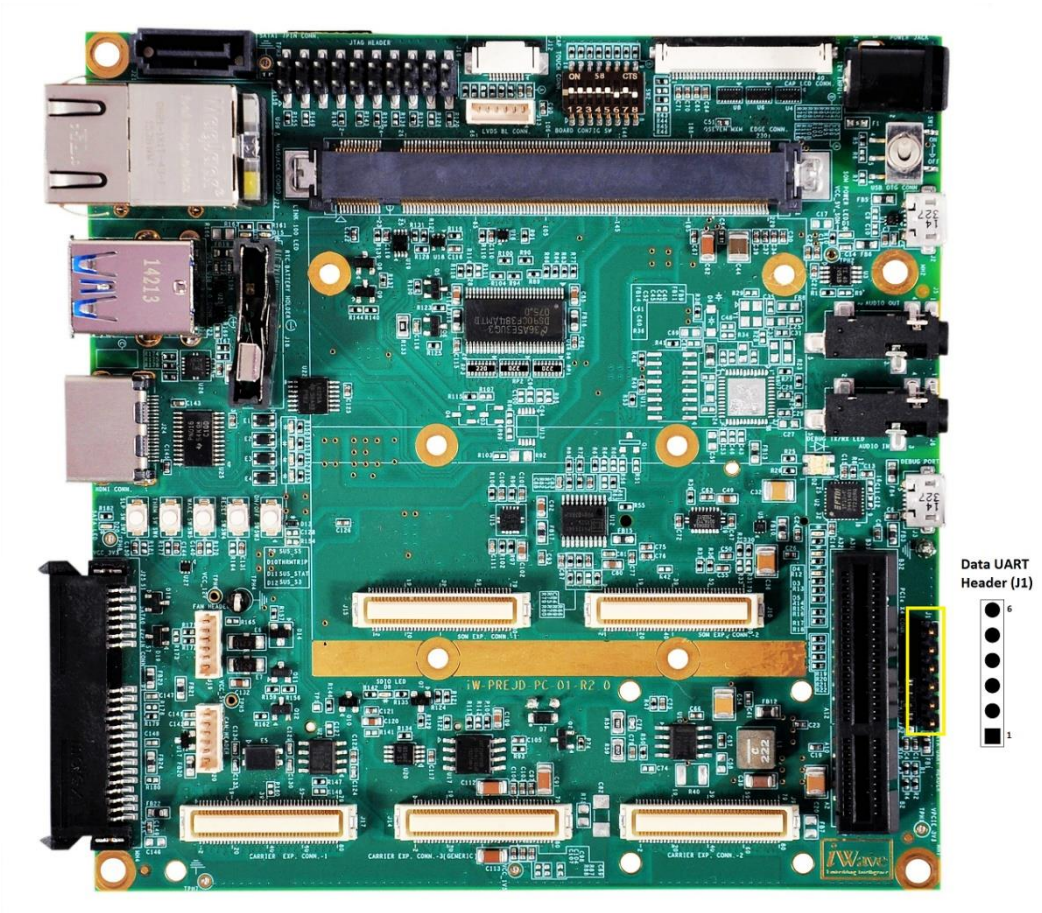

Figure 4: Data UART Header

Table 4: Data UART Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	GND	GND	Power	Ground.
2	UART_CTS#	UART0_CTS_B	O, 3.3V CMOS	UART0 interface Clear to Send signal.
3	VCC_3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
4	UART_RXD	UART0_RX	I, 3.3V CMOS	UART0 interface Receive signal.
5	UART_TXD	UART0_TX	O, 3.3V CMOS	UART0 interface Transmit signal.
6	UART_RTS#	UART0_RTS_B	I, 3.3V CMOS	UART0 interface Ready to Send signal.

2.5 High Speed Interface Features

2.5.1 PCIe Interface

The i.MX8 QM/QP Qseven Development platform by default supports two PCIe Lanes PCIe0 and PCIe1. PCIe0 lane supported through i.MX8 CPU's PCIe0 Interface and other PCIe1 lane supported through i.MX8 CPU's PCIe1 Interface

Both PCIe 0 signals of Qseven MXM connector are connected to separate 1:2 Multiplexer/Demultiplexer switch and the output of both the Multiplexer/Demultiplexer switch are connected to PCIex4 connector and other one to Mini-PCIe connector. The selection between PCIex4 connector and Mini-PCIe connector can be done by setting the 6th bit of Board configuration switch (SW2) to appropriate position. PCIe reference clock from Qseven MXM connector is connected to 1:2 output clock buffer and then connected to PCIex4 connector and Mini PCIe connector for clock reference.

If the 6th bit of Board configuration switch is set to ON position, then PCIe channel0 of Qseven MXM connector is connected to PCIex4 connector which is physically located at the top of the board as shown below.

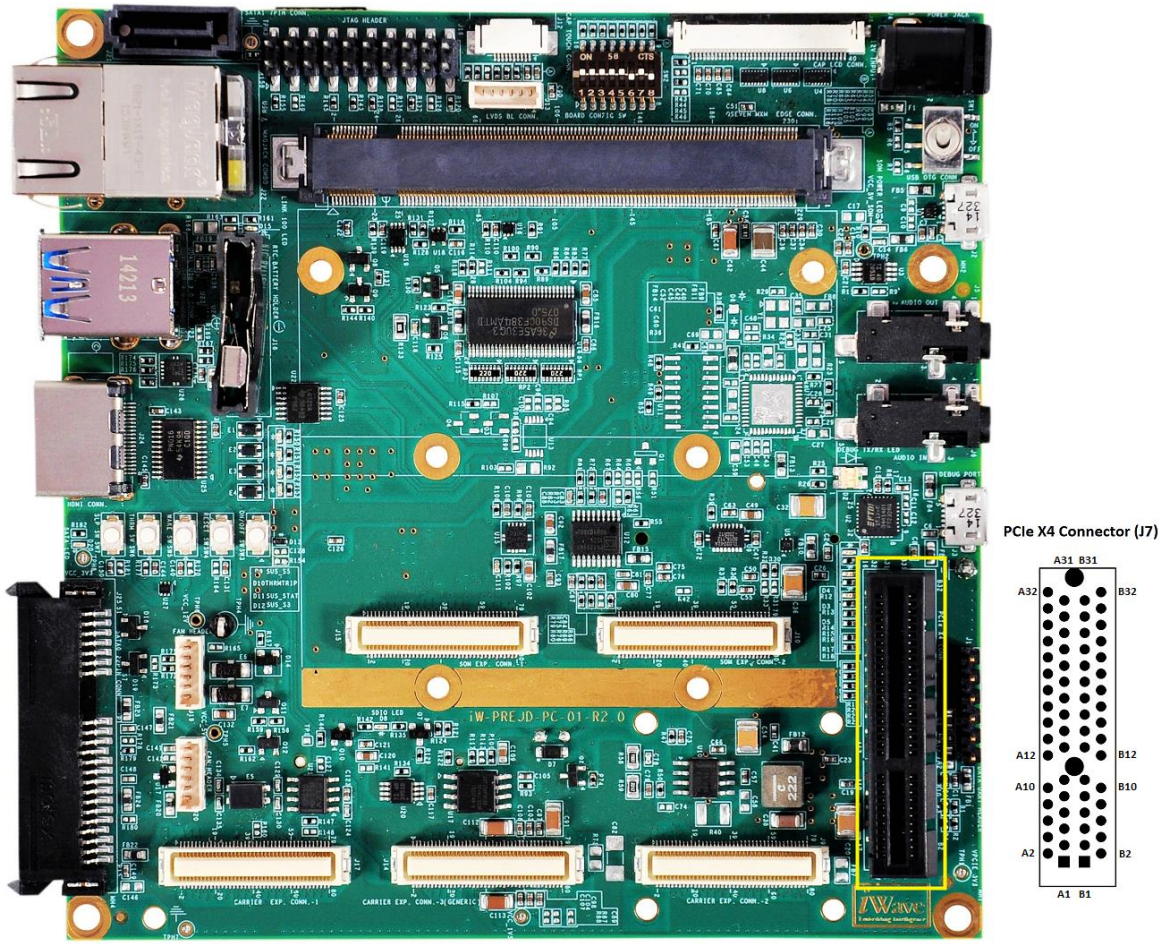

Figure 5: PCIex4 Connector

Table 5: PCIex4 Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A4	GND	GND	Power	Ground.
B4	GND	GND	Power	Ground.
A5	TCK	NC	NA	NC.
B5	SMCLK	DMA_I2C1_SCL	O, 3.3V CMOS	SMB Clock.
A6	TDI	NC	-	NC.
B6	SMDAT	DMA_I2C1_SDA	IO, 3.3V CMOS	SMB Data.
A7	TDO	NC	-	NC.
B7	GND	GND	Power	Ground.
A8	TMS	NC	-	NC.
B8	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
A9	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NC	-	NC.
A10	+3.3V	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
B10	3V3AUX	VAUX_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	PCIE_A_RST_B(GPIO4_29)	O, 3.3V CMOS	PCIe PERST#.
B11	WAKE#	PCIE_A_WAKE_B(GPIO4_28)	O, 3.3V CMOS	PCIe WAKE#.
A12	GND	GND	Power	Ground.
B12	RSVD2	NC	-	NC, Reserved Pin.
A13	PCIe0_CLK+	PCIe0_CLK+	O, PCIe	PCIe Clock positive. *Note: PCIe0_CLK+ FROM 1:2 output clock buffer*
B13	GND	GND	Power	Ground.
A14	PCIe0_CLK-	PCIe0_CLK-	O, PCIe	PCIe Clock negative. *Note: PCIe0_CLK- FROM 1:2 output clock buffer*
B14	PCIE0_TX+	PCIE0_A_TX0_P	O, PCIe	PCIe Port 0 Transmit pair positive. *Note: Refer SW2 setting from* ***Error! Reference source not found.*** *to support PCIE0_TX.*
A15	GND	GND	Power	Ground.
B15	PCIE0_TX-	PCIE0_A_TX0_N	O, PCIe	PCIe Port 0 Transmit pair negative.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
				*Note: Refer SW2 setting from **Error! Reference source not found.** to support PCIE0_TX.*
A16	PCIE0_RX+	PCIE0_A_RX0_P	I, PCIe	PCIe Port 0 Receive pair positive. *Note: Refer SW2 setting from **Error! Reference source not found.** to support PCIE0_RX.*
B16	GND	GND	Power	Ground.
A17	PCIE0_RX-	PCIE0_A_RX0_N	I, PCIe	PCIe Port 0 Receive pair negative. *Note: Refer SW2 setting from table to support PCIE0_RX.*
B17	PRSNT2#	NC	-	NC.
A18	GND	GND	Power	Ground.
B18	GND	GND	Power	Ground.
A19	RSVD	NC	-	NC, Reserved Pin.
B19	PCIE1_TX+	PCIE1_B_TX0_P	O, PCIe	PCIe Port 1 Transmit pair positive.
A20	GND	GND	Power	Ground.
B20	PCIE1_TX-	PCIE1_B_TX0_N	O, PCIe	PCIe Port 1 Transmit pair negative.
A21	PCIE1_RX+	PCIE1_B_RX0_P	I, PCIe	PCIe Port 1 Receive pair positive.
B21	GND	GND	Power	Ground.
A22	PCIE1_RX-	PCIE1_B_RX0_N	I, PCIe	PCIe Port 1 Receive pair negative.
B22	GND	GND	Power	Ground.
A23	GND	GND	Power	Ground.
B23	PCIE2_TX+	NC	-	NC, PCIe Port 2 Transmit pair positive.
A24	GND	GND	Power	Ground.
B24	PCIE2_TX-	NC	-	NC, PCIe Port 2 Transmit pair negative.
A25	PCIE2_RX+	NC	-	NC, PCIe Port 2 Receive pair positive.
B25	GND	GND	Power	Ground.
A26	PCIE2_RX-	NC	-	NC, PCIe Port 2 Receive pair negative.
B26	GND	GND	Power	Ground.
A27	GND	GND	Power	Ground.
B27	PCIE3_TX+	NC	-	NC, PCIe Port 3 Transmit pair positive.
A28	GND	GND	Power	Ground.
B28	PCIE3_TX-	NC	-	NC, PCIe Port 3 Transmit pair negative.
A29	PCIE3_RX+	NC	-	NC, PCIe Port 3 Receive pair positive.
B29	GND	GND	Power	Ground.
A30	PCIE3_RX-	NC	-	NC, PCIe Port 3 Receive pair negative.
B30	RSVD	NC	-	NC, Reserved Pin.
A31	GND	GND	Power	Ground.
B31	PRSNT3#	NC	-	NC.
A32	RSVD	NC	-	NC, Reserved Pin.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
B32	GND	GND	Power	Ground.

If the 6th bit of Board configuration switch (SW2) is set to OFF position, then PCIe channel0 of Qseven MXM connector is connected to Mini PCIe connector which is physically located at the bottom of the board as shown below.

Mini PCIe Connector: Mini PCIe connector (J26) is physically located at the bottom of the board as shown below.

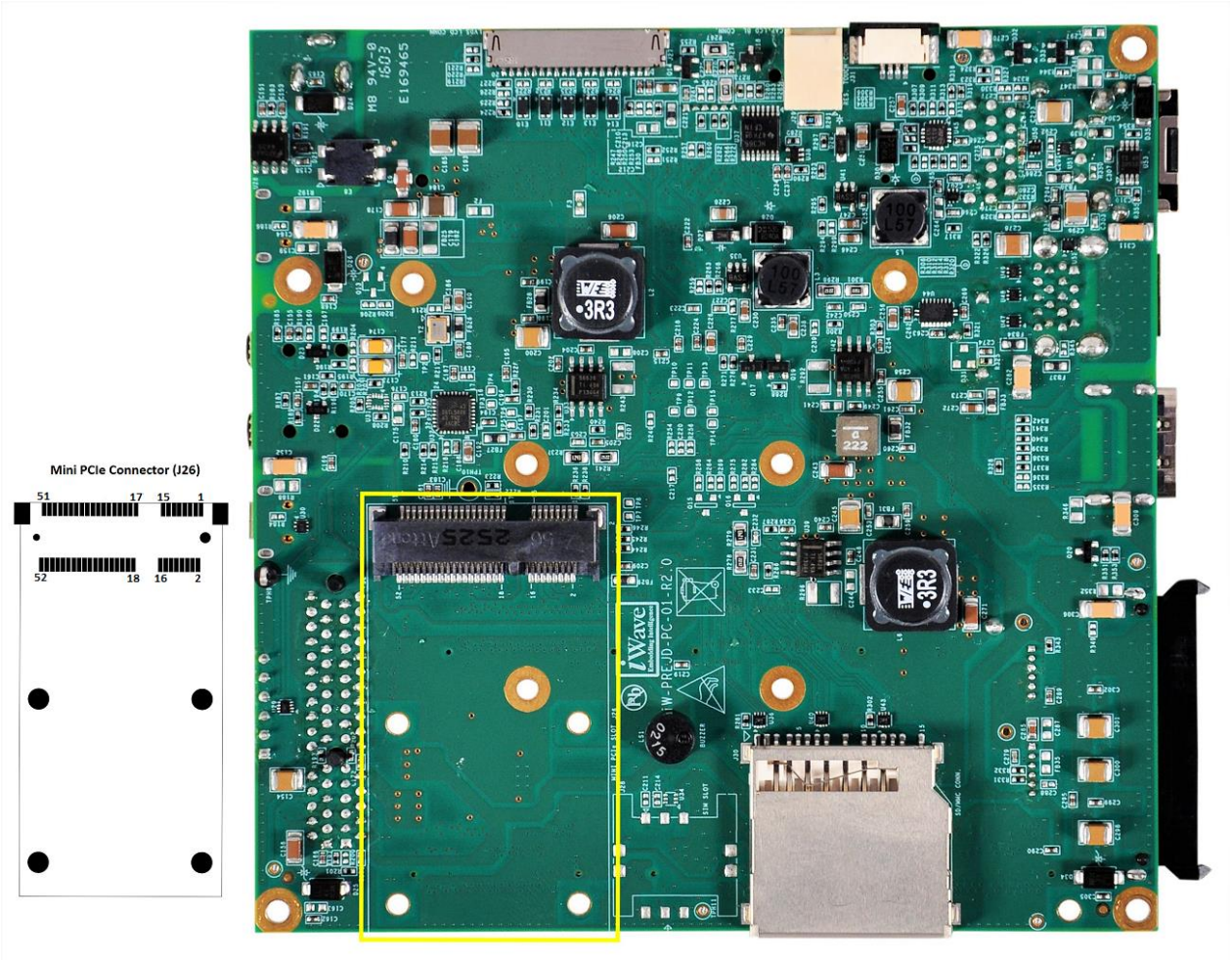

Figure 6: Mini PCIe Connector

Table 6: Mini-PCIe Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	PCIe_WAKE	PCIE_A_WAKE_B(GPIO4_28)	O, 3.3V CMOS	PCIe WAKE#.
2	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
3	COEX1	NC.	-	NC.
4	GND	GND	Power	Ground.
5	COEX2	NC.	-	NC.
6	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
7	CLK_REQ#	CLK_REQ#	O, 3.3V CMOS	Used to enable Clock.
8	UIM_PWR	NC.	-	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
9	GND	GND	Power	Ground.
10	UIM_DATA	NC.	-	NC.
11	REFCLK-	PCIe1_CLK	O, DIFF	PCIe Clock negative. *Note: PCIe1_CLK- FROM 1:2 output clock buffer*
12	UIM_CLK	NC.	-	NC.
13	REFCLK+	PCIe1_CLK+	O, DIFF	PCIe Clock positive. *Note: PCIe1_CLK+ FROM 1:2 output clock buffer*
14	UIM_RESET	NC.	-	NC.
15	GND	GND	Power	Ground.
16	UIM_VPP	NC.	-	NC.
17	RESERVED	NC.	-	NC.
18	GND	GND	Power	Ground.
19	RESERVED	NC.	-	NC.
20	W_DISABLEG	Q7_GPIO_1(GPIO3_02)	O, 3.3V CMOS	Wireless Disable.
21	GND	GND	Power	Ground.
22	PERST#	PCIE_A_RST_B(GPIO4_29)	O, 3.3V CMOS	PCIe Reset.
23	PCIE0_RX-	PCIE0_A_RX0_N	I, DIFF	PCIe Port0/1 Receive pair negative. *Note: Refer SW2 setting from **Error! Reference source not found.** for support PCIE0_RX-.*
24	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
25	PCIE0_RX+	PCIE0_A_RX0_P	I, DIFF	PCIe Port0/1 Receive pair positive. *Note: Refer SW2 setting from **Error! Reference source not found.** for support PCIE0_RX+.*
26	GND	GND	Power	Ground.
27	GND	GND	Power	Ground.
28	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
29	GND	GND	Power	Ground.
30	SMB_CLK	DMA_I2C1_SCL	O, 3.3V CMOS	SMB Clock.
31	PCIE0_TX-	PCIE0_A_TX0_N	O, DIFF	PCIe Port0/1 Transmit pair negative. *Note: Refer SW2 setting from **Error! Reference source not found.** for support PCIE0_TX-.*
32	SMB_DATA	DMA_I2C1_SDA	IO, 3.3V CMOS	SMB DATA.
33	PCIE0_TX+	PCIE0_A_TX0_P	O, DIFF	PCIe Port0/1 Transmit pair positive. *Note: Refer SW2 setting from **Error! Reference source not found.** for support PCIE0_TX+.*
34	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
35	GND	GND	Power	Ground.
36	USB_D-	NC.	NA	NC.
37	GND	GND	Power	Ground.
38	USB_D+	NC.	NA	NC.
39	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
40	GND	GND	Power	Ground.
41	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.
42	LED_WWAN#	LED_WWAN#	O, 3.3V CMOS	Connected to D4 Green LED cathode.
43	GND	GND	Power	Ground.
44	LED_WLAN#	LED_WLAN#	O, 3.3V CMOS	Connected to D5 Green LED cathode.
45	RESERVED	NC.	-	NC.
46	LED_WPAN#	LED_WPAN#	O, 3.3V CMOS	Connected to D3 Green LED cathode.
47	RESERVED	NC.	-	NC.
48	1.5V	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
49	RESERVED	NC.	-	NC.
50	GND	GND	Power	Ground.
51	RESERVED	NC.	-	NC.
52	+3.3V_aux	VPCIe_3V3	O, 3.3V Power	3.3V Supply Voltage.

2.5.2 SATA Interface

The i.MX8 QM/QP Qsevn carrier board supports SATA interface from PCIE_SATA0 of i.MX8 QM/QP processor using 22 pins SATA connector (J25). The Qsevn carrier board also supports SATA activity LED (D20) on Top side of the board for SATA activity indication. This 22 Pins SATA connector is physically located at the top of the board.

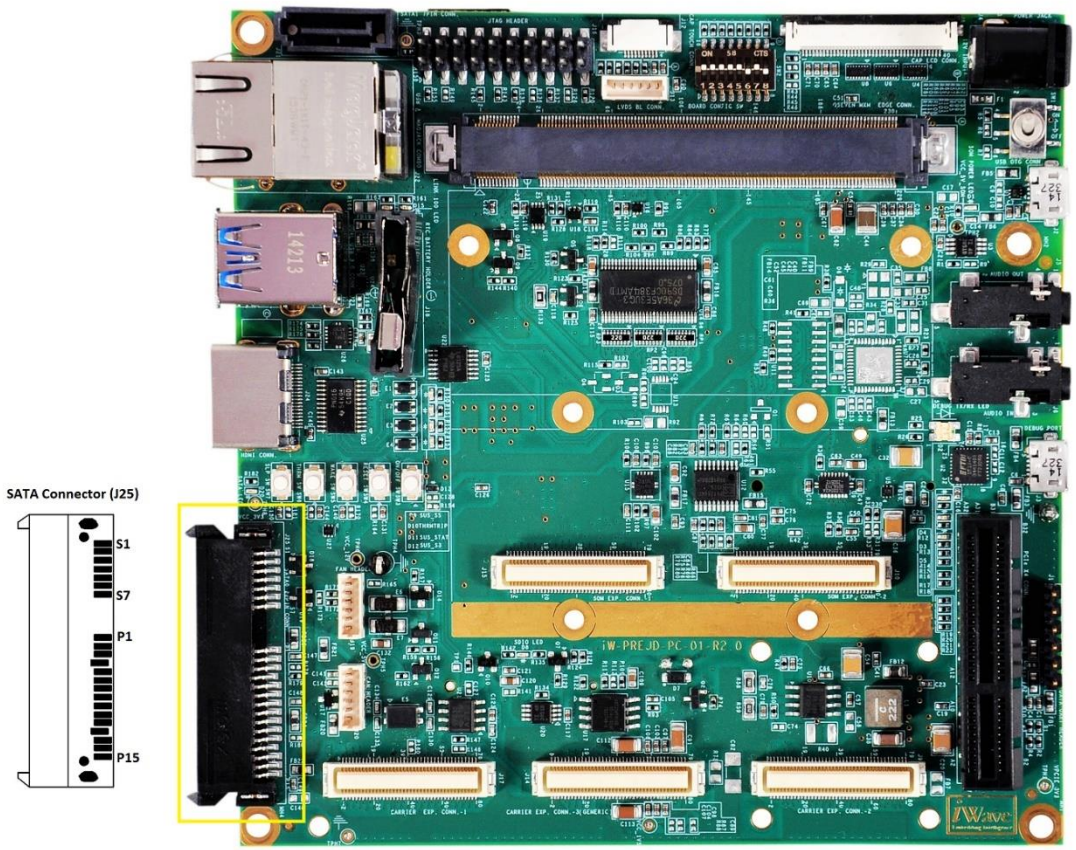

Figure 7: SATA Connector

Refer below table for the pinout is listed of SATA connector.

Table 7: 22 pins SATA Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
S1	GND	GND	Power	Ground.
S2	SATA1_TXP	PCIE_SATA0_TX0_P	O, SATA	SATA Transmit Differential pair positive.
S3	SATA1_TXN	PCIE_SATA0_TX0_N	O, SATA	SATA Transmit Differential pair negative.
S4	GND	GND	Power	Ground.
S5	SATA1_RXN	PCIE_SATA0_RX0_N	I, SATA	SATA Receive Differential pair negative.
S6	SATA1_RXP	PCIE_SATA0_RX0_P	I, SATA	SATA Receive Differential pair positive.
S7	GND	GND	Power	Ground.
P1	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P2	V33	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
P3	V33	Q7_GPIO_7(GPIO0_00)	I, 3.3V CMOS	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
P4	GND	GND	Power	Ground.
P5	GND	GND	Power	Ground.
P6	GND	GND	Power	Ground.
P7	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P8	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P9	V5	VCC_5V	O, 5V Power	5V Supply Voltage.
P10	GND	GND	Power	Ground.
P11	DAS_DSS	NC	NA	NC.
P12	GND	GND	Power	Ground.
P13	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P14	V12	VCC_12V	O, 12V Power	12V Supply Voltage.
P15	V12	VCC_12V	O, 12V Power	12V Supply Voltage.

2.5.3 USB3.0 Host Interface

The i.MX 8 QM/QP Qseven carrier board supports Super Speed USB3.0 Host interface through on SOM USB3.0 Hub. This USB3.0 Port0 signals of Qseven MXM connector is directly connected to bottom port of dual stack USB3.0 TypeA connector (J23). Also, USB2.0 Port2 signals of Qseven MXM connector is connected to this connector for USB2.0 host interface from 3.0 USB Hub used on SOM.

The VBUS power of this USB3.0 connector is connected through current limit power switch and limit is set as 900mA. If connected USB3.0 device takes more than 900mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 6 & 7. This USB3.0 connector (J23) is physically located at the top of the board as shown below.

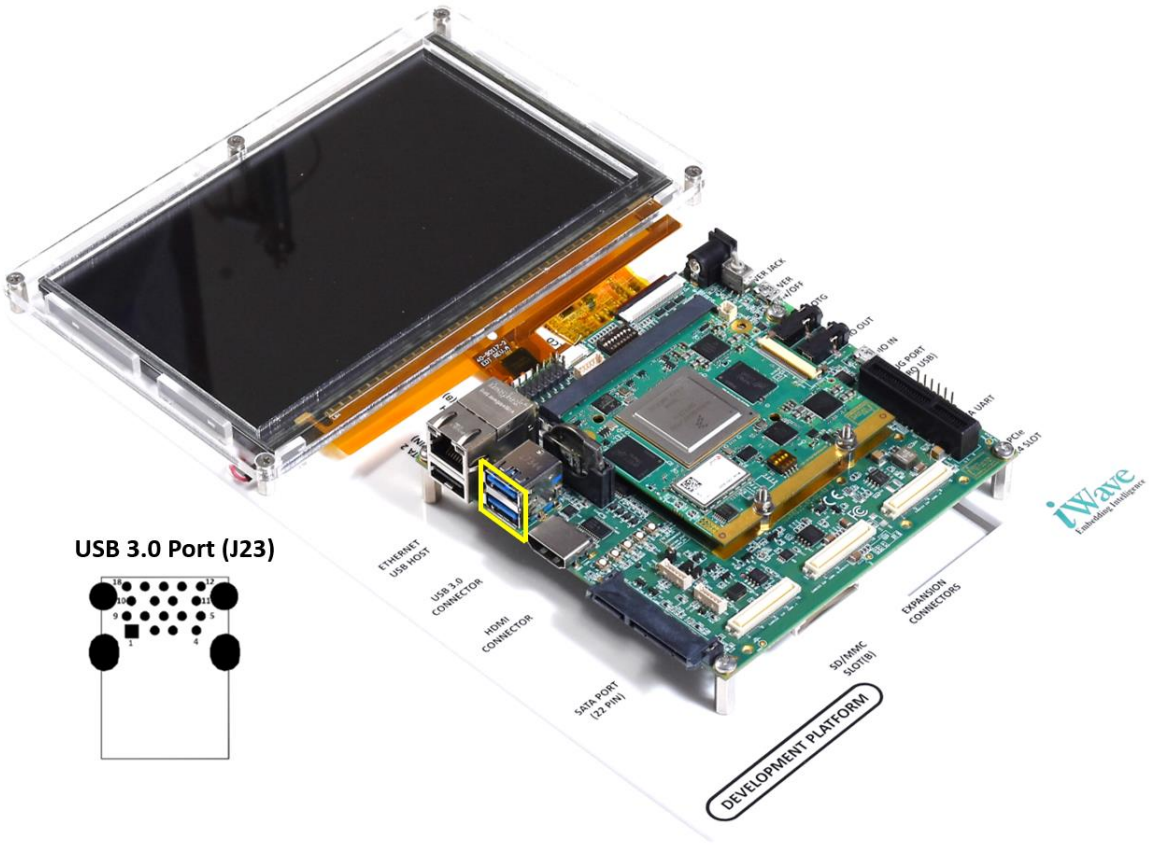

Figure 8: USB3.0 Host

2.6 Communication Interface Features

2.6.1 Gigabit Ethernet Interface

The i.MX8 QM/QP Qseven development board supports Ethernet Port interface through on SOM Ethernet PHY which supports 10/100/1000Mbps Ethernet. The Ethernet PHY output signals from Qseven MXM connector GBE0 is directly connected to RJ45 Magjack (J22). Also, it supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack. This RJ45 Magjack combo connector is physically located at the top of the board as shown below.

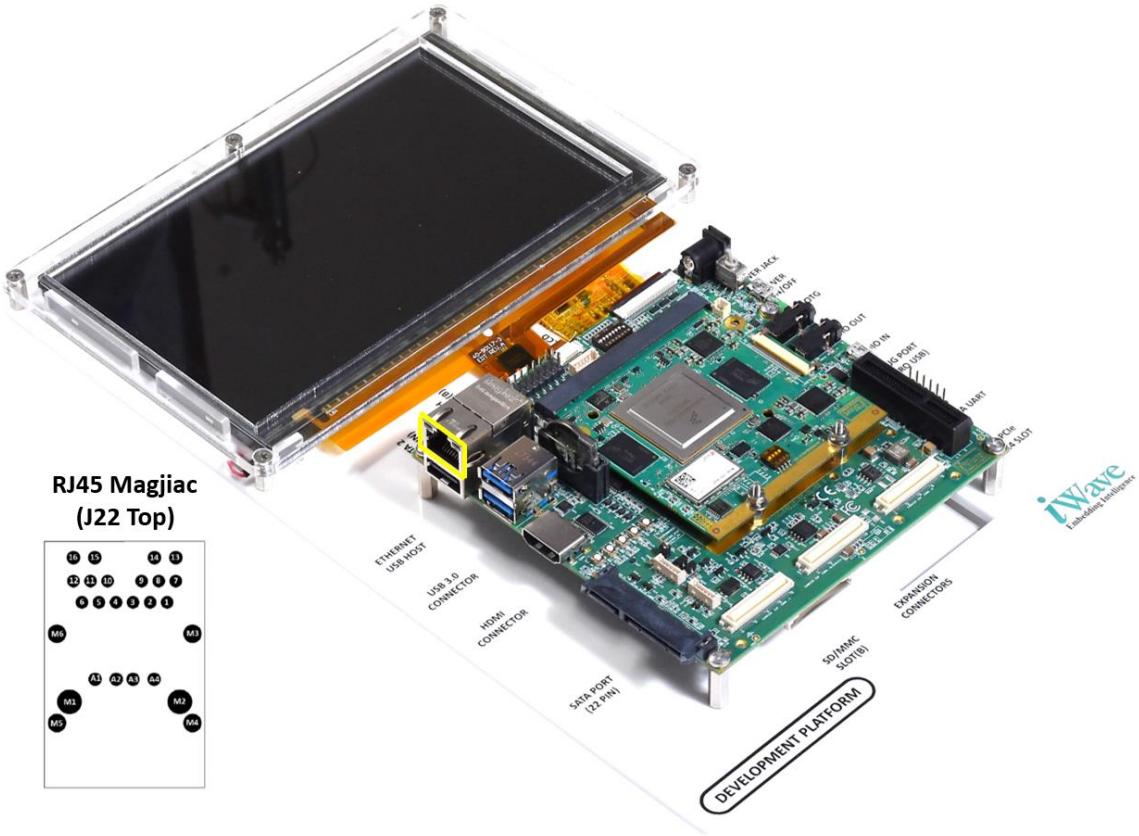

Figure 9: RJ45 Magjack

2.6.2 USB2.0 Host Interface

The i.MX8 QM/QP Qseven carrier board supports three USB2.0 Host interface through on SOM USB3.0 Hub via Qseven Port0, Port2 and Port3. These three host ports from the Qseven MXM connector are directly connected to USB2.0 TypeA combo connector (J22),bottom and top port of dual stack USB3.0 TypeA connector (J23) respectively.

The VBUS power of USB2.0 Port0 connector is connected through current limit power switches which limits the current above 500mA. If connected USB2.0 device takes more than 500mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1 (86th Pin).

The VBUS power of USB2.0 Port3 connector is connected through current limit power switches which limits the current above 1000mA. If connected USB2.0 device takes more than 1000mA current, this power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 2 & 3 (85th Pin).

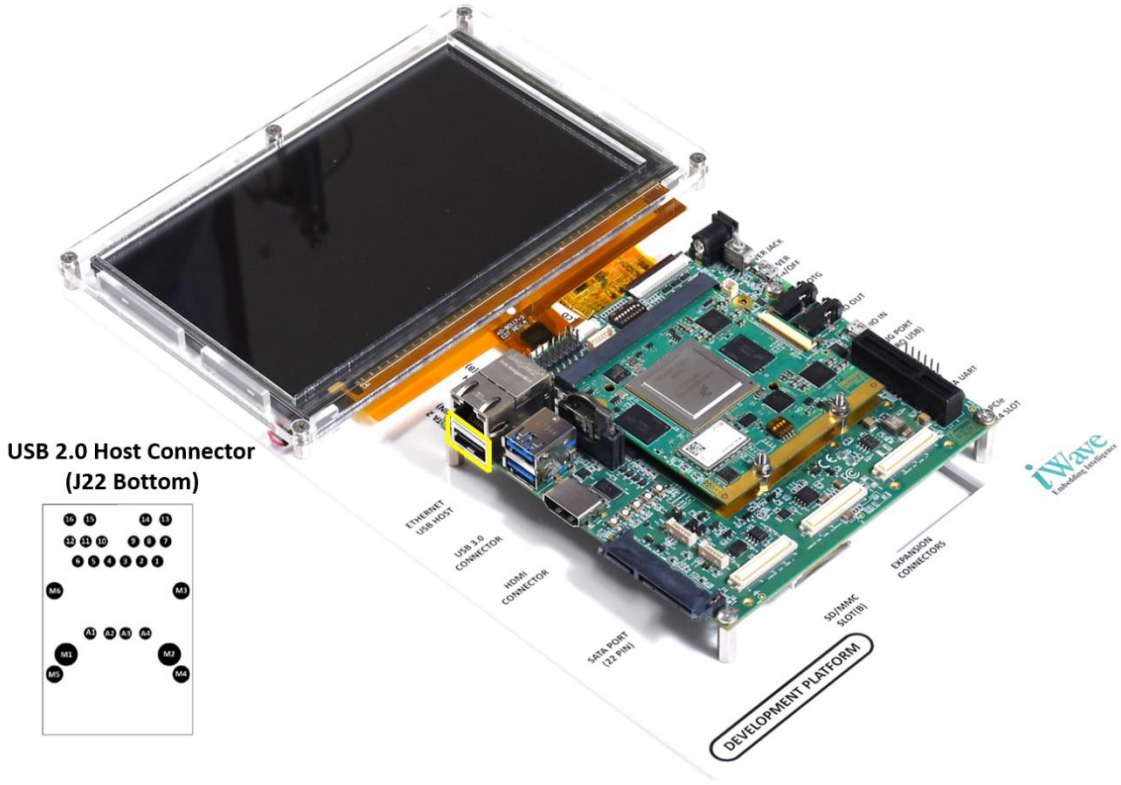

Figure 10: USB2.0 Host

2.6.3 USB2.0 OTG Interface

The i.MX 8 QM/QP Qseven carrier Board supports USB2.0 High Speed OTG interface through i.MX8 CPU's USB0 interface. This USB2.0 Port1 signals of Qseven MXM connector is directly connected to USB2.0 MicroAB connector (J2). This port can be used as USB OTG functionality which supports USB host and USB device based on USB ID pin status. This USB ID pin is also connected to DIP switch (SW2) 8th position and can be used to force this port as USB host alone by setting to ON position. When the DIP switch (SW2) 8th position is OFF position, either Host or device functionality can be set based on the USB ID pin status.

The VBUS power of this USB2.0 connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 500mA in host mode. The connected Qseven SOM detects the USB functionality through USB ID pin and controls the power using the USB_DRIVE_VBUS pin

(56th pin) of Qseven MXM connector. In Host mode, USB_DRIVE_VBUS should drive high to enable the power to the connector and in device mode, USB_DRIVE_VBUS should drive low to disable the power to the connector.

If connected USB2.0 device takes more than 500mA current, current limit power switch limits the current to constant mode and sends the over current indication signal to the over current indicator pin of Qseven MXM connector USB port 0 & 1. This USB2.0 OTG connector is physically located at the top of the board as shown below.

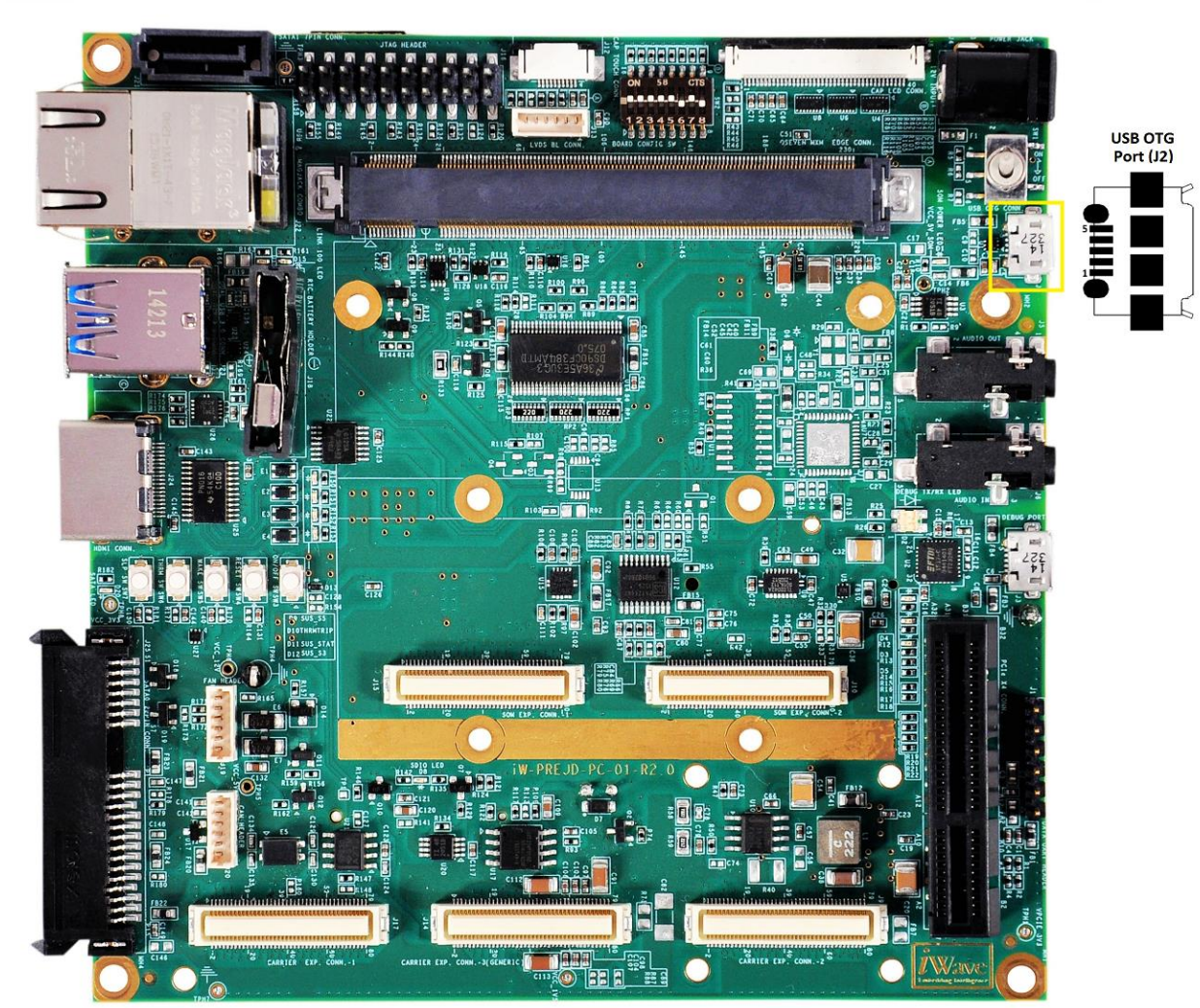

Figure 11: USB2.0 OTG

2.6.4 SDIO Interface

The i.MX 8 QM/QP Carrier Board supports SDIO interface through CPU's uSDHC1 interface. This uSDHC1 signals from Qseven MXM connector is connected to SD/MMC connector (J30) to support Standard SD interface. This connector supports up to 4-bit data transfer with card detect and write protect. Also it supports SDIO activity Green LED (D8) on board for SDIO bus transfer indication.

The main power to SD/MMC connector is 3.3V and it is connected through power switch to support power enable/disable feature. This power enable/disable is controlled from the SDIO_PWR# pin of Qseven MXM connector. This SD/MMC connector (J30) is physically located at the bottom of the board as shown below.

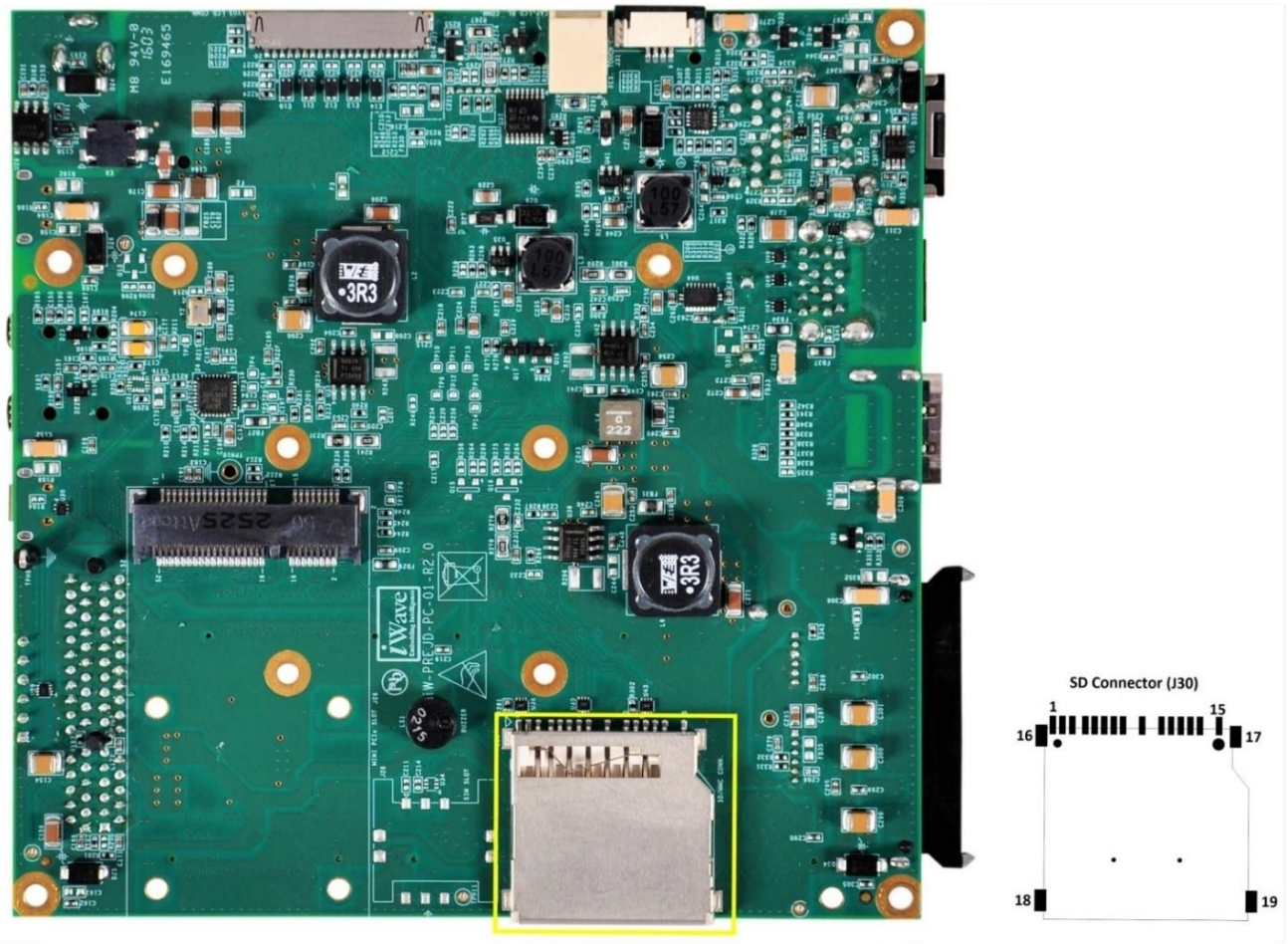

Figure 12:Standard SD Connector

2.6.5 CAN Interface

The i.MX 8 QM/QP Qseven Carrier Board supports CAN interface through i.MX 8 QM/QP CAN interface. This CAN1 interface signals from Qseven MXM connector (pins 129th & 130th) is connected to CAN Bus transceiver "SN65HVD230DR" and to 6pin custom CAN header (J20). Mode select pin (Rs) of the CAN Bus transceiver is connected to GPIO4 (189th Pin) of the Qseven MXM connector. This CAN header is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

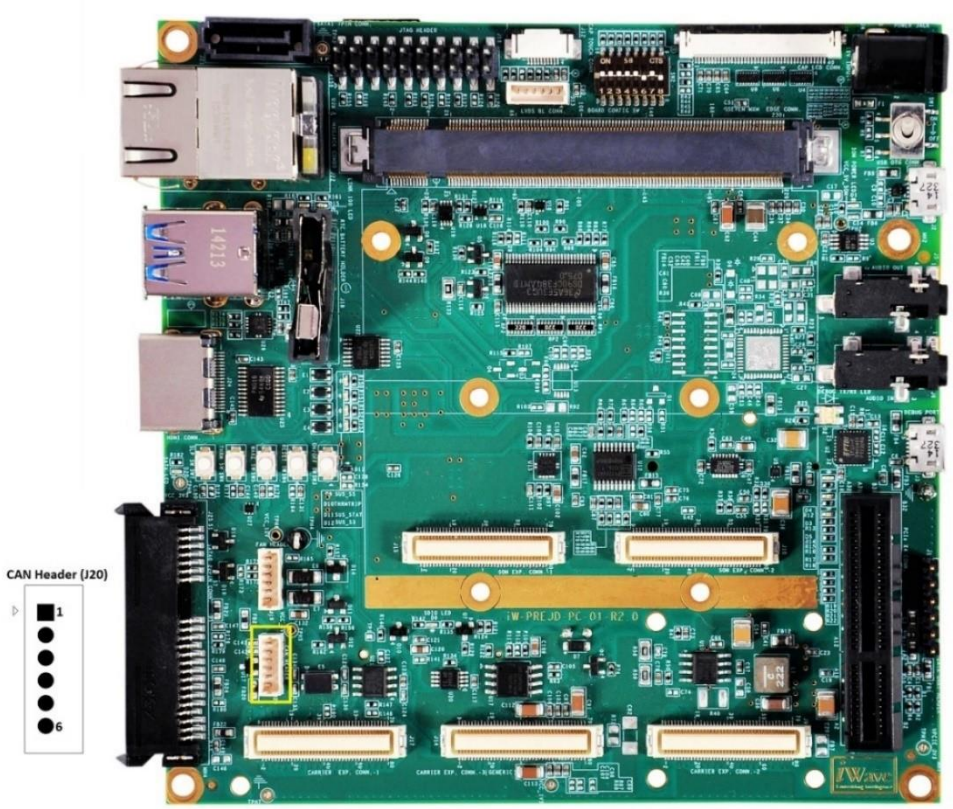

Figure 13: CAN Header

Table 8: CAN Header Pinout

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	VCC_5V	O, 5V Power	5V Supply Voltage.
2	VCC_12V	NC	NA	*Note: Optionally connected to 12V supply Volatge.*

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
3	CANL	CAN0_LOW	IO, DIFF	CAN0 Low-Level Voltage I/O
4	GND	GND	Power	Ground.
5	CANH	CAN0_HIGH	IO, DIFF	CAN0 High-Level Voltage I/O
6	GND	GND	Power	Ground.

2.7 Audio/Video Features

2.7.1 HDMI Interface

The i.MX 8 QM/QP CPU supports HDMI 2.0 audio/video out. HDMI Signals from the Qseven MXM connector along with HDMI DDC clock & data is connected to Standard HDMI Type-A connector with ESD protection circuitry. HDMI Output connector (J23) is physically located on top of the board as shown below.

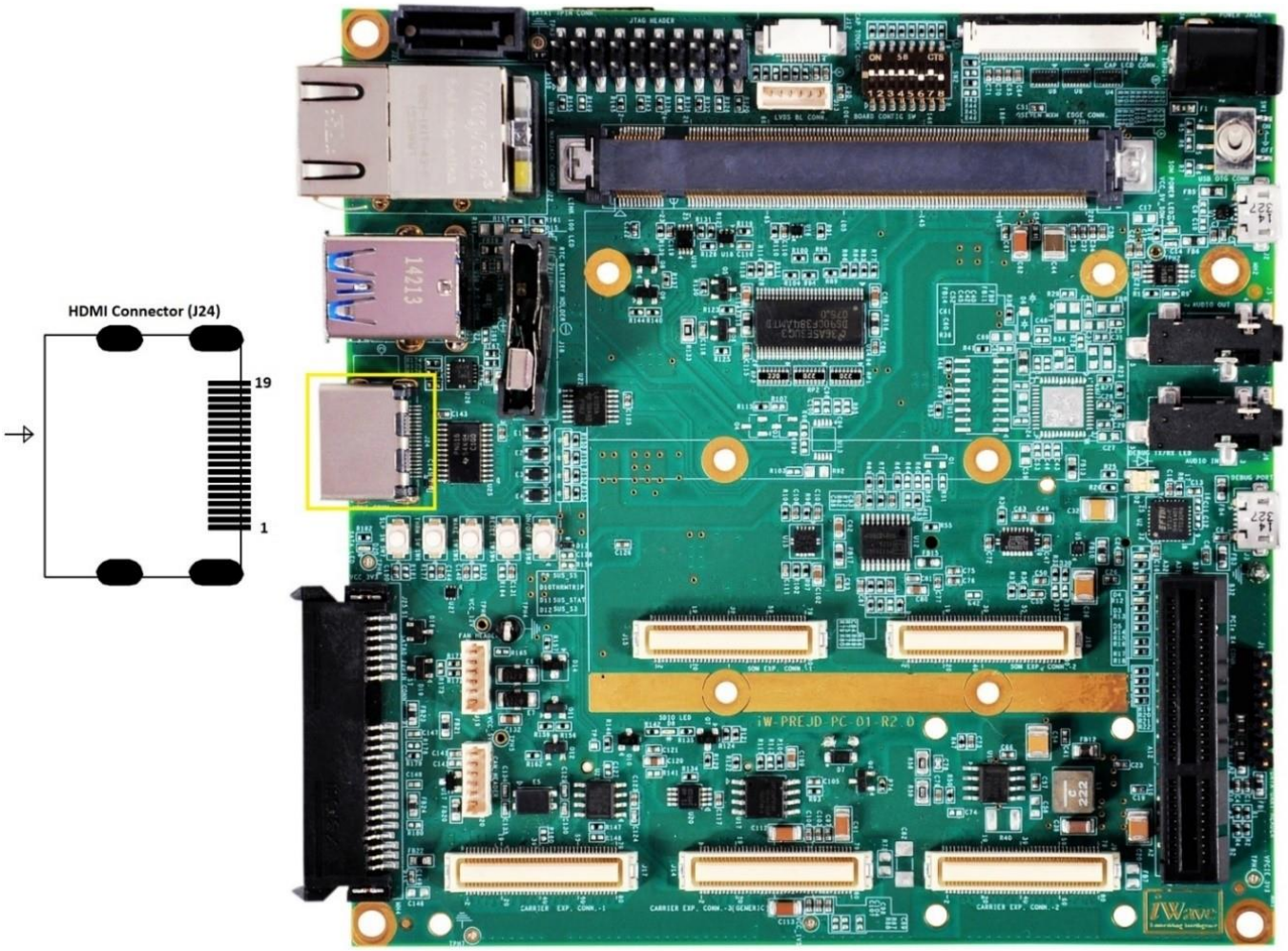

Figure 14: HDMI Output

2.7.2 I2S Audio Interface

The i.MX 8 QM/QP Qseven carrier board supports Audio In and Out through CPU's CPU's SAI1 interface which can support I2S format. This four wire I2S signals from Qseven MXM connector is connected to I2S Audio Codec "SGTL5000" to support Headphone Stereo output and Mono Mic input which is supported through 3.5mm Jack J5 and J6 correspondingly. Also, Headphone detect and Mic detect is supported through Qseven MXM connector pins GPIO3 (188th Pin) & GPIO2 (187th Pin) correspondingly. These Audio Jacks are physically located at the top of the board as shown below.

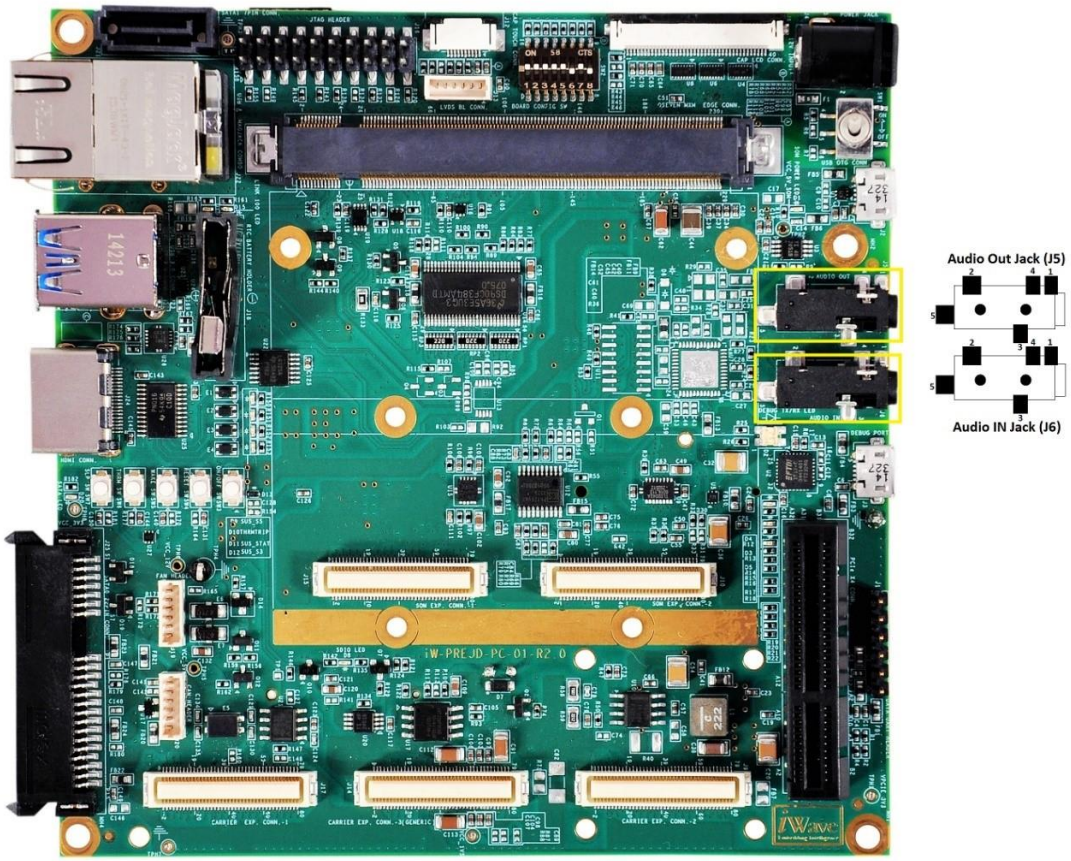

Figure 15: Audio Jack

2.7.3 7” LCD with Capacitive Touch

The i.MX 8 QM/QP Qseven carrier board supports 7inch, 18bpp RGB LCD “ETM070001ADH6” from Emerging Display Technologies Corporation (EDT) with capacitive touch panel. i.MX 8 CPU’s LVDS1_CH0 port is connected to primary LVDS channel of Qseven MXM connector. This primary LVDS interface signals are directly connected to LVDS transmitter (DS90CF384A) in carrier board which converts LVDS Interface signals to RGB and connects to RGB LCD connector (J8). This RGB LCD connector (J8) is physically located at the top of board as shown below.

This RGB LCD’s power enable and backlight enable is connected from LVDS_PPEN (111th pin) & LVDS_BLEN (112th pin) of Qseven MXM connector which is i.MX 8 CPU’s GPIO pins “GPIO01_14” and “GPIO01_09” respectively. Also, RGB LCD’s brightness is controlled from LVDS_BLT_CTRL (123rd pin) of Qseven MXM connector which is i.MX 8 CPU’s PWM(GP0_22).

Note: In i.MX 8 QM/QP carrier board, LVDS brightness control GPIO from Qseven MXM connector (123rd Pin) is shared to both primary & secondary LCD’s brightness control.

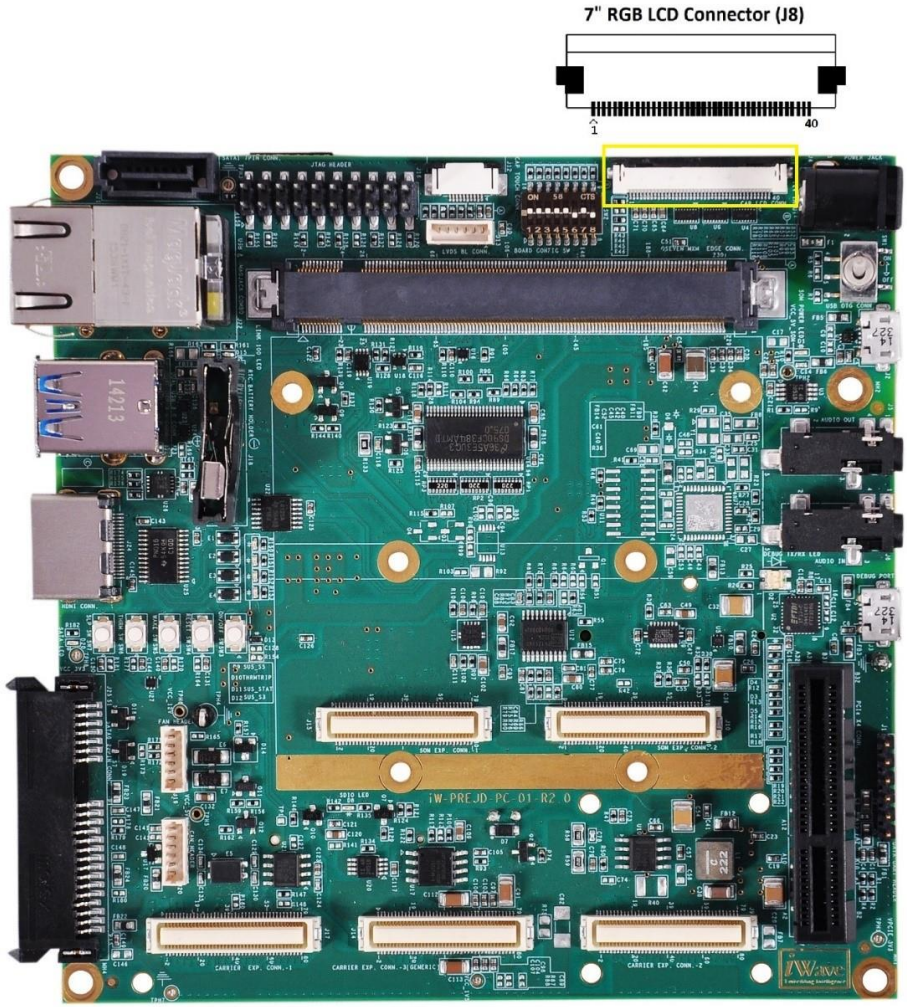

Figure 16: RGB LCD Connector

Table 9: 7” RGB LCD Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	U/D	U/D	O, 3.3V CMOS	Up or Down Scanning Direction.
2	L/R	L/R	O, 3.3V CMOS	Left or Right Scanning Direction.
3	NC	NC	-	-
4	VCC1	VCC1	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
5	VCC2	VCC2	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
6	VCC3	VCC3	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
7	VCC4	VCC4	O, 3.3V Power	3.3V Supply voltage for LED Driver Circuit.
8	NC	NC	-	-
9	DIS_DE	DIS_DE	O, 3.3V CMOS	Data Enable Output.
10	VSS1	GND	Power	Ground.
11	VSS2	GND	Power	Ground.
12	VSS3	GND	Power	Ground.
13	B5	DIS_B7	O, 3.3V CMOS	Display Blue Data 7(MSB).
14	B4	DIS_B6	O, 3.3V CMOS	Display Blue Data 6.
15	B3	DIS_B5	O, 3.3V CMOS	Display Blue Data 5.
16	VSS4	GND	Power	Ground.
17	B2	DIS_B4	O, 3.3V CMOS	Display Blue Data 4.
18	B1	DIS_B3	O, 3.3V CMOS	Display Blue Data 3.
19	B0	DIS_B2	O, 3.3V CMOS	Display Blue Data 2(LSB).
20	VSS5	GND	Power	Ground.
21	G5	DIS_G7	O, 3.3V CMOS	Display Green Data 7(MSB).
22	G4	DIS_G6	O, 3.3V CMOS	Display Green Data 6.
23	G3	DIS_G5	O, 3.3V CMOS	Display Green Data 5.
24	VSS6	GND	Power	Ground.
25	G2	DIS_G4	O, 3.3V CMOS	Display Green Data 4.
26	G1	DIS_G3	O, 3.3V CMOS	Display Green Data 3.
27	G0	DIS_G2	O, 3.3V CMOS	Display Green Data 2(LSB).
28	VSS7	GND	Power	Ground.
29	R5	DIS_R7	O, 3.3V CMOS	Display Red Data 7(MSB).
30	R4	DIS_R6	O, 3.3V CMOS	Display Red Data 6.
31	R3	DIS_R5	O, 3.3V CMOS	Display Red Data 5.
32	VSS8	GND	Power	Ground.
33	R2	DIS_R4	O, 3.3V CMOS	Display Red Data 4.
34	R1	DIS_R3	O, 3.3V CMOS	Display Red Data 3.
35	R0	DIS_R2	O, 3.3V CMOS	Display Red Data 2(LSB).
36	VSS9	GND	Power	Ground.
37	NC	NC	-	-
38	CLK	DIS_CLK	O, 3.3V CMOS	DOT Data Clock.
39	HSYNC	DIS_HSYNC	O, 3.3V CMOS	Horizontal SYNC Output.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
40	VSYNC	DIS_VSYNC	O, 3.3V CMOS	Vertical SYNC Output.

2.7.4 LVDS Port with Resistive Touch

The i.MX 8 QM/QP Qseven carrier board can support LVDS LCD interface through i.MX 8 QM/QP CPU's LVDS1_CH1 display port. These LVDS signals from Qseven MXM connector is directly connected to 20pin LVDS connector (J27). And LVSD LCD's power enable and backlight enable is connected from GPIO6 (191st pin) & GPIO5 (190th pin) of Qseven MXM connector which is i.MX 8 QM/QP CPU's GPIO pins "GPIO05_00" and "GPIO01_11" respectively. This LVDS LCD connector (J27) is physically located at the bottom of board as shown below.

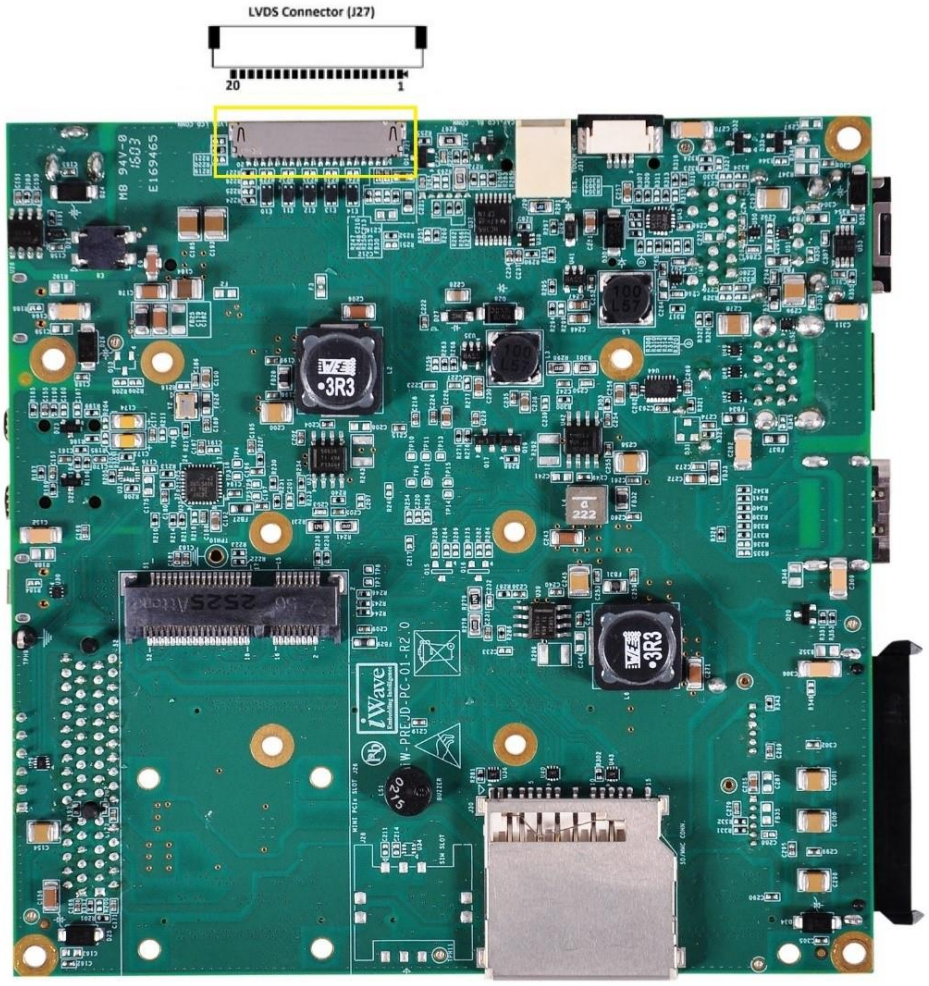

Figure 17: LVDS Display Connector

Table 10: LVDS Connector Pinout

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VDD1	VCC_3V3_TFT0	Power	3.3V Supply voltage

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
2	VDD2	VCC_3V3_TFT0	Power	3.3V Supply voltage
3	GND1	GND	Power	Ground
4	GND2	GND	Power	Ground
5	RIN0-	LVDS1_CH1_TX0_N	I, LVDS	LVDS channel differential pair0 negative
6	RIN0+	LVDS1_CH1_TX0_P	I, LVDS	LVDS channel differential pair0 positive
7	GND3	GND	Power	Ground
8	RIN1-	LVDS1_CH1_TX1_N	I, LVDS	LVDS channel differential pair1 negative
9	RIN1+	LVDS1_CH1_TX1_P	I, LVDS	LVDS channel differential pair1 positive
10	GND4	GND	Power	Ground
11	RIN2-	LVDS1_CH1_TX2_N	I, LVDS	LVDS channel differential pair2 negative
12	RIN2+	LVDS1_CH1_TX2_P	I, LVDS	LVDS channel differential pair2 positive
13	GND5	GND	Power	Ground
14	CLKIN-	LVDS1_CH1_CLK_N	I, LVDS	LVDS channel differential Clock negative
15	CLKIN+	LVDS1_CH1_CLK_P	I, LVDS	LVDS channel differential Clock positive
16	GND6	GND	Power	Ground
17	RIN3-	LVDS1_CH1_TX3_N	I, LVDS	LVDS channel differential pair3 negative
18	RIN3+	LVDS1_CH1_TX3_P	I, LVDS	LVDS channel differential pair3 positive
19	GND7	GND	Power	Ground
20	GND8	GND	Power	Ground

2.8 Additional Features

2.8.1 SPI Flash

The i.MX 8 QM/QP Qseven development board supports SPI Flash(U62) through i.MX8 CPU's SPI3 interface. This SPI interface signals from MXM connector is connected to SPI Flash "SST25VF016B-50" and operating at 3.3V Level.

2.8.2 RTC Coin Cell Holder

The i.MX 8M/QP Qseven carrier board supports Coin Cell Holder to connect "2032" series coin cell. This coin cell voltage is connected to Qseven MXM connector VDD_RTC pin (193th) for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J18) is physically located at the top of the board as shown below.

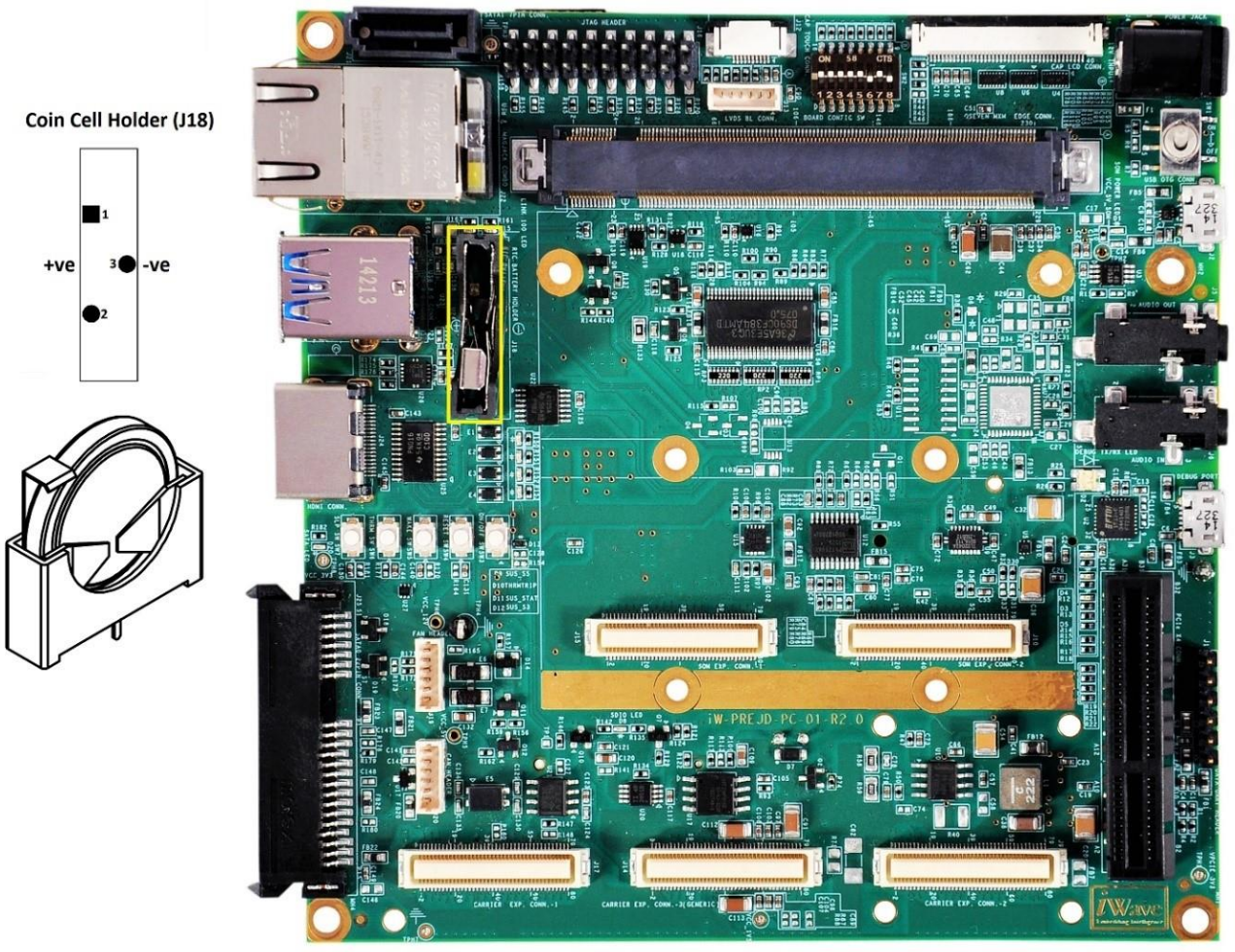

Figure 18: RTC Battery Holder

2.8.3 Fan Header

The i.MX 8M/QP Qseven carrier board supports 6pin Fan Header (J19) to connect the Fan if required. The "FAN_PWMOUT" signal of Qseven MXM connector is connected to Fan header to control the speed of the Fan. The i.MX 8M/QP CPU's PWM3 interface is used for Fan speed control PWM. This Fan Header (J19) is physically located at the top of the board as shown below.

Number of Pins : 6

Connector Part number : 53047-0610 from Molex

Mating Connector : 0510210600 from Molex with crimping pins

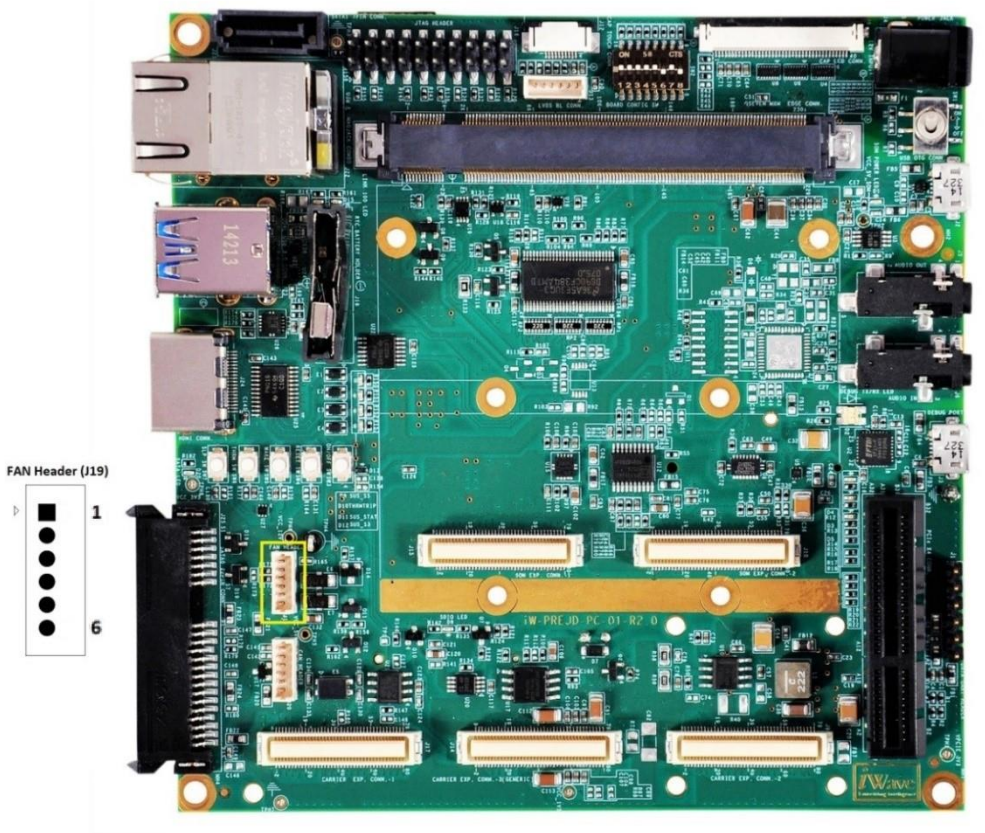

Figure 19: Fan Header

Table 11: Fan Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC	VCC_12V	O, 12V Power	12V Supply Voltage.
2	PWM	PWM3(GPIO0_16)	O, 3.3 CMOS	Fan Speed control.
3	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
4	NC	NC	-	-
5	FAN_PWR	VCC_FAN	O, Power	Fan Power Control.
6	GND	GND	Power	Ground.

2.8.4 JTAG Header (Optional)

A Standard 20-pin ARM JTAG Header is available in i.MX 8M/QP Qseven carrier board for debug purpose. JTAG signals from Qseven MXM connector is connected to JTAG Header (J16) through 3.3V level Buffer. This JTAG Header (J16) is physically located at the top of the board as shown below.

As per Qseven specification version 2.0, Debug UART and JTAG interfaces share the same pins in Qseven Edge connector. Hence either debug UART or JTAG interface can be used at a time. By default, Debug UART (UART4) is supported in the i.MX 8M/QP Qseven SOM and hence JTAG connector on i.MX 8M/QP Qseven carrier board cannot be used for debugging.

Number of Pins : 20

Connector Part number : 0015912200 from Molex

Mating Connector : 0015445820 from Molex

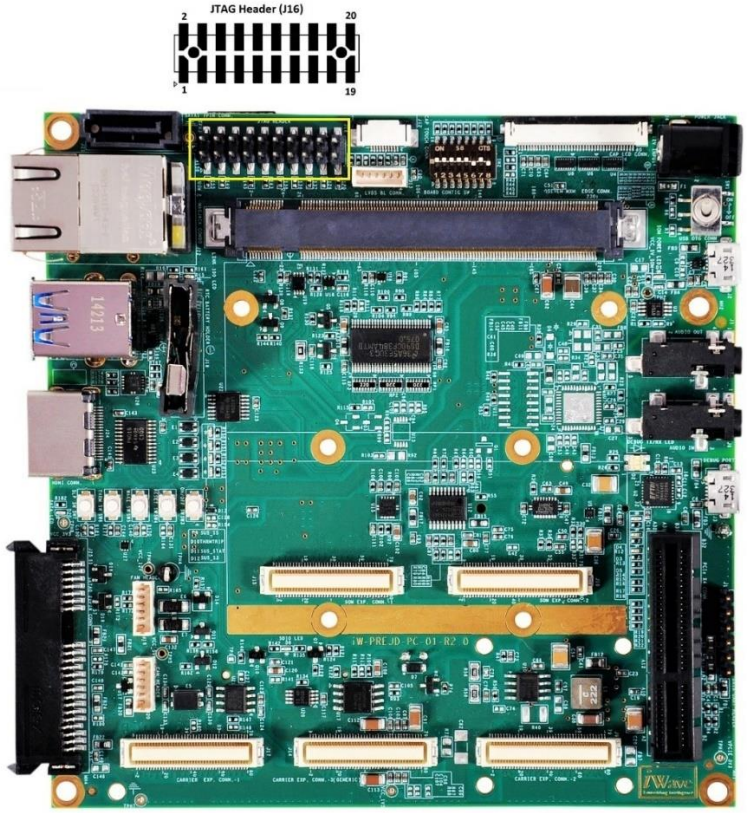

Figure 20: JTAG Header

2.9 On Board Switches

2.9.1 Power ON/OFF Switch

The i.MX 8M/QP Qseven carrier board has power ON/OFF switch (SW1) to control the Main Power Input On/Off functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

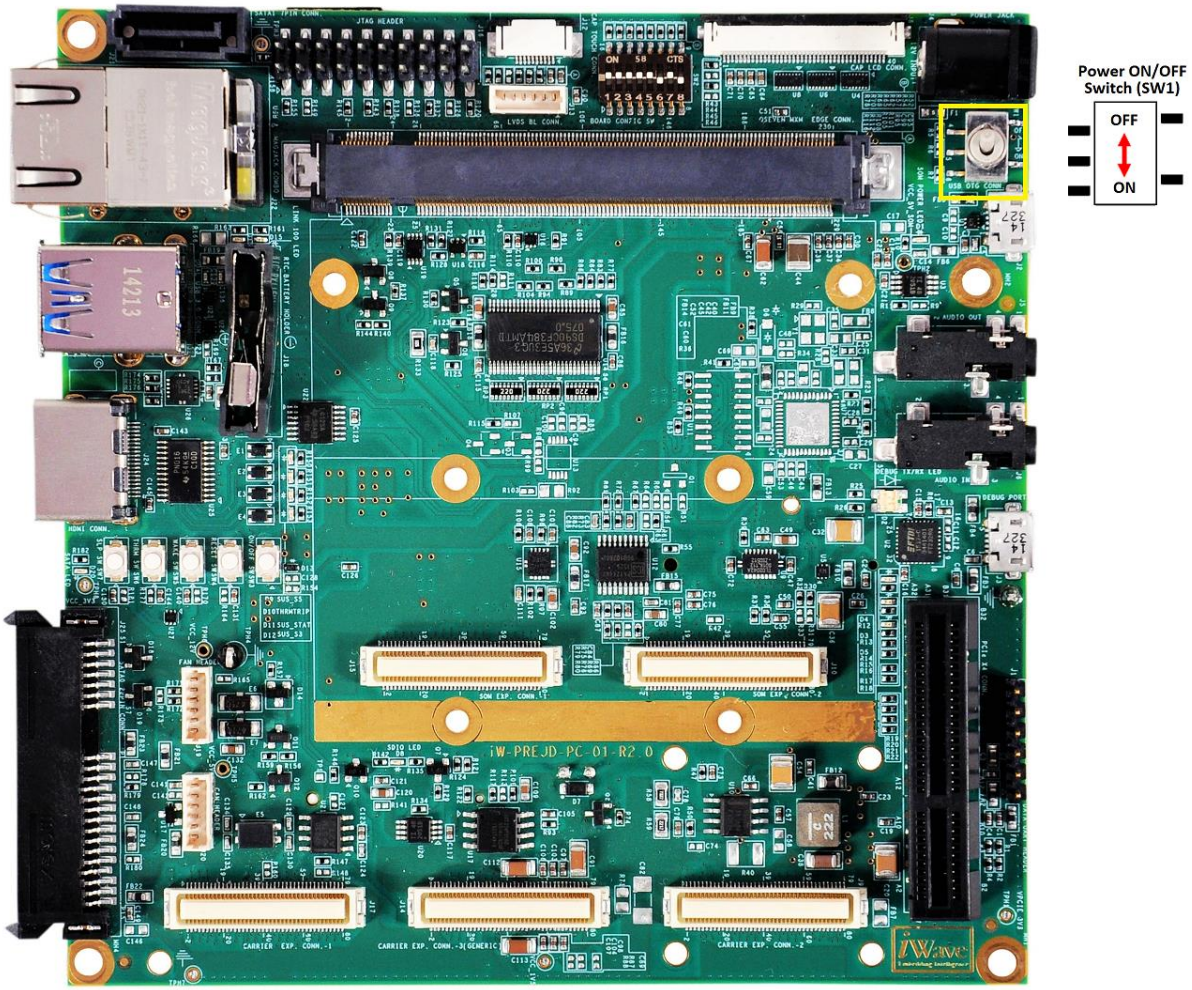

Figure 21: Power ON/OFF Switch

2.9.2 Reset Switch

The i.MX 8M/QP Qseven carrier board supports Push button switch (SW4) to reset the i.MX 8M/QP CPU. “RSTBTN” signal of Qseven MXM connector is directly connected from Reset Push button switch. This Reset Push button switch (SW4) is physically located at the top of the board as shown below.

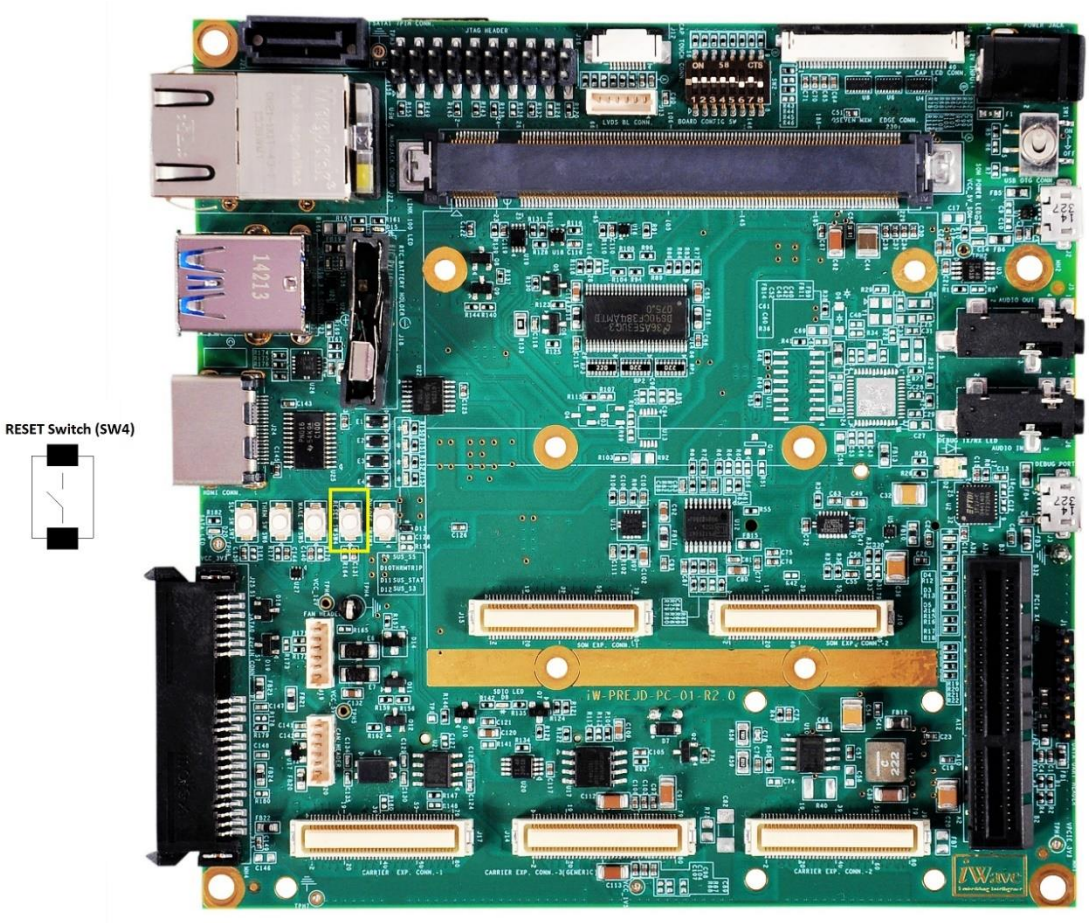

Figure 22: Reset Switch

2.9.3 Board Configuration Switch

The i.MX 8M/QP Qseven carrier board has one 8bit Board configuration switch (SW2) to configure board specific feature setting. Each bit of this switch is used to select the different features or modes. This Board configuration switch is physically located at the top of the board as shown below.

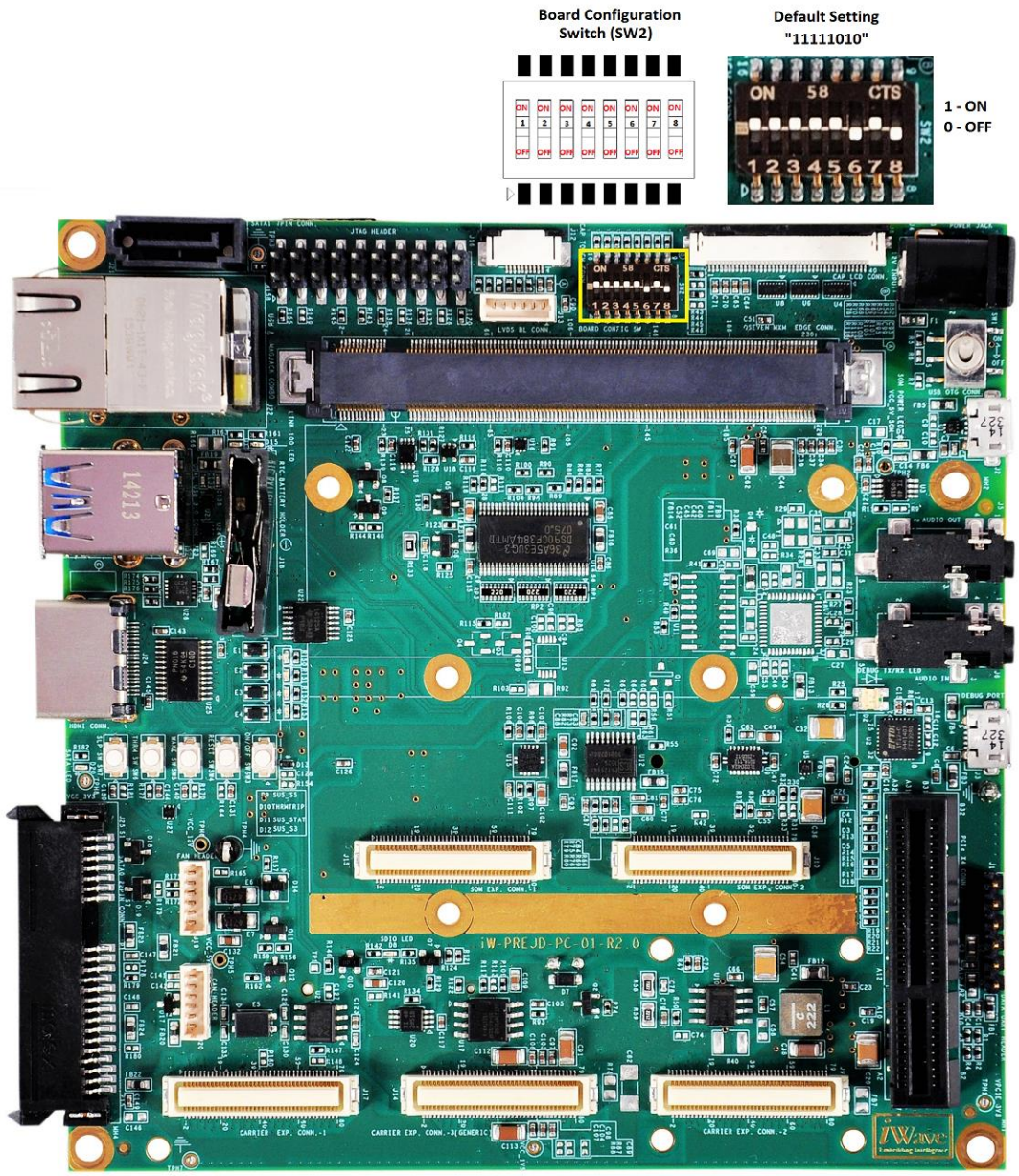

Figure 23: Board Configuration Switch

The functionality of Board configuration switch (SW2) in i.MX 8M/QP Qseven carrier board is explained in the following table. All the bits of Board configuration switch are not used in i.MX 8M/QP Qseven carrier board and so only the required bits are explained with default setting highlighted.

Table 12: Board Configuration Switch

SW2 Bits	SW2 Bit Name	Description	
		OFF	ON
1	BIOS_DSIABLE#	-	-
2	BATLOW#	-	-
3	LID_BTN#	-	-
4	USB_SELECT	-	-
5	CODEC_SELECT	-	-
6	PCIe_SELECT	PCIe channel0 is connected to Mini-PCIe Slot.	PCIe channel0 is connected to PCIex4 Slot.
7	DEBUG_SELECT	-	Debug Port is selected as UART.
8	USB_ID	USB0 acts as Host mode or Device mode based on the connected cable in USB MicroAB connector (J2).	USB0 is forced to Host Mode.

2.1 SOM Expansion Connectors

The i.MX 8M/QP Qseven carrier board has two 80pin Expansion Connectors for mating with i.MX 8M/QP Qseven SOM. This SOM Expansion connector 1 & 2 (J15 & J10) pins are one to one directly connected to Carrier board Expansion connector 1 & 2 (J17 & J9) pins in i.MX 8M/QP Qseven carrier board.

These Expansion connectors J15 & J10 are physically located at the top of the board as shown below.

Connectors Part number : DF17(2.0)-80DP-0.5V(57) from Hirose
Mating Connector : DF17(3.0)-80DS-0.5V(57) from Hirose

Note: For SOM expansion connector pinout, refer the i.MX 8 QM/QP Qseven SOM Hardware User Guide.

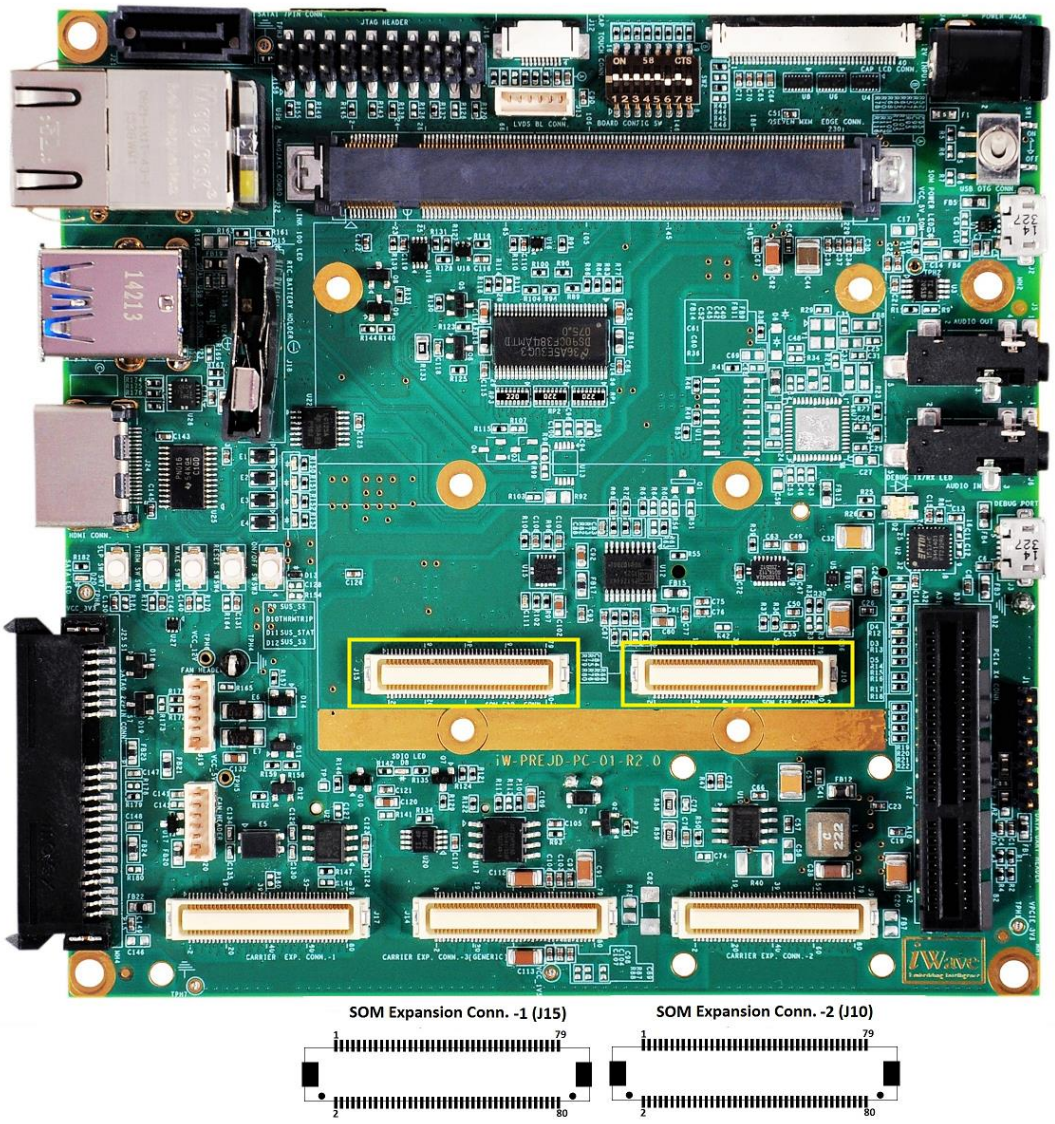

Figure 24: SOM Expansion Connectors

2.2 Carrier Board Expansion Connectors

The i.MX 8M/QP Qseven carrier board has three 80pin Expansion Connectors for expansion purpose. In these three connectors, Carrier Board Expansion connector 1 & 2 (J17 & J9) pins are one to one directly connected from SOM Expansion connector 1 & 2 (J15 & J10) pins in i.MX 8M/QP Qseven carrier board.

The i.MX 8M/QP CPU's SPI (with CS1), I2C0, I2C2 interfaces and unused GPIOs from Qseven MXM connector are directly connected to Expansion Connector3 (J14). Also, on-board 5V, 3.3V & 1.5V power pins are connected to this connector for Add-On Module power.

These Expansion connectors J17, J9 & J14 are physically located at the top of the board as shown below.

Connectors Part number: DF17(3.0)-80DS-0.5V(57) from Hirose

Mating Connector : DF17(2.0)-80DP-0.5V(57) from Hirose

Important Note: Since carrier board Expansion connector 1 & 2 pins are one to one directly connected from i.MX 8 QM/QP Qseven SOM Expansion connector 1 & 2 pins, these connectors pinout information are not included in this document. Refer i.MX 8 QM/QP Qseven SOM hardware user guide for Expansion connector 1 & 2 pinout details.

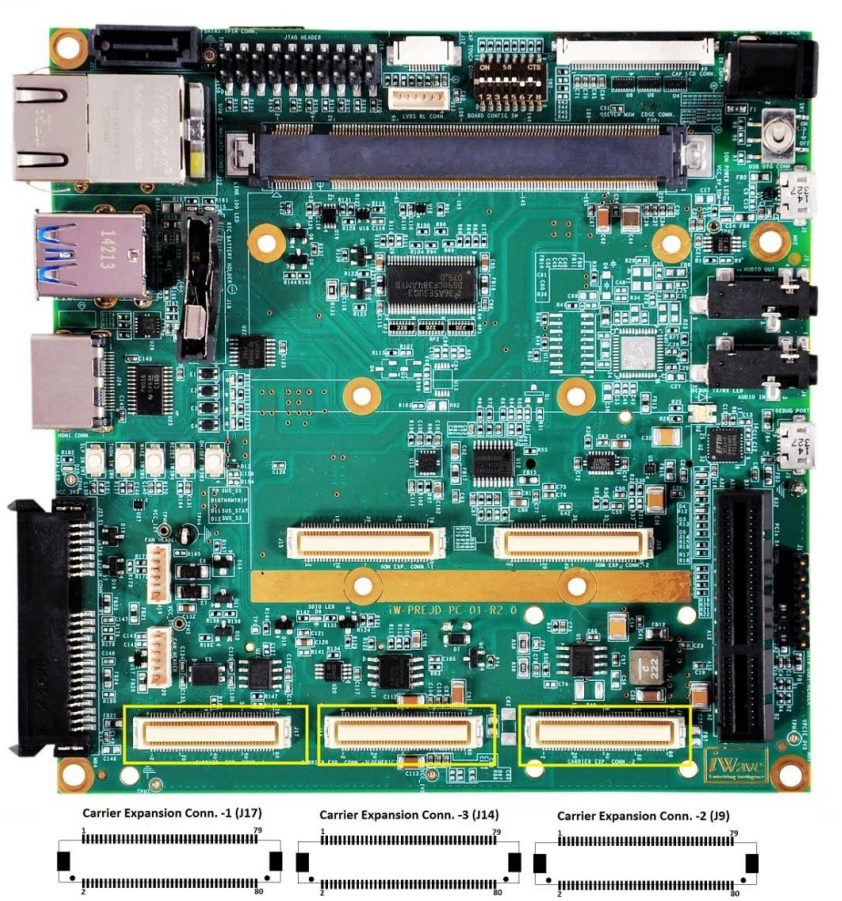

Figure 25: Carrier Board Expansion Connectors

Table 13: Expansion Connector3 Pin Out

Pin No	Signal Name	Signal Type / Termination	Description
1	GND	Power	Ground.
2	GND	Power	Ground.
3	GND	Power	Ground.
4	GND	Power	Ground.
5	GND	Power	Ground.
6	GND	Power	Ground.
7	SUS_S3_Q7	I, 3.3V CMOS	*Note: 10K PU Provided in i.MX 8M/QP Qseven carrier board.* *Note: This pin is connected from Qseven MXM connector 18th pin.*
8	SUS_S5_Q7	I, 3.3V CMOS	*Note: 10K PU Provided in i.MX 8M/QP Qseven carrier board.* *Note: This pin is connected from Qseven MXM connector 16th pin.*
9	Q7_GPIO_7(GPIO0_00)	IO, 3.3V CMOS	Qseven General purpose Input/Output7. *Note: This pin is connected to GPIO0_00 of i.MX 8M/QP CPU through Qseven MXM connector 192nd pin.*
10	SUS_STAT_Q7(GPIO2_05)	O, 3.3V CMOS	Suspend Status *Note: This pin is connected to GPIO02_02 of i.MX 8M/QP CPU through Qseven MXM connector 19nd pin.*
11	SMBUS_ALERT(GPIO1_15)	O, 3.3V CMOS	System Management Bus Alert output *Note: This pin is connected to GPIO01_15 of i.MX 8M/QP CPU through Qseven MXM connector 64nd pin.*
12	RSTBN	O, 3.3V CMOS	Active low Reset button Output. *Note: This pin is connected to Qseven MXM connector 28th pin.*
13	GND	Power	Ground.
14	GND	Power	Ground.
15	WDOUT	I, 3.3V CMOS	Watchdog event indicator. *Note: This pin is connected to Qseven MXM connector 72nd pin.*
16	WAKE#(GPIO3_04)	O, 3.3V CMOS	External system wake event. *Note: This pin is connected to GPIO03_04 of i.MX 8M/QP CPU through Qseven MXM connector 17nd pin.*
17	WDTRIG#	O, 3.3V CMOS	Watchdog trigger signal. *Note: This pin is connected to Qseven MXM connector 70th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
18	GND	Power	Ground.
19	DMA_I2C2_SDA	NA	NC. *Note: This pin is optionally connected to DMA_I2C2_SDA line of i.MX 8M/QP CPU through Qseven MXM connector 126th pin.*
20	GPIO_THRMTRIP_Q7(GPIO3_05)	I, 3.3V CMOS	Thermal Alarm. *Note: This pin is connected to GPIO03_05 of i.MX 8M/QP CPU through Qseven MXM connector 69th pin.*
21	DMA_I2C2_SCL	NA	NC. *This pin is optionally connected to DMA_I2C2_SCL line of i.MX 8M/QP CPU through Qseven MXM connector 128th pin.*
22	GPII_1(GPIO0_04)	I, 3.3V CMOS	Sleep button signal. *Note: This pin is connected to GPIO00_04 of i.MX 8M/QP CPU through Qseven MXM connector 21st pin.*
23	USB3_HUB2_TXM	I, USB SS	USB3.0 Host Port1 Transmit Differential pair negative. *Note: This pin is connected to Qseven MXM connector 132nd pin.*
24	PWRBTN#	O, 3.3V CMOS	Power Button. *Note: This pin is connected to Qseven MXM connector 20th pin.*
25	USB3_HUB2_TXP	I, USB SS	USB3.0 Host Port1 Transmit Differential pair positive. *Note: This pin is connected to Qseven MXM connector 134th pin.*
26	GND	Power	Ground.
27	GND	Power	Ground.
28	GPII_0(GPIO3_03)	O, 3.3V CMOS	LID button. *Note: This pin is connected to GPIO03_03 of i.MX 8M/QP CPU through Qseven MXM connector 22nd pin.*
29	USB3_HUB2_RXM	O, USB SS	USB3.0 Host Port1 Receive Differential pair negative. *Note: This pin is connected to Qseven MXM connector 144th pin.*
30	GPII_2(GPIO0_05)	O, 3.3V CMOS	Battery low output. *Note: This pin is connected to Qseven MXM connector 27th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
31	USB3_HUB2_TXP	O, USB SS	USB3.0 Host Port1 Receive Differential pair positive. *Note: This pin is connected to Qseven MXM connector 146th pin.*
32	BIOS_DISABLE#	NA	NC. *Note: This pin is connected to Qseven MXM connector 41st pin.*
33	GND	Power	Ground.
34	Q7_GPIO_1(GPIO3_02)	IO, 3.3V CMOS/ 10K PU	Qseven General Purpose Input/Output1. *Note: This pin is connected to i.MX 8 QM/QP CPU's GPIO line GPIO02_02 through Qseven MXM connector 186th pin through default populated resistor.* *Note: Also, this pin is connected to Mini PCIe connector (J26) 20th pin through default populated resistor.*
35	LVDS1_I2C0_SDA	IO, 3.3V OD	LVDS I2C_SDA. *Note: This pin is connected to LVDS1_I2C0_SDA line of i.MX 8 QM/QP CPU through Qseven MXM connector 125th pin.*
36	Q7_GPIO_0(GPIO3_12)	I,3.3V CMOS/ 10K PU	Qseven General Purpose Input/Output0. This pin is connected to Capacitive Touch Connector and Resistive Touch Controller for touch interrupt. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO pin GPIO03_12 through Qseven MXM connector 185th pin through default populated resistor.*
37	LVDS1_I2C0_SCL	I, 3.3V OD	LVDS I2C_SCL. *Note: This pin is connected to LVDS1_I2C0_SCL line of i.MX 8 QM/QP CPU through Qseven MXM connector 127th pin.*
38	GND	Power	Ground.
39	DP_HPD(GPIO0_02)	O, 3.3V CMOS	Display port hot plug. *Note: This pin is optionally connected to i.MX 8 QM/QP CPU GPIO line GPIO0_02 through Qseven MXM connector 154th pin.*

Pin No	Signal Name	Signal Type / Termination	Description
40	Q7_GPIO_6(GPIO5_00)	IO, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output6. This pin is used to enable the LVDS display Power. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO line GPIO05_00 through Qseven MXM connector 191st pin through resistor and default populated.*
41	Q7_GPIO_3(GPIO3_11)	I, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output3 This pin is connected from Audio Out Jack for Headphone detect. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO line GPIO03_11 through Qseven MXM connector 188th pin through resistor and default populated.*
42	GPIO_RESET(GPIO1_05)	O, 3.3V CMOS	Touch Panel Reset. This pin is connected to Capacitive touch panel connector for reset. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO line GPIO01_05 through Qseven MXM connector 61st pin through default populated resistor.*
43	GND	Power	Ground.
44	Q7_GPIO_5(GPIO1_11)	IO, 3.3V CMOS	Qseven General purpose Input/Output5. This pin is connected to control the LVDS Backlight Power. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO line GPIO01_11 through Qseven MXM connector 190th pin through default populated resistor.*
45	Q7_GPIO_2(GPIO3_14)	I, 3.3V CMOS/ 10K PU	Qseven General purpose Input/Output2. This pin is connected from Audio IN Jack for Headphone Mic detect. *Note: This pin is also connected to i.MX 8 QM/QP CPU GPIO line GPIO03_14 through Qseven MXM connector 187th pin through default populated resistor.*
46	SPI3_MOSI [1]	I, 3.3V CMOS	SPI Master In Slave Out. This Pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8 QM/QP CPU SPI3_SDI line through Qseven MXM connector 201st pin.*

Pin No	Signal Name	Signal Type / Termination	Description
47	Q7_GPIO_4(GPIO1_08)	IO, 3.3V CMOS	Qseven General purpose Input/Output4. This pin is connected to CAN0 Transceiver Power down control. *Note: This pin is connected to i.MX 8 QM/QP CPU GPIO line GPIO1_08 through Qseven MXM Connector 189th pin.*
48	SPI3_MOSI [1]	O, 3.3V CMOS	SPI Master Out Slave In. This pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8 QM/QP CPU SPI3_SDO line through Qseven MXM connector 199th pin.*
49	SPI3_CS1 [1]	I, 3.3V CMOS	SPI Chip Select1. *Note: This pin is connected to i.MX 8 QM/QP CPU SPI3_CS1 line through Qseven MXM connector 202nd pin.*
50	GND	Power	Ground.
51	SPI3_SCLK	I, 3.3V CMOS	SPI Clock. This Pin is used for On Board SPI Flash. *Note: This pin is connected to i.MX 8 QM/QP CPU SPI3_SCLK line through Qseven MXM connector 203rd pin.*
52	EDP_AUX_P	I, EDP	EDP AUX+. *Note: This pin is connected to Qseven MXM connector 138th pin.*
53	GPIO_THRMTRIP_Q7(GPIO3_05)	I, 3.3V CMOS	Connected to LED (D11) through buffer in carrier board for thermal trip indication. *Note: This pin is connected i.MX 8 QM/QP GPIO line GPIO3_05 through Qseven MXM connector 71st pin.*
54	EDP_AUX_N	I, EDP	EDP AUX-. *Note: This pin is connected to Qseven MXM connector 140th pin.*
55	GND	Power	Ground.
56	GND	Power	Ground.
57	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
58	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
59	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
60	VCC_1V5	O, 1.5V Power	1.5V Supply Voltage.
61	GND	Power	Ground.
62	GND	Power	Ground.
63	VCC_5V	O, 5V Power	5V Supply Voltage.
64	VCC_5V	O, 5V Power	5V Supply Voltage.

Pin No	Signal Name	Signal Type / Termination	Description
65	VCC_5V	O, 5V Power	5V Supply Voltage.
66	VCC_5V	O, 5V Power	5V Supply Voltage.
67	VCC_5V	O, 5V Power	5V Supply Voltage.
68	VCC_5V	O, 5V Power	5V Supply Voltage.
69	VCC_5V	O, 5V Power	5V Supply Voltage.
70	VCC_5V	O, 5V Power	5V Supply Voltage.
71	GND	Power	Ground.
72	GND	Power	Ground.
73	GND	Power	Ground.
74	GND	Power	Ground.
75	GND	Power	Ground.
76	GND	Power	Ground.
77	DMA_I2C1_SCL	O, 3.3V OD	DMA_I2C1 clock. *Note: This pin is connected to i.MX 8 QM/QP CPU DMA_I2C1_SCL line through Qseven MXM Connector 60th pin through default populated resistor.*
78	DMA_I2C2_SCL	O, 3.3V OD	DMA_I2C2 clock. *Note: This pin is connected to i.MX 8 QM/QP CPU DMA_I2C2_SCL line through Qseven MXM Connector 66th pin through default populated resistor.*
79	DMA_I2C1_SDA	IO, 3.3V OD	DMA_I2C1 Data. *Note: This pin is connected to i.MX 8 QM/QP CPU DMA_I2C1_SDA line through Qseven MXM Connector 62nd pin through default populated*
80	DMA_I2C2_SDA	IO, 3.3V OD	DMA_I2C2 Data. *Note: This pin is connected to i.MX 8 QM/QP CPU DMA_I2C2_SDA line through Qseven MXM Connector 68th pin through default populated resistor.*

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8 QM/QP Qseven Development Platform technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The i.MX 8 QM/QP Qseven Carrier Board is designed to work with a +12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the Qseven Carrier Board through Power Jack (J4). This 2.5mm x 6.5mm barrel connector Jack should fit standard DC Plugs with an inner dimension of 2.5mm and an outer dimension of 5.5mm (DC Plug Centre Pin is Positive). This connector is physically placed at the top of the board as shown below.

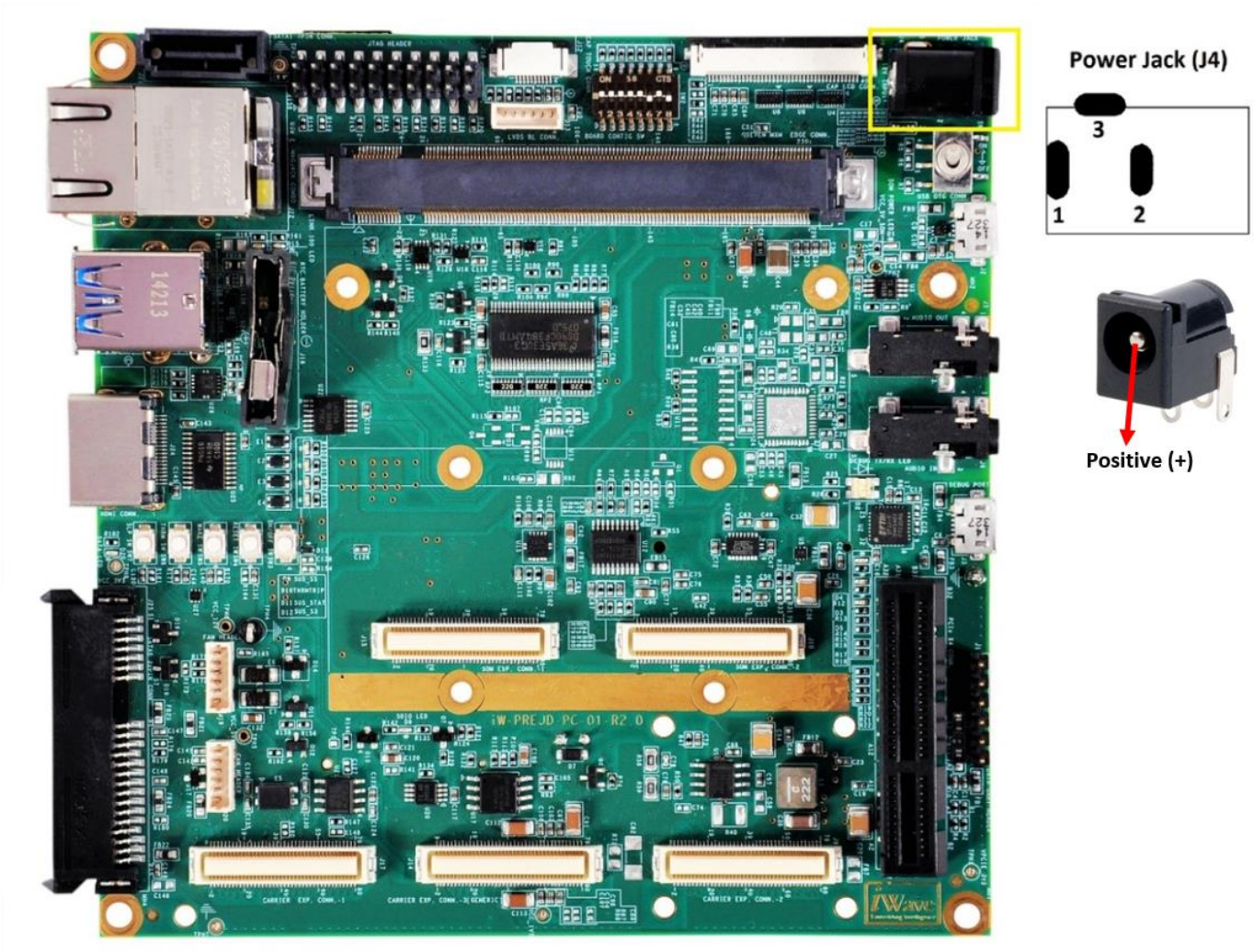

Figure 26: Power Jack

Table 14: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V[1]	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[2]	2.8V	3V	3.3V	±20mV

[1] Qseven Carrier Board is designed to work with 12V, 2A input power from external Power adapter.

[2] This voltage is from Coin cell holder and used as backup power source to RTC circuit of i.MX 8 QM/QP Qseven SOM when SOM VCC is off. This is an optional power and required only if RTC functionality is used.

Important Note: All carrier board power supplies should be powered ON only after the i.MX 8 QM/QP CPU is powered ON completely in the i.MX 8 QM/QP Qseven SOM. This is to ensure that there is no back voltage (leakage) from any supply on the board towards the i.MX 8 QM/QP CPU IO pins.

3.2 Power Output Specification

The i.MX 8 QM/QP Qseven Carrier Board has dedicated power regulator to provide +5V power to Qseven SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided to Qseven SOM for Real time clock support.

The i.MX 8 QM/QP Qseven carrier board also shares on board +5V, +3.3V and +1.5V power to Expansion connector3 for Add-On Module power.

Table 15: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current (mA)
Power to Qseven SOM (through Qseven MXM connector)					
1	VCC_5V_SOM	4.85V	5V	5.15V	4000mA
2	VRTC_3V0	2.8V	3V	3.3V	-
Power to Add-On Module (through Expansion connector3)					
2	VCC_5V	4.85V	5V	5.15V	1500mA
3	VCC_3V3	3.15	3.3	3.45	1000mA
4	VCC_1V5	1.35	1.5	1.65	500mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX8 Qseven Development Platform.

Table 16: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	60°C

[1] *iWave guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's i.MX 8 QM/QP Qseven Development Platform is designed by using RoHS3 compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's i.MX 8 QM/QP Qseven Development Platform is sensitive to electrostatic discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the Development Platform except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8 QM/QP Qseven Carrier Board Mechanical Dimensions

i.MX 8 QM/QP Qseven Development Platform PCB size is 120 mm x 120 mm x 1.6mm. Qseven carrier card mechanical dimensions is shown below. (All dimensions are shown in mm)

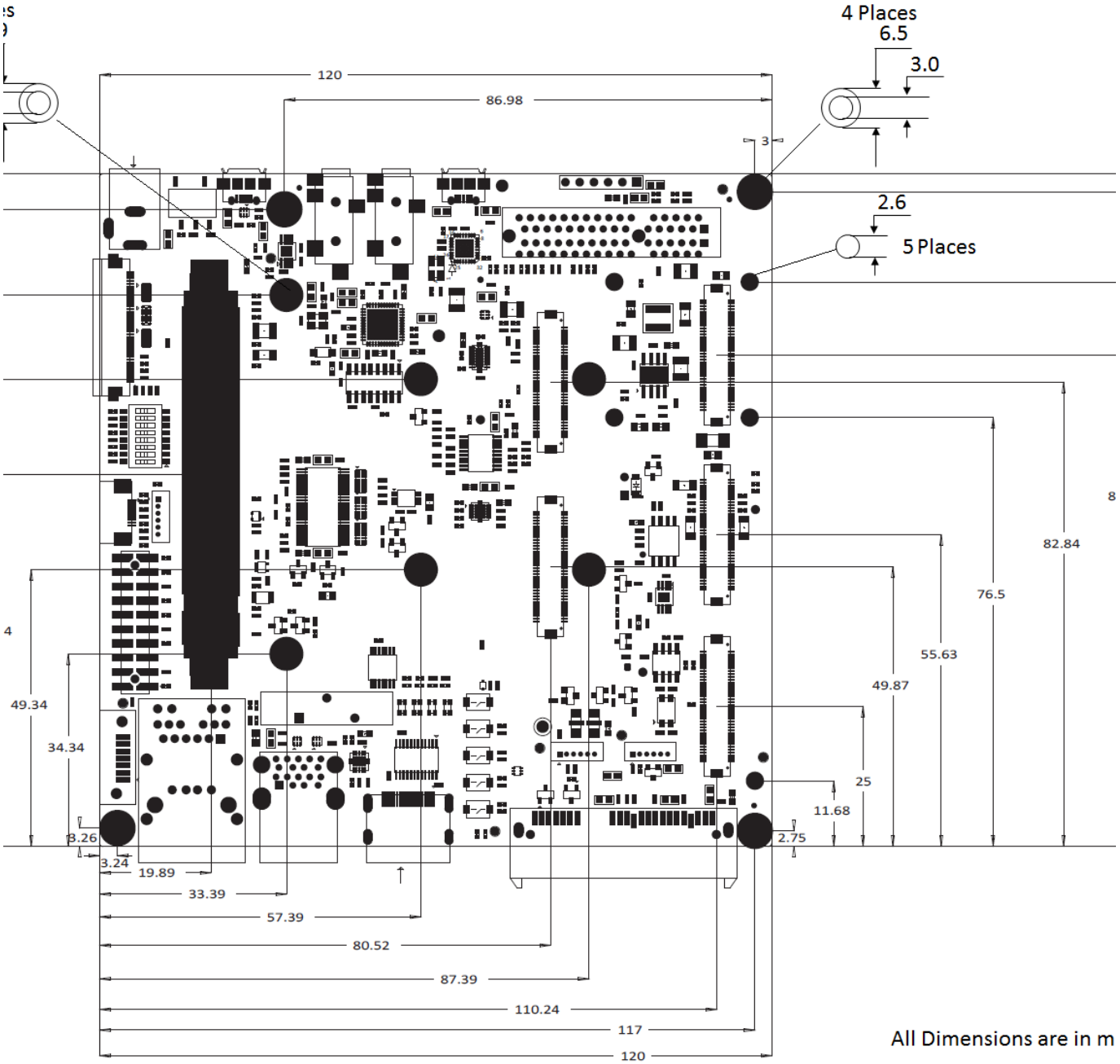

Figure 27: Mechanical dimensions of i.MX 8 QM/QP Qseven Carrier Board- Top View

i.MX 8 QM/QP Qseven Development Platform PCB thickness is 1.6mm±0.16mm, top side maximum height component is connector Ethernet Jack J22 (23.24mm) and bottom side maximum height component Ground Test Point (5.59mm). Please refer the below figure which gives height details of the i.MX 8 QM/QP Qseven Development kit.

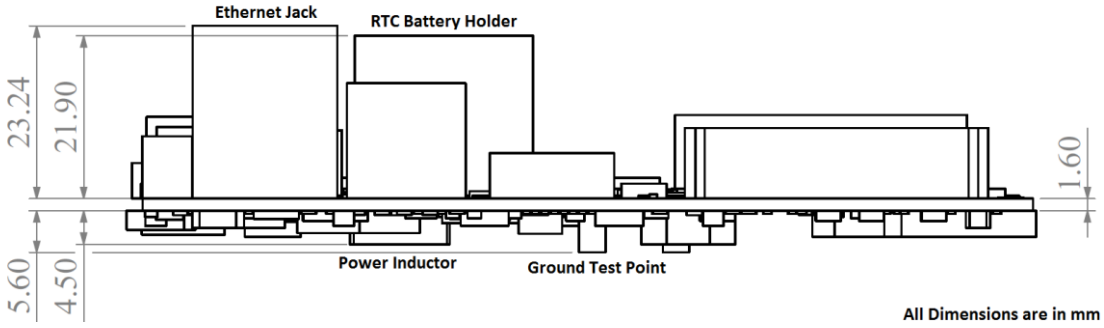

Figure 28: Mechanical dimensions of i.MX 8 QM/QP Qseven Carrier Board - Side View

3.4.2 Guidelines to insert the Qseven SOM into Carrier Board

- Make sure that power is not provided to the carrier board.
- Insert the Qseven module in to the MXM connector at an angle of 30° as shown in below image.
- Check the Notch position of Qseven module is proper while inserting.
- Once the Qseven module is inserted to the MXM connector properly, press the board vertically down as shown below, such that the board is fixed firmly into the expansion connectors and fix the board by screwing.

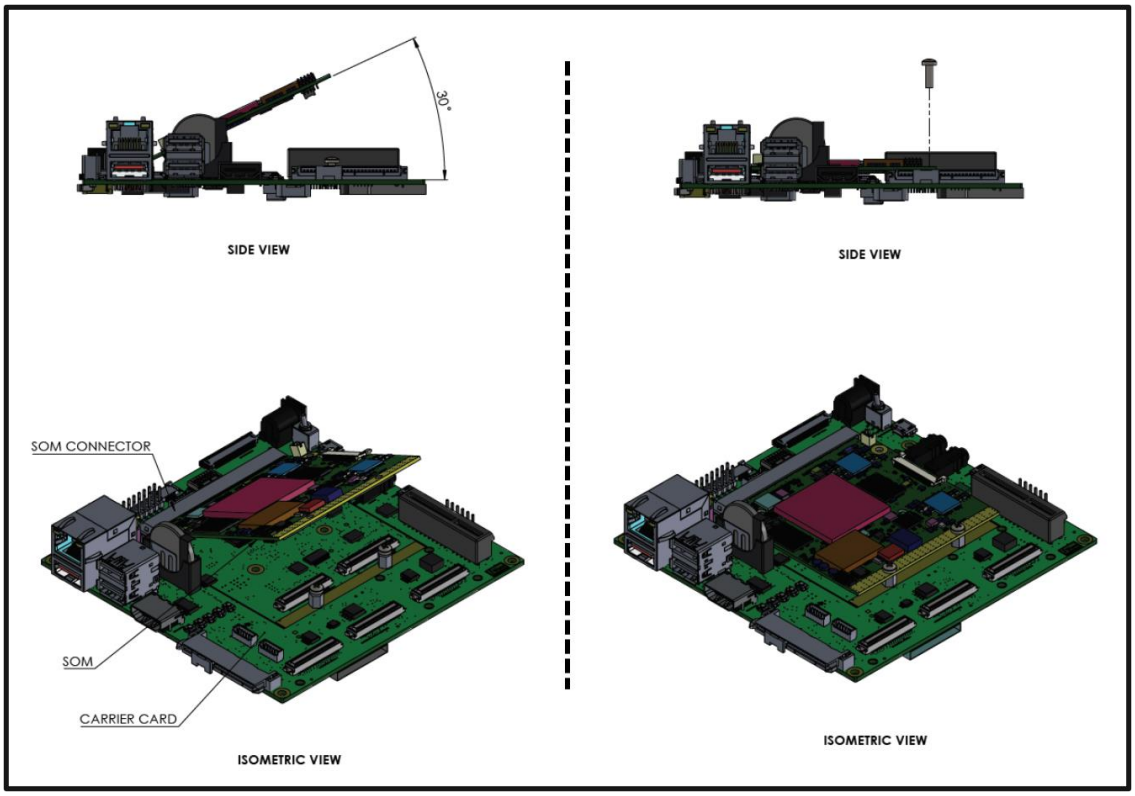

Figure 29: SOM Insertion Guideline

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8 QM/QP Qseven Development Platform which includes i.MX8 QM/QP Qseven SOM and Qseven carrier board.

Table 17: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G27D-Q7QM-4L004G-E016G-LCA	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Linux Kit with LCD display	0°C to 60°C
iW-G27D-Q7QM-4L004G-E016G-ACA	i.MX8 Quad Max, 4GB LPDDR4, 16GB eMMC flash Android Kit with LCD display	0°C to 60°C
iW-G27D-Q7QM-4L008G-E032G-LCA	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Linux Kit with LCD display	0°C to 60°C
iW-G27D-Q7QM-4L008G-E032G-ACA	i.MX8 Quad Max, 8GB LPDDR4, 32GB eMMC flash Android Kit with LCD display	0°C to 60°C

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.