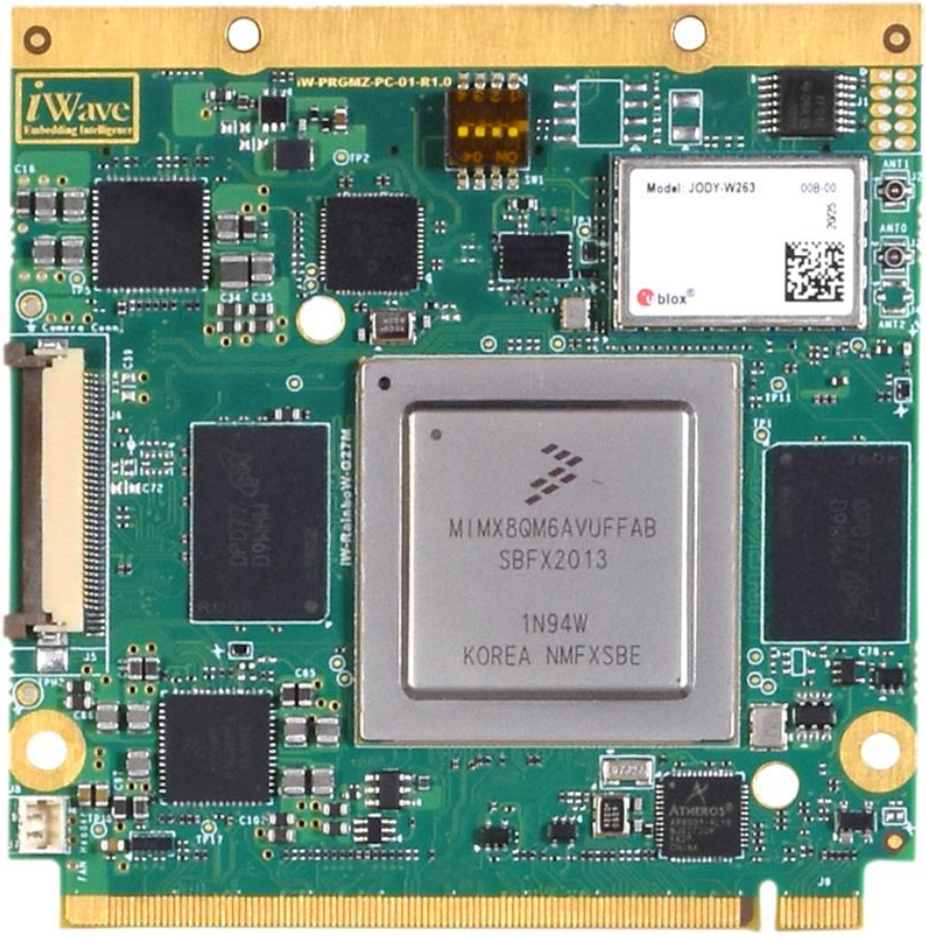
iW-RainboW-G27M

i.MX 8 QM/QP Qseven System On Module Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the Qseven SOM based on the NXP's i.MX 8 QM/QP Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX 8 QM/QP Qseven SOM from a Hardware Systems perspective.

1.2 Qseven SOM Overview

The Qseven is a versatile small form factor computer Module definition, targeting application that require low power, low costs, and high performance. The Modules are used as building blocks for portable and stationary embedded systems. The core SoC and support circuits, including DRAM, boot flash, power sequencing, SoC power supplies, GBE, dual channel LVDS/MIPI display transmitter are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

NXP's i.MX 8 QM/QP SoC based Qseven System on Module is rich with i.MX 8 QM/QP features along with on SOM LPDDR4, eMMC, Gigabit Ethernet PHY, USB3.0 Hub, Wi-Fi & BT module and comes in compact 70mm x 70mm form factor. The Module PCB has 230 edge fingers that mate with a low profile 230 pin 0.5mm pitch right angle connector.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
SoC	System on Chip
SOM	System On Module
BT	Bluetooth
CAN	Controller Area Network
CMOS	Complementary Metal-Oxide Semiconductor
CPU	Central Processing Unit
CTS	Clear to Send
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec

Acronyms	Abbreviations
GPIO	General Purpose Input Output
GPU	Graphics Processing Unit
HDMI	High-Definition Multimedia Interface
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound
IC	Integrated Circuit
JTAG	Joint Test Action Group
LPDDR4	Low Power Double Data Rate4
LVDS	Low Voltage Differential Signal
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
OTG	On-The-Go
PCB	Printed Circuit Sheet
PCIe	Peripheral Component Interconnect express
PMIC	Power management integrated circuits
RAM	Random Access Memory
RGMII	Reduced gigabit media-independent interface
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
RTS	Request to Send
SAI	Serial Audio Interface
SD	Secure Digital
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity
SATA	Serial Advanced Technology Attachment
SPDIF	The Sony/Philips Digital Interface
MLB	Media Local Bus

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
GBE	Gigabit Ethernet Signal
LVDS	Low Voltage Differential Signal
MIPI	Mobile Industry Processor Interface Signal
OD	Open Drain Signal
OC	Open Collector Signal
PCIe	Peripheral Component Interconnect Express Signal
USB	Universal Serial Bus Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-Qseven SOM.

1.5 References

- iMX8QMAEC_ Rev.x.pdf
- iMX8QM_RM_Rev_x.pdf
- Qseven Specification v2.1

1.6 Important Note

In this document, wherever i.MX 8 QM/QP SoC signal name is mentioned, it is followed as per below format for easy understanding.

- If SoC pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: ENET_TXC

  In this signal, ***ENET_TXC*** pad is used for same functionality.

- If SoC pin selected as GPIO function, then the signal name is mentioned as

  "Functionality Description (GPIO Number)"

  Example: BCONFIG_0(GPIO1_9)

  In this signal, ***BCONFIG_0*** is the GPIO functionality which we are using and ***GPIO1_9*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to SoC.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX 8 QM/QP Qseven SOM features and Hardware architecture with high level block diagram.

2.1 i.MX 8 QM/QP Qseven SOM Block Diagram

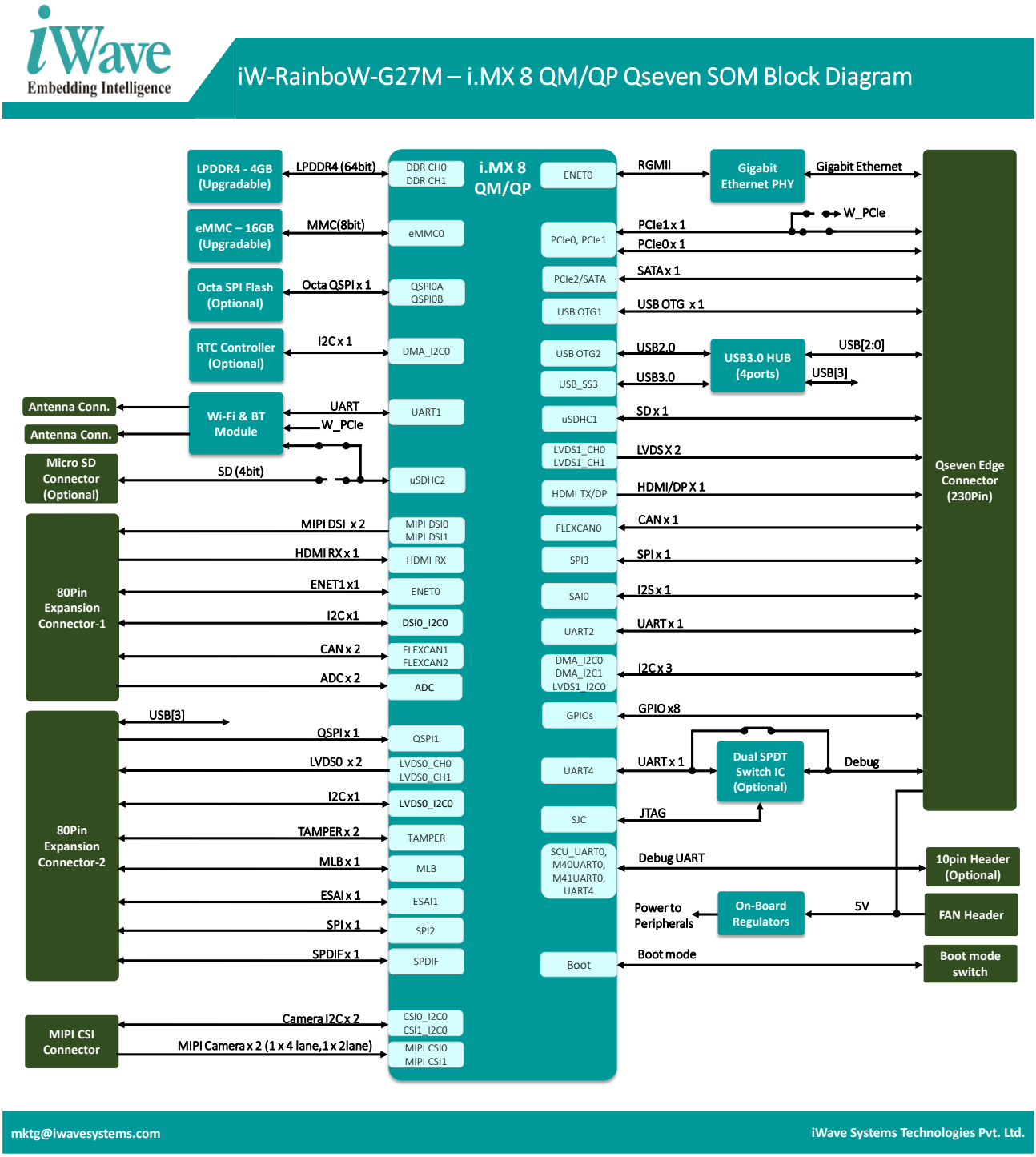


Figure 1: i.MX 8 QM/QP Qseven SOM Block Diagram

2.2 i.MX 8 QM/QP Qseven SOM Features

i.MX 8 QM/QP Qseven SOM supports the following features.

SoC

- i.MX8 QM/QP Processor[1]:
  - i.MX8 QuadMax : 2 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F
  - i.MX8 QuadPlus : 1 x Cortex-A72, 4 x Cortex-A53 & 2 x Cortex-M4F

Power

- PF8100 PMIC x 2

Memory

- LPDDR4 - 4GB (Expandable up to 8GB)[2,3]
- eMMC Flash - 16GB (Expandable)[3,4]
- Micro SD Connector (Optional)[5]
- FlexSPI Flash (Optional)

Other On-SOM Features

- WiFi 802.11a/b/g/n/ac + Bluetooth 5.0 Module[5,6]
- Gigabit Ethernet PHY Transceiver
- USB 3.0 High Speed 4-Port Hub
- RTC Controller (Optional)
- FAN Header
- UART Header (Optional)

MIPI-CSI2 Camera Connector

- MIPI CSI x 2 Channel (1 x 4 lane,1 x 2lane)
- CSI-I2C x 2

Qseven PCB Edge Interfaces

- PCIe Gen 3.0 x 2 Port
- SATA 3.0 x 1 Port
- USB Host 3.0 x 3 Port (through On-SOM USB Hub)
- USB Host 2.0 x 3 Port (through On-SOM USB Hub)
- USB OTG 2.0 x 1 Port
- Gigabit Ethernet x 1 Port (through On-SOM Gigabit Ethernet PHY transceiver)
- LVDS1 x 2 Port

- SDIO(4bit) x 1 Port
- HDMI/DP x 1 Port[7]
- SPI x 1 Port
- I2S (Audio Interface) x 1 Port
- CAN x 1 Port
- Data UART (with CTS & RTS) x 1 Port
- PWM x 3
- I2C x 3
- JTAG/Debug UART x 1[8]
- GPIO's
- Power & Management Signals

Expansion Connector1 Interfaces (Optional)

- MIPI-DSI x 2 Channel
- HDMI Receiver x 1 Channel
- ENET1 x 1
- I2C x 1
- CAN x 2 Port
- ADC x 2
- PWM x 1
- GPIO's

Expansion Connector2 Interfaces (Optional)

- LVDS0 x 2 Channel
- USB Host 3.0 X 1 (through On-SOM USB Hub)
- USB Host 2.0 X 1 (through On-SOM USB Hub)
- QSPI x 1
- I2C x 1
- TAMPER x 2
- MLB x 1 Port
- ESAI x 1 Port
- SPI x 1 Port
- SPDIF x 1 Port

General Specification

- Power Supply : 5V,2.5A
- Form Factor : 70mm X 70mm

1. *There are two configurations of i.MX 8 QM/QP Processor supported by NXP, hence in this document i.MX 8 QM/QP is used to represent either of one based on SOM Part Number.*
2. *The i.MX 8 can support up to 16GB RAM but considering the available LPDDR4 configuration, it can support 8GB RAM by using two 4GB LPDDR4 chips. If 8GB (64Gb) LPDDR4 chips are available then 16GB RAM can be supported on Board.*
3. *Memory Size will differ based on iWave's SOM Product Part Number.*
4. *16GB and 32GB eMMC are already validated on i.MX8 QM platform.*
5. *JODY-W2 Wi-Fi is supported by using SDIO interface, hence On SOM microSD will be an optional feature.*
6. *802.11ax (Wi-Fi 6) can be supported by changing from JODY-W2 to JODY-W3*
7. *The i.MX 8 support HDMI or Display Port through same pins, hence any one can be supported at a time based on SOM part Number.*
8. *The i.MX 8 support JTAG and Debug UART interface, but in Qseven Specification JTAG and Debug UART interface are multiplexed hence any one can be used via on SOM multiplexer.*

2.3 SoC

iW-RainboW-G27M Qseven SOM can support i.MX 8 Soc from NXP. The i.MX 8 Family consists of two processors: i.MX 8 QuadMax & i.MX 8 QuadPlus. The Major Difference between i.MX 8 processors are:

- i.MX 8 QuadMax : 2 x Cortex-A72 @ 1.6 GHz, 4 x Cortex-A53 @ 1.2 GHz & 2 x Cortex-M4F @ 264 MHz
- i.MX 8 QuadPlus : 1 x Cortex-A72 @ 1.6 GHz, 4 x Cortex-A53 @ 1.2 GHz & 2 x Cortex-M4F@ 264 MHz

The i.MX 8 QM/QP processors along with ARM core it supports dual 32-core GPU subsystems, 4K, H.265 capable VPU, and dual failover-ready display controllers, 2× 4K displays, supporting multiple display output options, including MIPI-DSI, HDMI 2.0, eDP/DP, and LVDS. Memory interfaces supporting LPDDR4, Quad SPI/Octal SPI (FlexSPI), eMMC 5.1, SD 3.0 and a wide range of peripheral I/Os such as PCIe 3.0 provide wide flexibility.

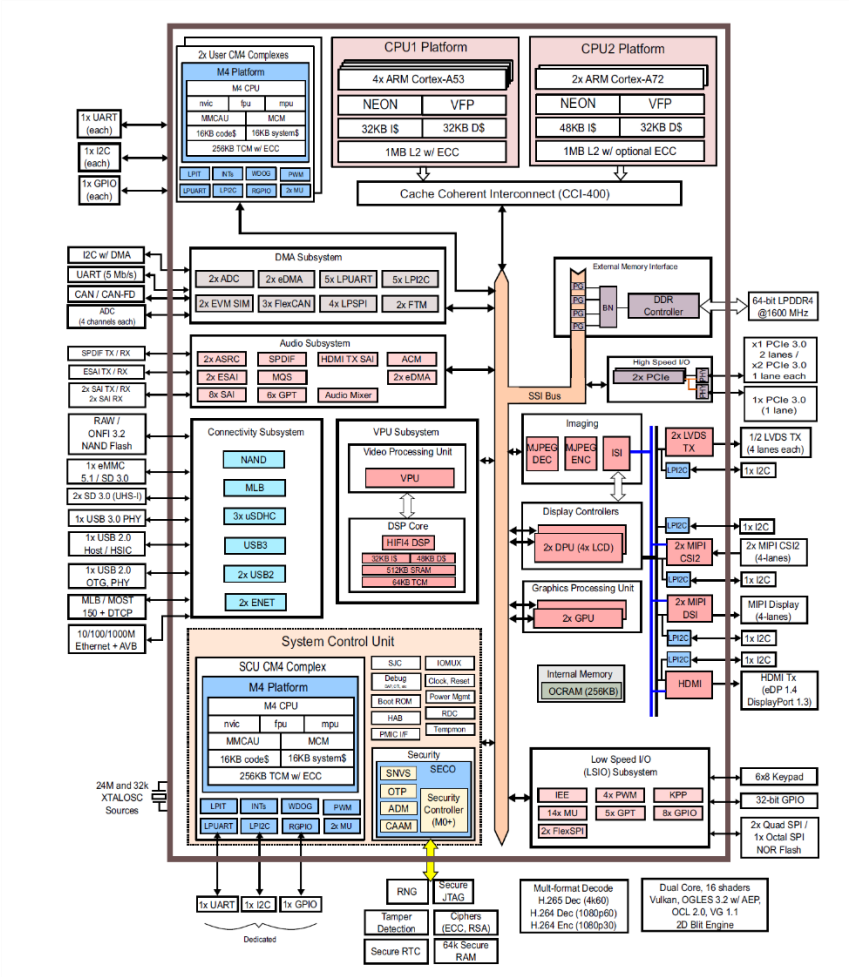


Figure 1. i.MX 8QuadMax System Block Diagram

Figure 2: i.MX 8 Block Diagram

Note: The i.MX 8 QM/QP processor offers numerous advanced features, please refer the latest i.MX 8 Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PMIC

i.MX 8 QM/QP Qseven SOM uses two PF8100/PF8200 PMIC for SOM Power management. Both the PF8100 PMIC are programmed with custom Sequence code EP and EQ from NXP.

The PF8100 is a power management integrated circuit (PMIC) features seven high efficiency buck converters and four linear regulators for powering the processor, memory and miscellaneous peripherals. Built-in one-time programmable memory stores key start up configurations, drastically reducing external components typically used to set output voltage and sequence of external regulators. Regulator parameters are adjustable through high-speed 3.4 MHz I2C after start up offering flexibility for different system states. The PF8100 PMIC U16 (EP) & U4 (EQ) comes in 56pin 8x8 QFN Packages and are placed on the Top side of the SOM.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX 8 QM/QP Qseven SOM supports 4GB RAM using two 32bit 2GB LPDDR4 IC connected to DDR_CH0 and DDR_CH1 channels of CPU to support LPDDR4 up to 1.6 GHz. Both the LPDDR4 parts U10 and U11 are placed on Top side of the SOM. LPDDR4 memory size can be customised based on the requirement by contacting iWave support team.

2.5.2 eMMC Flash

The i.MX 8 QM/QP Qseven SOM supports 16GB eMMC as default boot and storage device. This is connected to eMMC0 version 5.1 controller of the i.MX 8 SoC and operates at 1.8V (I/O supply) and 3.3V (NAND core supply) Voltage levels.

The eMMC flash (U26) memory is physically located on bottom side of the Qseven SOM. The memory size of the eMMC Flash can be customised based on the requirement by contacting iWave Support Team.

2.5.3 Micro SD Connector (Optional)

The i.MX 8 QM/QP Qseven SOM optionally supports Micro SD connector which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J12) is connected to the USDHC2 controller of the i.MX 8 SoC. The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX 8 Qseven SOM supports configurable I/O voltage levels for USDHC2 lines through LDO2OUT of PMIC1/PMIC2. The I/O voltage level of USDHC2 lines can be set 1.8V or 3.3V based on PMIC configuration. And the micro SD Connector is physically located on Bottom side of the i.MX 8 Qseven SOM.

Note: In default configuration USDHC2 is used for on board Wi-Fi module. Contact iWave Support team if microSD feature is required or refer Application Note: "TBD"

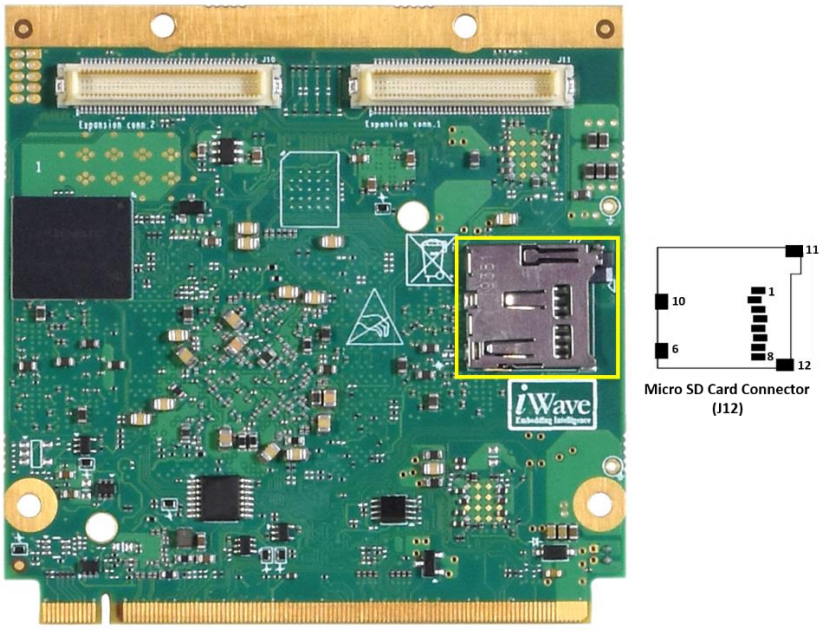


Figure 3: Micro SD Connector

2.5.4 FlexSPI Flash (Optional)

The i.MX 8 QM/QP Qseven SOM optionally supports FlexSPI using Micron's 512MB Xccela™ Flash Memory as a storage and can be used as optional boot device. FlexSPI is connected to QSPI0 controller of the i.MX 8 processor and operates at 1.8V Voltage levels. The Xccela™ Flash (U25) memory is physically located on Bottom side of the Qseven SOM. The FlexSPI can be supported with customised memory size based on the requirement by contacting iWave Support Team.

Note: If FlexSPI Flash feature is required, contact iWave Support Team or refer Application Note: "TBD"

2.6 RTC Controller (Optional)

The i.MX 8 QM/QP Qseven SOM supports external RTC Controller “PCF85263” On-SOM for Real time clock support. This external RTC Controller IC (U3) is connected to i.M X 8 QM/QP SoC through DMA_I2C1 Interface and operates at 3.3V voltage level. In SOM power off condition, this device will take power from Qseven PCB Edge - Pin No. 193 (VRTC_3V0) coin cell power input and continues to keep the current time.

2.7 Wi-Fi and Bluetooth Interface

The i.MX 8 QM/QP Qseven SOM is integrated with u-blox's "JODY-W263" based Wi-Fi & Bluetooth module. The JODY-W2 series are compact modules based on the Marvell 88W8987 AEC-Q100 compliant chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication. The JODY-W2 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz

• Dual-mode Bluetooth 5, including audio, can be operated fully simultaneous with Wi-Fi

The JODY-W2 undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX 8 Qseven SOM uses processor's UART1 interface for Bluetooth and USDHC2 interface for Wi-Fi in a default configuration.

In i.MX 8 QM/QP Qseven SOM, antenna pins of JODY-W263 Bluetooth and Wi-Fi are connected to J3 and J2 connector respectively.

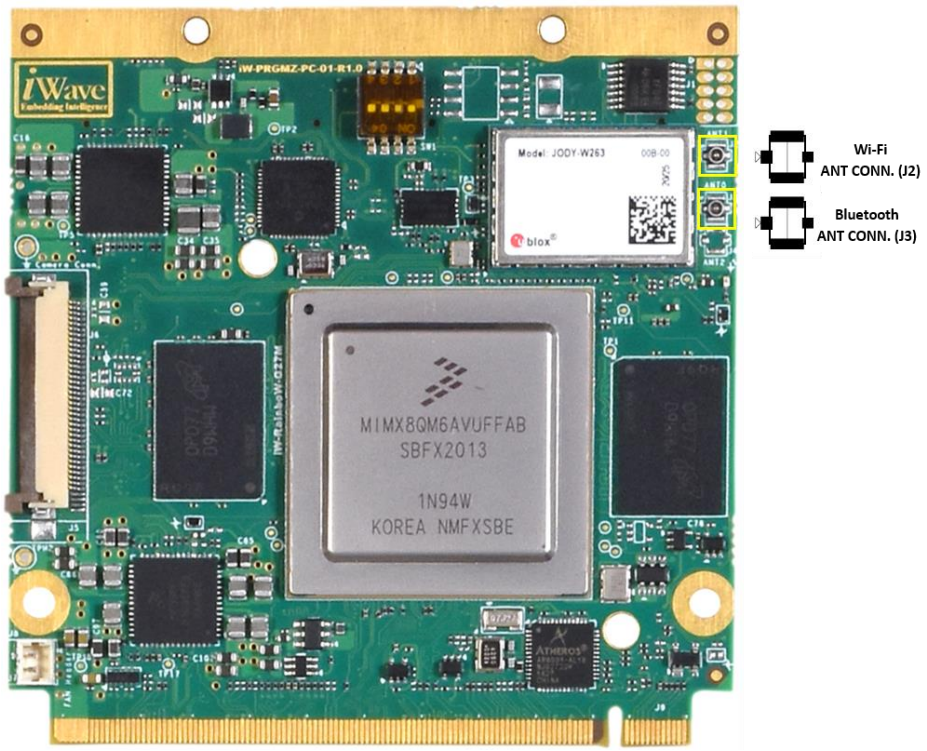


Figure 4: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number - : MM4829-2702RA4 from Murata Electronics.

Antenna Part Number - : 2042811100 from Molex/FXP830.24.0100B from Taoglas Limited

Note: In default configuration 802.11ax (Wi-Fi 6) is not supported, but 802.11ax can be supported by changing Wi-Fi module from JODY-W2 to JODY-W3, contact iWave Support Team for further information.

2.8 MIPI-CSI2 Camera Connector

The i.MX 8 SoC supports two 4-lane camera interfaces, the CSI-2 Rx Controller Core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The Local Interface is an easy-to-use pixel-based interface that supports 1 to 4 virtual channels and all data types. The Local interface runs at the User Interface clock rate for all implementations. The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus.

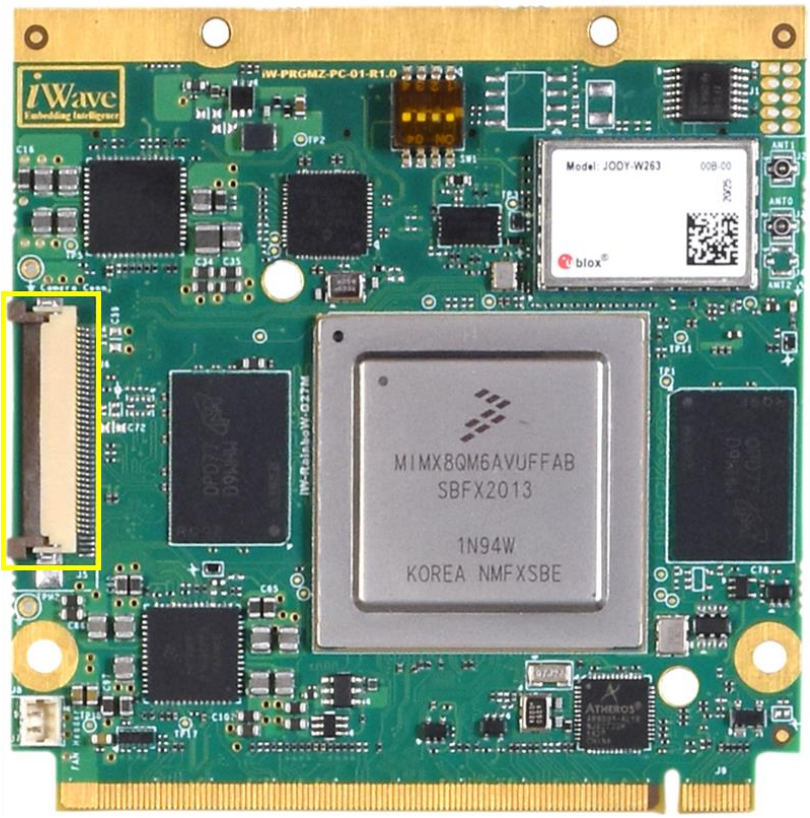


Figure 5: MIPI CSI Connector

Number of Pins - : 36

Connector Part - : FH12A-36S-0.5SH(55)

For more details on MIPI-CSI2 pinouts on Camera connector, refer below table:

Table 3: MIPI-CSI2 Camera Connector

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	CAM_PWR	NA	Power	3V3 Camera Power
2	CAM_PWR	NA	Power	3V3 Camera Power

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
3	MIPI_CSI0_DATA0_P	MIPI_CSI0_DATA0_P/ BF22	I, MIPI	MIPI CSI0 differential data lane 0 positive.
4	MIPI_CSI0_DATA0_N	MIPI_CSI0_DATA0_N/ BE23	I, MIPI	MIPI CSI0 differential data lane 0 negative.
5	GND	NA	Power	Ground.
6	MIPI_CSI0_DATA1_P	MIPI_CSI0_DATA1_P/ BF18	I, MIPI	MIPI CSI0 differential data lane 1 positive.
7	MIPI_CSI0_DATA1_N	MIPI_CSI0_DATA1_N/ BE19	I, MIPI	MIPI CSI0 differential data lane 1 negative.
8	GND	NA	Power	Ground.
9	MIPI_CSI0_DATA2_P	MIPI_CSI0_DATA2_P/ BF24	I, MIPI	MIPI CSI0 differential data lane 2 positive.
10	MIPI_CSI0_DATA2_N	MIPI_CSI0_DATA2_N/ BE25	I, MIPI	MIPI CSI0 differential data lane 2 negative.
11	CAM0_RST(GPIO1_27)	MIPI_CSI0_GPIO0_00/ BL23	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal
12	MIPI_CSI0_DATA3_P	MIPI_CSI0_DATA3_P/ BF16	I, MIPI	MIPI CSI0 differential data lane 3 positive.
13	MIPI_CSI0_DATA3_N	MIPI_CSI0_DATA3_N/ BE17	I, MIPI	MIPI CSI differential data lane 3 negative.
14	GND	NA	Power	Ground.
15	MIPI_CSI0_CLK_P	MIPI_CSI0_CLK_P/ BF20	I, MIPI	MIPI CSI0 differential Clock positive.
16	MIPI_CSI0_CLK_N	MIPI_CSI0_CLK_N/ BE21	I, MIPI	MIPI CSI0 differential Clock negative.
17	GND	NA	Power	Ground.
18	MIPI_CSI0_I2C0_SCL	MIPI_CSI0_I2C0_SCL/ BH24	I, 1.8V OD/ 2.2K PU	I2C Clock for MIPI CSI0 Camera.
19	MIPI_CSI0_I2C0_SDA	MIPI_CSI0_I2C0_SDA/ BN19	IO, 1.8V OD/ 2.2K PU	I2C Data for MIPI CSI0 Camera.
20	CAM0_EN(GPIO1_28)	MIPI_CSI0_GPIO0_01/ BM22	I, 1.8V CMOS 10K PU	Camera 0 Enable (active low).
21	MIPI_CSI0_MCLK_OUT	MIPI_CSI0_MCLK_OUT/ BJ23	I, 1.8V CMOS	NC *Note: Optionally Master Clock.*
22	CAM1_EN(GPIO4_20)	LSIO.GPIO4.IO20/ G11	I, 1.8V CMOS 10K PU	Camera 1 Enable (active low).
23	MIPI_CSI1_I2C0_SCL	MIPI_CSI1_I2C0_SCL/ BN17	I, 1.8V OD/ 2.2K PU	I2C Clock for MIPI_CSI1 Camera.
24	MIPI_CSI1_I2C0_SDA	MIPI_CSI1_I2C0_SDA/ BE15	IO, 1.8V OD/ 2.2K PU	I2C Data for MIPI_CSI1 Camera.
25	GND	NA	Power	Ground.
26	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/ BJ17	I, MIPI	MIPI CSI1 differential Clock positive.
27	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/ BH16	I, MIPI	MIPI CSI1 differential Clock negative.
28	GND	NA	Power	Ground.
29	MIPI_CSI1_DATA0_P	MIPI_CSI1_DATA0_P/ BJ19	I, MIPI	MIPI CSI1 differential data lane 0 positive.

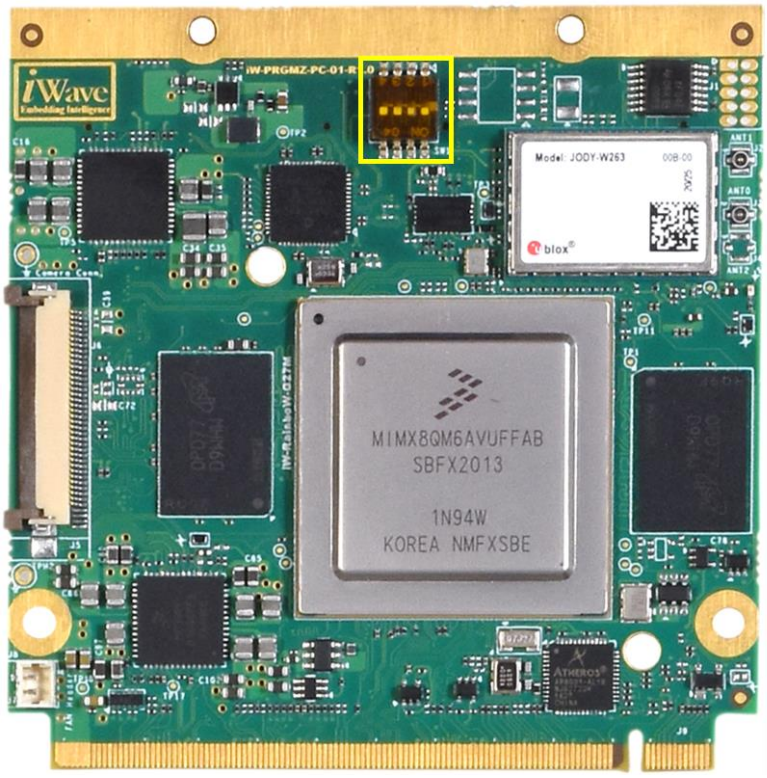
Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
30	MIPI_CSI1_DATA0_N	MIPI_CSI1_DATA0_N/ BH18	I, MIPI	MIPI CSI1 differential data lane 0 negative.
31	CAM1_RST(GPIO1_29)	MIPI_CSI1_MCLK_OUT/ BN23	I, 1.8V CMOS 10K PU	MIPI Camera Reset signal
32	MIPI_CSI1_DATA1_P	MIPI_CSI1_DATA1_P/ BJ15	I, MIPI	MIPI CSI1 differential data lane 1 positive.
33	MIPI_CSI1_DATA1_N	MIPI_CSI1_DATA1_N/ BH14	I, MIPI	MIPI CSI1 differential data lane 1 negative.
34	GND	NA	Power	Ground.
35	CAM0_GPIO(GPIO1_30)	MIPI_CSI1_GPIO0_00/ BN15	I/O, 1.8V CMOS	GPIO for Camera 0
36	CAM1_GPIO(GPIO1_31)	MIPI_CSI1_GPIO0_01/ BN13	I/O, 1.8V CMOS	GPIO for Camera 1

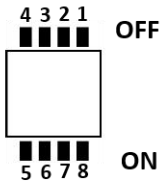
Note: Contact iWave team for Camera module

2.9 Boot Media Setting

i.MX 8 QM/QP Qseven SOM supports four positions Boot Media Switch (SW1) which is physically located in the top of the PCB. This switch is used to select the boot media of i.MX 8 QM/QP. i.MX 8 QM/QP Qseven SOM supports two boot media options for booting i.MX 8 QM/QP as mentioned in the below table. By default, eMMC boot media supported.

Note: Contact iWave if different boot media support is required other than eMMC flash.





Boot Media Selection Switch (SW1)

Figure 6: Boot Media Switch

Table 4: Boot Media Settings

Boot Media	SW1(4 Position Switch)			
	POS1	POS2	POS3	POS4
Boot from Fuse	OFF	OFF	OFF	OFF
USB Serial Download	OFF	ON	OFF	OFF
eMMC Boot	OFF	OFF	ON	OFF
USDHC1 SD Boot	OFF	ON	ON	OFF
USDHC2 SD Boot	ON	ON	ON	OFF
FlexSPI Boot	OFF	OFF	ON	ON

2.10 Qseven PCB Edge Connector

i.MX 8 QM/QP Qseven SOM Supports 230pin Qseven PCB edge connector for interfaces expansion. The interfaces which are available at Qseven Edge connector are explained in the following sections.

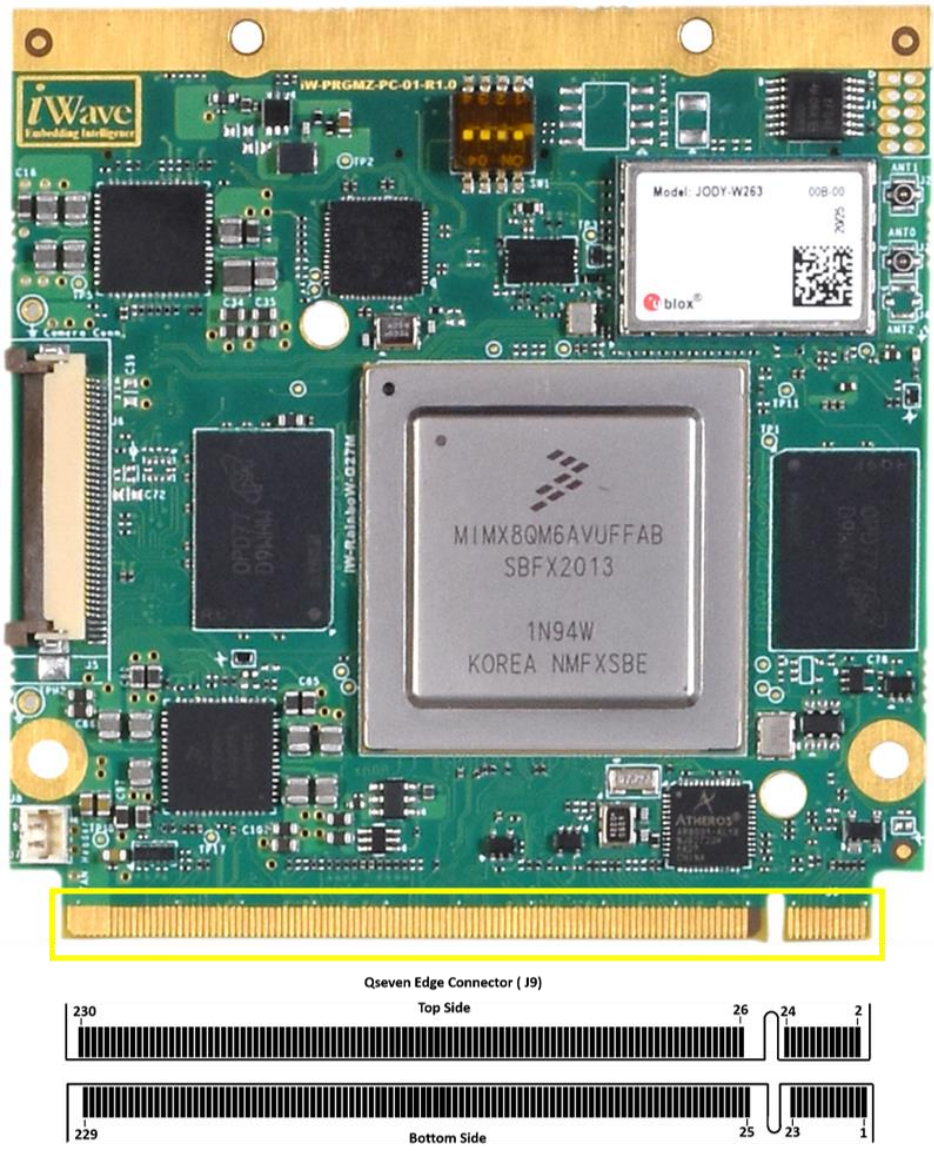


Figure 7: Qseven Edge Connector

Number of Pins - : 230

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 88882-2Dxx from Aces

BEC5230S9xFREDC from Yamaichi

AS0B32x-S78N-xF from FOXCONN

IMSA-18010S-230A-GN1 from IRISO

Table 5: Qseven Edge Connector Pinouts

Signal	Qseven Pin (Bottom)	Qseven Pin (Top)	Signal
GND	1	2	GND
GBE0_MDI3-	3	4	GBE0_MDI2-
GBE0_MDI3+	5	6	GBE0_MDI2+
GBE0_LINK100#	7	8	GBE0_LINK1000#
GBE0_MDI1-	9	10	GBE0_MDI0-
GBE0_MDI1+	11	12	GBE0_MDI0+
GPHY_LINK_LED	13	14	GBE0_LINK_ACT#
VPHY0_DVDDL	15	16	SUS_S5_Q7
WAKE#(GPIO3_04)	17	18	SUS_S3_Q7
SUS_STAT_Q7(GPIO2_05)	19	20	PWRBTN#
GPII_1(GPIO0_04)	21	22	GPII_0(GPIO3_03)
GND	23	24	GND
Key			
GND	25	26	PWRGIN
GPII_2(GPIO0_05)	27	28	RSTBN
PCIE_SATA0_TX0_P	29	30	NC
PCIE_SATA0_TX0_N	31	32	NC
GPIO_SATA_ACT#(GPIO1_18)	33	34	GND
PCIE_SATA0_RX0_P	35	36	NC
PCIE_SATA0_RX0_N	37	38	NC
GND	39	40	GND
NC	41	42	uSDHC1_CLK
GPIO_SDC1_CD(GPIO1_23)	43	44	GPIO_SD1_LED(GPIO3_06)
uSDHC1_CMD	45	46	GPIO_SDC1_WP(GPIO1_22)
GPIO_SDC1_PWR_EN(GPIO1_19)	47	48	uSDHC1_DATA1
uSDHC1_DATA0	49	50	uSDHC1_DATA3
uSDHC1_DATA2	51	52	NC *(Note: Optionally uSDHC1_DATA5)*
NC *(Note: Optionally uSDHC1_DATA4)*	53	54	NC *(Note: Optionally uSDHC1_DATA7)*
NC *(Note: Optionally uSDHC1_DATA6)*	55	56	USB_OTG1_PWR(GPIO4_03)
GND	57	58	GND
SAI1_TXFS	59	60	DMA_I2C1_SCL
GPIO_RESET(GPIO1_05)	61	62	DMA_I2C1_SDA
SAI1_TXC	63	64	SMBUS_ALERT(GPIO1_15)
SAI1_RXD	65	66	DMA_I2C2_SCL
SAI1_TXD	67	68	DMA_I2C2_SDA
THRM#	69	70	Q7_WDTRIG_B
GPIO_THRMTRIP_Q7(GPIO3_05)	71	72	Q7_WDOG_B

Signal	Qseven Pin (Bottom)	Qseven Pin (Top)	Signal
GND	73	74	GND
USB3_HUB1_TXM	75	76	USB3_HUB1_RXM
USB3_HUB1_TXP	77	78	USB3_HUB1_RXP
NC	79	80	NC
USB3_HUB3_TXM	81	82	USB3_HUB3_RXM
USB3_HUB3_TXP	83	84	USB3_HUB3_RXP
USB_HUB3_OC/USB_HUB2_OC	85	86	USB_UB1_OC/USB_OTG1_OC(GPIO 0_03)
USB_HUB3OUT_DM	87	88	USB_HUB2OUT_DM
USB_HUB3OUT_DP	89	90	USB_HUB2OUT_DP
VBUS_OTG1	91	92	USB_ID
USB_OTG1_DM	93	94	USB_HUB1OUT_DM
USB_OTG1_DP	95	96	USB_HUB1OUT_DP
GND	97	98	GND
LVDS1_CH0_TX0_P	99	100	LVDS1_CH1_TX0_P
LVDS1_CH0_TX0_N	101	102	LVDS1_CH1_TX0_N
LVDS1_CH0_TX1_P	103	104	LVDS1_CH1_TX1_P
LVDS1_CH0_TX1_N	105	106	LVDS1_CH1_TX1_N
LVDS1_CH0_TX2_P	107	108	LVDS1_CH1_TX2_P
LVDS1_CH0_TX2_N	109	110	LVDS1_CH1_TX2_N
LCD1_VDD_EN(GPIO1_14)	111	112	LCD1_EN(GPIO1_09)
LVDS1_CH0_TX3_P	113	114	LVDS1_CH1_TX3_P
LVDS1_CH0_TX3_N	115	116	LVDS1_CH1_TX3_N
GND	117	118	GND
LVDS1_CH0_CLK_P	119	120	LVDS1_CH1_CLK_P
LVDS1_CH0_CLK_N	121	122	LVDS1_CH1_CLK_N
LCD1_BL_PWM(GPIO1_10)	123	124	HDMI_TX0_CEC
LVDS1_I2C0_SDA	125	126	NC *(Note: Optionally DMA_I2C2_SCL)*
LVDS1_I2C0_SCL	127	128	NC *(Note: Optionally DMA_I2C2_SDA)*
FLEXCAN0_TX	129	130	FLEXCAN0_RX
HDMI_TX0_CLK_P/EDP3_P	131	132	USB3_HUB2_TXM
HDMI_TX0_CLK_N/EDP3_N	133	134	USB3_HUB2_TXP
GND	135	136	GND
HDMI_TX0_DATA1_P/EDP1_P	137	138	EDP_AUX_P
HDMI_TX0_DATA1_N/EDP1_N	139	140	EDP_AUX_N
GND	141	142	GND
HDMI_TX0_DATA0_P/EDP2_P	143	144	USB3_HUB2_RXM
HDMI_TX0_DATA0_N/EDP2_N	145	146	USB3_HUB2_RXP
GND	147	148	GND

Signal	Qseven Pin (Bottom)	Qseven Pin (Top)	Signal
HDMI_TX0_DATA2_P/EDP0_P	149	150	HDMI_TX0_CTRL_DAT
HDMI_TX0_DATA2_N/EDP0_N	151	152	HDMI_TX0_CTRL_CLK
HDMI_TX_HPD	153	154	NC *(Note: Optionally DP_HPD)*
PCIE_A_REFCLK_P	155	156	PCIE_A_WAKE_B(GPIO4_28)
PCIE_A_REFCLK_N	157	158	PCIE_A_RST_B(GPIO4_29)
GND	159	160	GND
NC	161	162	NC
NC	163	164	NC
GND	165	166	GND
NC	167	168	NC
NC	169	170	NC
UART0_TX	171	172	UART0_RTS_B
PCIE1_B_TX0_P	173	174	PCIE1_B_RX0_P
PCIE1_B_TX0_N	175	176	PCIE1_B_RX0_N
UART0_RX	177	178	UART0_CTS_B
PCIE0_A_TX0_P	179	180	PCIE0_A_RX0_P
PCIE0_A_TX0_N	181	182	PCIE0_A_RX0_N
GND	183	184	GND
Q7_GPIO_0(GPIO3_12)	185	186	Q7_GPIO_1(GPIO3_02)
Q7_GPIO_2(GPIO3_14)	187	188	Q7_GPIO_3(GPIO3_11)
Q7_GPIO_4(GPIO1_08)	189	190	Q7_GPIO_5(GPIO1_11)
Q7_GPIO_6(GPIO5_00)	191	192	Q7_GPIO_7(GPIO0_00)
VDD_RTC	193	194	PWM2(GPIO0_19)
Q7_FAN_TECHOIN(GPIO0_01)	195	196	PWM3(GPIO0_16)
GND	197	198	GND
SPI3_MOSI	199	200	SPI3_CS0
SPI3_MISO	201	202	SPI3_CS1
SPI3_SCLK	203	204	MFG_NC4 *(Note: Optionally JTAG_TRSTB)*
NC	205	206	NC
JTAG_TCK	207	208	UART4_RX/JTAG_TDI
UART4_TX/JTDO_UTX	209	210	JTAG_TMS
NC	211	212	NC
NC	213	214	NC
NC	215	216	NC
NC	217	218	NC
VCC_5V	219	220	VCC_5V
VCC_5V	221	222	VCC_5V
VCC_5V	223	224	VCC_5V
VCC_5V	225	226	VCC_5V

Signal	Qseven Pin (Bottom)	Qseven Pin (Top)	Signal
VCC_5V	227	228	VCC_5V
VCC_5V	229	230	VCC_5V

2.10.1 Gigabit Ethernet

The i.MX8 QM/QP Qseven SOM supports one Gigabit Ethernet using on SOM Ethernet PHY "AR8031" from Atheros, Qualcomm. ENET0 of i.MX 8 is connected to GBE port of Qseven edge connector. The AR8031 integrates Atheros Green ETHOS® power saving technologies and significantly saves power not only during the work time, but also overtime. Atheros Green ETHOS® power savings include ultra-low power in cable unplugged mode or port power down mode, and automatic optimized power saving based on cable length. The AR8031 also supports IEEE 802.3az EEE standard (Energy Efficient Ethernet) and Atheros proprietary SmartEEE. SmartEEE allows legacy MAC/SoC devices without 802.3az support to function as a complete 802.3az system. Further, the AR8031 supports Wake-on-LAN (WoL) feature to be able to help manage and regulate total system power requirements. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX 8 QM/QP Qseven SOM also supports Link and Activity indication LED control signals for GBE port to Qseven PCB Edge connector.

For more details on GBE pinouts on Qseven PCB Edge connector, refer below Table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
10	GBE0_MDI0-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 negative.
12	GBE0_MDI0+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 0 positive.
9	GBE0_MDI1-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 negative.
11	GBE0_MDI1+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 1 positive.
4	GBE0_MDI2-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 negative.
6	GBE0_MDI2+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 2 positive.
3	GBE0_MDI3-	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 negative.
5	GBE0_MDI3+	NA	IO, GBE	Gigabit Ethernet MDI differential pair 3 positive.
15	VPHY0_DVDDL	NA	Power	Power Inductor pin of Gigabit Ethernet
13	GPHY_LINK_LED	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
8	GBE0_LINK1000#	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
14	GBE0_LINK_ACT#	NA	O, 3.3V CMOS	Gigabit Ethernet activity status.

2.10.2 PCIe Interface

The i.MX 8 SoC supports two Lane PCI Express 3.0 (PCIe gen3: 8GHz to get 8GHz baud clock) channels. In i.MX 8 Qseven SOM PCIe0 and PCIe1 lane are directly connected to Qseven Edge connector by default and as per Qseven specification TX lines are AC coupled with 0.22uF capacitors. Also, 100MHz reference clock is provided for both Channel 1 & Channel 2 from a single 100MHz Oscillator. PCIe wake and reset signals are supported in Qseven PCB Edge connector from i.MX 8 SoC General purpose IO GPIO4_28 and GPIO4_29 respectively.

Note: As per Qseven specification PCIe differential PCIe_TX lines are ac coupled on SOM itself and for PCIe_RX ac coupling has to be implemented close to the respective device. Also, PCIe differential clock lines from external clock oscillator are having On-SOM termination resistors and so no external termination is required.

For more details on PCIe pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
155	PCIE_A_REFCLK_P	NA	O, PCIe	PCIe Clock Positive. *Note: This signal is coming from 100MHz External Oscillator in SOM.*
157	PCIE_A_REFCLK_N	NA	O, PCIe	PCIe Clock Negative. *Note: This signal is coming from 100MHz External Oscillator in SOM.*
180	PCIE0_A_RX0_P	PCIE0_RX0_P /A29	I, PCIe	PCIe1 Receive Positive.
182	PCIE0_A_RX0_N	PCIE0_RX0_N /B30	I, PCIe	PCIe1 Receive Negative.
179	PCIE0_A_TX0_P	PCIE0_TX0_P /B26	O, PCIe / 0.22uF AC Couple	PCIe1 Transmit Positive.
181	PCIE0_A_TX0_N	PCIE0_TX0_N /C27	O, PCIe / 0.22uF AC Couple	PCIe1 Transmit Negative.
174	PCIE1_B_RX0_P	PCIE1_RX0_P /A21	I, PCIe	PCIe2 Receive Positive.
176	PCIE1_B_RX0_N	PCIE1_RX0_N /B22	I, PCIe	PCIe2 Receive Negative.
173	PCIE1_B_TX0_P	PCIE1_TX0_P /B24	O, PCIe / 0.22uF AC Couple	PCIe2 Transmit Positive.
175	PCIE1_B_TX0_N	PCIE1_TX0_N /C25	O, PCIe / 0.22uF AC Couple	PCIe2 Transmit Negative.
156	PCIE_A_WAKE_B(GPIO4_28)	PCIE_CTRL0_WAKE_B/ A15	I, 3.3V CMOS	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.
158	PCIE_A_RST_B(GPIO4_29)	PCIE_CTRL0_PERST_B/ D20	O, 3.3V CMOS	Reset Signal for external devices

2.10.3 SATA Interface

The i.MX8 SoC supports SATA-3(Gen3: 6GHz to get 6GHz baud clock). This is in addition to the standard PCIe 3.0 and connected to Qseven SATA Edge connector pins via 0.022uF AC coupled capacitors on both TX an RX lines.

For more details on SATA pinouts, refer below table:

Pin No.	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
29	PCIE_SATA0_TX0_P	PCIE_SATA0_ TX0_P/ B16	O, SATA / 0.022uF AC Couple	SATA Transmit Lane Positive
31	PCIE_SATA0_TX0_N	PCIE_SATA0_ TX0_N/ C17	O, SATA / 0.022uF AC Couple	SATA Transmit Lane Negative
35	PCIE_SATA0_RX0_P	PCIE_SATA0_ RX0_P/ A19	I, SATA / 0.022uF AC Couple	SATA Receive Lane Positive
37	PCIE_SATA0_RX0_N	PCIE_SATA0_ RX0_N/ B20	I, SATA / 0.022uF AC Couple	SATA Receive Lane Negative
33	GPIO_SATA_ACT#(GPIO1_18)	MIPI_DSI0_ GPIO0_00/BD30	O, 3.3V OC	Serial ATA Led. Open collector output pin driven during SATA command activity.

2.10.4 SD Interface

The i.MX 8 Qseven SOM supports 4bit SD interface over Qseven PCB Edge connector which can be used to connect SD card as Mass storage or optional boot device. uSDHC1 controller of the i.MX8 SoC is used to support Qseven SD interface. uSDHC1 operates in 3.3V IO level and supports maximum of 25 Mbit/s per line in High speed mode. SDIO Power enable signal is supported in Qseven PCB Edge connector from i.MX 8 SoC General purpose IO GPIO1_19.

For more details on SD pinouts on Qseven PCB Edge connector, refer below Table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
45	uSDHC1_CMD	USDHC1_CMD /G41	IO, 3.3V CMOS	SD command. *Note: 10K pullup option is provided.*
42	uSDHC1_CLK	USDHC1_CLK /J39	O, 3.3V CMOS	SD Clock. *Note: 10K pullup option is provided.*
49	uSDHC1_DATA0	USDHC1_DATA0 /E37	IO, 3.3V CMOS	SD data 0. *Note: 10K pullup option is provided.*
48	uSDHC1_DATA1	USDHC1_DATA1 /F38	IO, 3.3V CMOS	SD data 1. *Note: 10K pullup option is provided.*
51	uSDHC1_DATA2	USDHC1_DATA2 /E39	IO, 3.3V CMOS	SD data 2. *Note: 10K pullup option is provided.*
50	uSDHC1_DATA3	USDHC1_DATA3 /F40	IO, 3.3V CMOS	SD data 3. *Note: 10K pullup option is provided.*
43	GPIO_SDC1_CD (GPIO1_23)	MIPI_DSI1_GPIO0 _01 /BK24	I, 3.3V CMOS 10K PU	SD Card Detect.
46	GPIO_SDC1_WP(GPIO1_2 2)	MIPI_DSI1_GPIO0 _00/BM24	I, 3.3V CMOS 10K PU	SD Write protect.
47	GPIO_SDC1_PWR_EN(GPI O1_19)	MIPI_DSI0_GPIO0 _01/BD28	O, 3.3V CMOS	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.

2.10.5 USB Interface

The i.MX 8 SoC supports two USB2.0 OTG and one USB_SS3. In i.MX 8 Qseven SOM USB_OTG1 goes to Qseven OTG connector and USB_OTG2 goes to on SOM USB3.0 hub USB5744-I/2G from Microchip along with CPUs USB_SS3 lines. USB Hub feature's controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports. The Downstream ports of Hub are connected to Qseven Edge connector and Expansion connector.

For more details on USB 2.0 OTG1 pinouts near Qseven edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
95	USB_OTG1_DP	USB_OTG1_DP / B40	IO, USB	USB2.0 Port0 Data Plus.
93	USB_OTG1_DM	USB_OTG1_DM / C39	IO, USB	USB2.0 Port0 Data Minus.
56	USB_OTG1_PWR (GPIO4_03)	USB_SS3_TC0/ J9	IO, 3.3V CMOS	USB OTG Power Enable/ Over Current Indicator.
91	VBUS_OTG1	USB_OTG1_VBUS/ A39	I, 5V Power	USB host power detection, when this port is used as a device.
92	USB_OTG_ID	USB_OTG1_ID/ A37	I, 3.3V CMOS	USB OTG ID.
86	USB_OTG1_OC(GPIO0_03)	LSIO.GPIO0.IO03/ AL43	I, 3.3V CMOS	USB Port Over Current Indicator.

For more details on USB 2.0 pinouts near Qseven edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
94	USB_HUB1OUT_DM	NA	IO, DIFF	USB Host Port 1 data negative. *Note: Connected to USB Hub.*
96	USB_HUB1OUT_DP	NA	IO, DIFF	USB Host Port 1 data positive. *Note: Connected to USB Hub.*
88	USB_HUB2OUT_DM	NA	IO, DIFF	USB Host port 2 data negative. *Note: Connected to USB Hub.*
90	USB_HUB2OUT_DP	NA	IO, DIFF	USB Host port 2 data positive. *Note: Connected to USB Hub.*
87	USB_HUB3OUT_DM	NA	IO, DIFF	USB Host port 3 data negative. *Note: Connected to USB Hub.*
89	USB_HUB3OUT_DP	NA	IO, DIFF	USB Host port 3 data positive. *Note: Connected to USB Hub.*
85	USB_HUB3_OC/USB_HUB2_OC	NA	I, 3.3V CMOS/ 10K PU	Over current sense for USB port 2 & 3. *Note: Connected to USB Hub.*
86	USB_HUB1_OC	NA	I, 3.3V CMOS/ 10K PU	Over current sense for USB port 0 & 1. *Note: Connected to USB Hub.*

For more details on USB 3.0 pinouts near Qseven edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
77	USB3_HUB1_TXP	NA	O, USB SS	USB3.0 Port1 Transmit Plus. *Note: Connected to USB Hub.*
75	USB3_HUB1_TXM	NA	O, USB SS	USB3.0 Port1 Transmit Minus. *Note: Connected to USB Hub.*
78	USB3_HUB1_RXP	NA	I, USB SS	USB3.0 Port1 Receive Plus. *Note: Connected to USB Hub.*
76	USB3_HUB1_RXM	NA	I, USB SS	USB3.0 Port1 Receive Minus. *Note: Connected to USB Hub.*
134	USB3_HUB2_TXP	NA	O, USB SS	USB3.0 Port2 Transmit Plus. *Note: Connected to USB Hub.*
136	USB3_HUB2_TXM	NA	O, USB SS	USB3.0 Port2 Transmit Minus. *Note: Connected to USB Hub.*
146	USB3_HUB2_RXP	NA	I, USB SS	USB3.0 Port2 Receive Plus. *Note: Connected to USB Hub.*
144	USB3_HUB2_RXM	NA	I, USB SS	USB3.0 Port2 Receive Minus. *Note: Connected to USB Hub.*
83	USB3_HUB3_TXP	NA	O, USB SS	USB3.0 Port3 Transmit Plus. *Note: Connected to USB Hub.*
81	USB3_HUB3_TXM	NA	O, USB SS	USB3.0 Port3 Transmit Minus. *Note: Connected to USB Hub.*
84	USB3_HUB3_RXP	NA	I, USB SS	USB3.0 Port3 Receive Plus. *Note: Connected to USB Hub.*
82	USB3_HUB3_RXM	NA	I, USB SS	USB3.0 Port3 Receive Minus. *Note: Connected to USB Hub.*

2.10.6 LVDS Display Interface

Qseven Specification supports dual channel LVDS interfaces over edge connector. i.MX 8 Processor has LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface. The LVDS signals are connected to Qseven PCB Edge connector.

For more details on DSI pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
99	LVDS1_CH0_TX0_P	LVDS1_CH0_TX0_P/ BN37	LVDS, DIFF	LVDS1 channel0 differential pair 0 positive.
101	LVDS1_CH0_TX0_N	LVDS1_CH0_TX0_N/ BL37	LVDS, DIFF	LVDS1 channel0 differential pair 0 negative.
103	LVDS1_CH0_TX1_P	LVDS1_CH0_TX1_P/ BM38	LVDS, DIFF	LVDS1 channel0 differential pair 1 positive.
105	LVDS1_CH0_TX1_N	LVDS1_CH0_TX1_N/ BK38	LVDS, DIFF	LVDS1 channel0 differential pair 1 negative.
107	LVDS1_CH0_TX2_P	LVDS1_CH0_TX2_P/ BN39	LVDS, DIFF	LVDS1 channel0 differential pair2 positive.
109	LVDS1_CH0_TX2_N	LVDS1_CH0_TX2_N/ BL39	LVDS, DIFF	LVDS1 channel0 differential pair 2 negative.
113	LVDS1_CH0_TX3_P	LVDS1_CH0_TX3_P/ BM40	LVDS, DIFF	LVDS1 channel0 differential pair 3 positive.
115	LVDS1_CH0_TX3_N	LVDS1_CH0_TX3_N/ BK40	LVDS, DIFF	LVDS1 channel0 differential pair 3 negative.
119	LVDS1_CH0_CLK_P	LVDS1_CH0_CLK_P/ BM36	LVDS, DIFF	LVDS1 channel0 differential clock positive.
121	LVDS1_CH0_CLK_N	LVDS1_CH0_CLK_N/ BK36	LVDS, DIFF	LVDS1 channel0 differential clock negative.
100	LVDS1_CH1_TX0_P	LVDS1_CH1_TX0_P/ BN33	LVDS, DIFF	LVDS1 channel1 differential pair 0 positive.
102	LVDS1_CH1_TX0_N	LVDS1_CH1_TX0_N/ BL33	LVDS, DIFF	LVDS1 channel1 differential pair 0 negative.
104	LVDS1_CH1_TX1_P	LVDS1_CH1_TX1_P/ BM32	LVDS, DIFF	LVDS1 channel1 differential pair 1 positive.
106	LVDS1_CH1_TX1_N	LVDS1_CH1_TX1_N/ BK32	LVDS, DIFF	LVDS1 channel1 differential pair 1 negative.
108	LVDS1_CH1_TX2_P	LVDS1_CH1_TX2_P/ BN31	LVDS, DIFF	LVDS1 channel1 differential pair2 positive.
110	LVDS1_CH1_TX2_N	LVDS1_CH1_TX2_N/ BL31	LVDS, DIFF	LVDS1 channel1 differential pair 2 negative.
114	LVDS1_CH1_TX3_P	LVDS1_CH1_TX3_P/ BM30	LVDS, DIFF	LVDS1 channel1 differential pair 3 positive.
116	LVDS1_CH1_TX3_N	LVDS1_CH1_TX3_N/ BK30	LVDS, DIFF	LVDS1 channel1 differential pair 3 negative.
120	LVDS1_CH1_CLK_P	LVDS1_CH1_CLK_P/ BM34	LVDS, DIFF	LVDS1 channel1 differential clock positive.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
122	LVDS1_CH1_CLK_N	LVDS1_CH1_CLK_N/ BK34	LVDS, DIFF	LVDS1 channel1 differential clock negative.
111	LCD1_VDD_EN(GPIO1_14)	LVDS1_I2C1_SCL/ BD32	O, 3.3V CMOS	Controls panel power enable
123	LCD1_BL_PWM(GPIO1_10)	LVDS1_GPIO00/ BD34	O, 3.3V CMOS	Backlight brightness via pulse width modulation (PWM)
112	LCD1_EN(GPIO1_09)	LVDS0_I2C1_SDA/ BE35	O, 3.3V CMOS	Controls panel backlight enable.

2.10.7 HDMI/DP Interface

The i.MX 8 SoC HD Display Transmitter Controller IP offers multi-protocol support of standards such as High Definition Multimedia Interface (HDMI), DisplayPort, embedded DisplayPort (eDP), with one of these standards supported at a time. These protocols enable switching between the modes to be applied on a system level and performed by means of software configuration. i.MX 8 SoC supports HDMI 1.4 Specification, HDMI 2.0a Specification, DisplayPort Specification Version 1.3 and eDP Specification Version 1.4 protocols.

In i.MX 8 Qseven SOM, HDMI and Display Transmitter output signals are multiplexed in same pins of Qseven edge connector and at a time anyone can be used, buy default HDMI is supported.

For more details on HDMI/eDP pinouts, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
131	HDMI_TX0_CLK_P/ EDP3_P	HDMI_TX0_CLK_EDP3_P/BL3	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential CLK Positive *Note: Optionally connected to Display Port Lane 3 Positive*
133	HDMI_TX0_CLK_N/ EDP3_N	HDMI_TX0_CLK_EDP3_N/BK2	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential CLK Negative *Note: Optionally connected to Display Port Lane 3 Negative*
137	HDMI_TX0_DATA1_P/ EDP1_P	HDMI_TX0_DATA1_EDP1_P /BL7	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 1 Positive *Note: Optionally connected to Display Port Lane 1 Positive*
139	HDMI_TX0_DATA1_N/ EDP1_N	HDMI_TX0_DATA1_EDP1_N /BM6	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 1 Negative *Note: Optionally connected to Display Port Lane 1 Negative*
143	HDMI_TX0_DATA0_P/ EDP2_P	HDMI_TX0_DATA0_EDP2_P /BL5	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 0 Positive

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
				Note: Optionally connected to Display Port Lane 2 Positive
145	HDMI_TX0_DATA0_N/ EDP2_N	HDMI_TX0_DATA0_EDP2_N /BM4	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 0 Negative *Note: Optionally connected to Display Port Lane 2 Negative*
149	HDMI_TX0_DATA2_P/ EDP0_P	HDMI_TX0_DATA2_EDP0_P /BL9	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 2 Positive *Note: Optionally connected to Display Port Lane 0 Positive*
151	HDMI_TX0_DATA2_N/ EDP0_N	HDMI_TX0_DATA2_EDP0_N /BM8	O, HDMI or EDP/ 0.1uF AC Couple	HDMI differential data lane 2 Negative *Note: Optionally connected to Display Port Lane 0 Negative*
150	HDMI_TX0_CTRL_DAT	HDMI_TX0_DDC_SDA/ BN5	IO, 3.3V CMOS	HDMI DDC I2C DATA *Note: Optionally connected to CPU ball BG3.*
152	HDMI_TX0_CTRL_CLK	HDMI_TX0_DDC_SCL/ BG1	O, 3.3V CMOS	HDMI DDC I2C Clock *Note: Optionally connected to CPU ball BH2.*
124	HDMI_TX0_CEC	HDMI_TX0_CEC/ BJ1	I, 3.3V CMOS	Consumer electronics control bus (CEC) of HDMI
153	HDMI_TX_HPD	HDMI_TX0_HPD / BH8	I, 3.3V CMOS/1M PD	HDMI Hot Plug Detect
138	EDP_AUX_P	HDMI_TX0_AUX_P / BH2	O, EDP/ 0.1uF AC Couple	Display Port AUX Positive
140	EDP_AUX_N	HDMI_TX0_AUX_N / BG3	O, EDP/ 0.1uF AC Couple	Display Port AUX Negative
154	DP_HPD(GPIO0_02)	LSIO.GPIO0.IO02/ AN45	I, 3.3V CMOS	Display Port Plug Detect

2.10.8 Audio Interface

The i.MX 8 Qseven SOM supports one I2S channels in Qseven Edge connector from SoC SAI1 channel. The SAI peripheral provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and Supports graceful restart after FIFO error. Only Transmitter Clock and Transmitter Left-Right Clock (LRCK) is supported as per Qseven specification.

In i.MX 8 Qseven SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio Interface pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
59	SAI1_TXFS	SAI1_TXFS /AV2	O, 3.3V CMOS	SAI1 Transmitter Frame Sync.
67	SAI1_TXD	SAI1_TXD /AU1	O, 3.3V CMOS	SAI1 Transmit Data Lane 0.
65	SAI1_RXD	SAI1_RXD/AV4	I, 3.3V CMOS	SAI1 Receive Data Lane 0.
63	SAI1_TXC	SAI1_TXC /AU5	O, 3.3V CMOS/ 33E Series	SAI1 Transmitter Bit Clock.
61	GPIO_RESET(GPIO1_05)	LVDS0_GPIO01/BD40	O, 3.3V CMOS	SAI1 Reset.

2.10.9 Data UART Interface

The i.MX 8 Qseven SOM supports one UART channels with CTS and RTS. The i.MX 8 SoC UART0 connected to Qseven Edge connector can be used for any data communication.

For more details on UART pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
171	UART0_TX	UART0_TX /AV48	O, 3.3V CMOS	UART0 Transmitter.
177	UART0_RX	UART0_RX /AV50	I, 3.3V CMOS	UART0 Receiver.
178	UART0_CTS_B	UART0_CTS_B /AW49	I, 3.3V CMOS	UART0 Clear to Send.
172	UART0_RTS_B	UART0_RTS_B /AU45	O, 3.3V CMOS	UART0 Request to Send

2.10.10 SPI Interface

The i.MX 8 SoC supports low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum clock speed of 40MHz. The i.MX 8 Qseven SOM supports one SPI channel in Qseven Edge connector with SPI3 of SoC side.

For more details on SPI pinouts, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
200	SPI3_CS0	SPI3_CS0/BG5	O, 3.3V CMOS/10K PU	SPI Chip Select 0
202	SPI3_CS1	SPI3_CS1/BD8	O, 3.3V CMOS/10K PU	SPI Chip Select 1
203	SPI3_SCLK	SPI3_SCLK/BF6	O, 3.3V CMOS/ 33E Series	SPI Clock
201	SPI3_MISO	SPI3_MISO/BE5	I, 3.3V CMOS	SPI Master IN Slave Out
199	SPI3_MOSI	SPI3_MOSI/ BF2	O, 3.3V CMOS	SPI Master Out Slave In

2.10.11 CAN Interface

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. The CAN protocol was primarily designed to be used as a vehicle serial data bus meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. The FLEXCAN module is a full implementation of the CAN protocol specification, which supports both standard and extended message frames. 64 Message Buffers are supported by the FlexCAN module. The i.MX 8 SoC supports three CAN interface and CAN0 interface is connected to Qseven Edge connector.

For more details on CAN pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
129	FLEXCAN0_TX	FLEXCAN0_TX/H6	O, 3.3V CMOS	Transmit output for CAN bus.
130	FLEXCAN0_RX	FLEXCAN0_RX/C5	I, 3.3V CMOS	Receive output for CAN bus.

2.10.12 I2C Interface

The i.MX 8 QM/QP Qseven SOM supports two general purpose I2C and one LVDS I2C interface on Qseven PCB Edge connector. i.MX 8 QM/QP SoCs' DMA_I2C1, DMA_I2C2 & LVDS_I2C interfaces are connected to Qseven PCB Edge connector.

For more details on I2C Interface pinouts on Qseven PCB edge connector, refer the below table.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
60	DMA_I2C1_SCL	DMA.I2C1.SCL /AY52	O, 3.3V OD/ 2.2K PU	I2C1 Serial Clock for General Purpose
62	DMA_I2C1_SDA	DMA.I2C1.SDA /AV52	IO, 3.3V OD/ 2.2K PU	I2C1 Serial Data for General Purpose.
66	DMA_I2C2_SCL	DMA.I2C2.SCL /BA53	O, 3.3V OD/ 2.2K PU	I2C2 Serial Clock for General Purpose. *Note: Same signal is optionally connected to Qseven edge connector 128th pin.*
68	DMA_I2C2_SDA	DMA.I2C2.SDA / AY50	IO, 3.3V OD/ 2.2K PU	I2C2 Serial Data for General Purpose. *Note: Same signal is optionally connected to Qseven edge connector 126th pin*
127	LVDS1_I2C0_SCL	LVDS1_I2C0_SCL/BL35	O, 3.3V OD/ 2.2K PU	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I2C data line.
125	LVDS1_I2C0_SDA	LVDS1_I2C0_SDA/E33	IO, 3.3V OD/ 2.2K PU	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I2C data line.

2.10.13 JTAG/Debug UART Interface

The i.MX 8 Qseven SOM supports JTAG/Debug UART interface for SoC debug purpose. The System JTAG Controller (SJC) provides debug and test control with the maximum security. The test access port (TAP) is designed to support features compatible with the IEEE Standard 1149.1 v2001 (JTAG). As per Qseven specification debug UART and JTAG signals are connected through on SOM multiplexer. Same time any one interface can be used in Qseven edge.

For more details on JTAG pinouts on Qseven PCB Edge connector, refer below table:

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
204	MFG_NC4	NA	I, 3.3V CMOS/ 10K PU	Used as control signal for a multiplexer circuit on the module enabling secondary function. When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes. By default, UART is Connected to edge. *Note: Optionally connect to JTAG_TRSTB*
208	JTDI_URX	NA	I, 3.3V CMOS	Via a multiplexer, as a UART_RX signal connected to Qseven edge. *Note: Via a multiplexer, as a JTAG_TDI signal can be connected to edge.*
210	JTAG_TMS	JTAG_TMS/BA49	I, 3.3V CMOS	JTAG test mode select.
207	JTAG_TCK	JTAG_TCK/BC51	I, 3.3V CMOS	JTAG test Clock.
209	JTDO_UTX	NA	O, 3.3V CMOS	Via a multiplexer, as a UART_TX signal connected to Qseven edge. *Note: Via a multiplexer, as a JTAG_TDO signal can be connected to edge.*

2.10.14 GPIO Interface

The i.MX 8 Qseven SOM supports GPIOs on Qseven PCB Edge connector. The i.MX 8 SoC GPIO (general-purpose input/output) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register.

For more details on GPIO Interface pinouts on Qseven PCB edge connector, refer the below table.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
185	Q7_GPIO_0(GPIO3_12)	SAI1_RXC/AV6	IO, 3.3V CMOS	General purpose input/output 0.
186	Q7_GPIO_1(GPIO3_02)	SPI0_SCK/BB4	IO, 3.3V CMOS	General purpose input/output 1.
187	Q7_GPIO_2(GPIO3_14)	SAI1_RXFS/AU3	IO, 3.3V CMOS	General purpose input/output 2.
188	Q7_GPIO_3(GPIO3_11)	SPI2_CS1/AY2	IO, 3.3V CMOS	General purpose input/output 3.
189	Q7_GPIO_4(GPIO1_08)	LVDS0_I2C1_SCL/BE37	IO, 3.3V CMOS	General purpose input/output 4.
190	Q7_GPIO_5(GPIO1_11)	LVDS1_GPIO01/BH36	IO, 3.3V CMOS	General purpose input/output 5.
191	Q7_GPIO_6(GPIO5_00)	PCIE_CTRL1_PERST_B/G25	IO, 3.3V CMOS	General purpose input/output 6.
192	Q7_GPIO_7(GPIO0_00)	LSIO.GPIO0.IO00/AL45	IO, 3.3V CMOS	General purpose input/output 7.

Note: These signals are default configured as input GPIOs (General Purpose Input/Output).

2.10.15 Power Control Signals

Qseven v2.1 specification supports control Signals, For more details on supported control Signals pinouts on Qseven PCB Edge connector and corresponding pin description, refer the below table.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
26	PWGIN	NA	I,5V CMOS/ 10K PU	High active input for the Qseven module to indicates that all power rails located on the carrier board are ready for use.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
20	PWRBTN#	ON_OFF_BUTTON/ BE47	I, 3.3V CMOS/ 10K PU	Power ON /OFF Input to SOM.

2.10.16 Power Management Signals

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
28	RSTBN	POR_B/BE49	I,3.3V CMOS 10K PU	Hard RESET Input to SOM.
17	WAKE#(GPIO3_04)	SPI0_SDI/ BA5	I, 3.3V CMOS	External system wake event.
16	SUS_S5#	NA	0, 3.3V CMOS 10K PU	
18	SUS_S3#	NA	0, 3.3V CMOS 10K PU	

2.10.18 Miscellaneous, Thermal & Fan Control Signals

The i.MX 8 Qseven SOM PCB Edge Connector includes the remaining signals from i.MX 8 SoC which includes Watchdog, GPII and PWM Signals. For more details on these signals pinout on Qseven Edge Connector, refer the below table.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
70	WDTRIG#	NA	I, 3.3V CMOS 10K PU	Watchdog trigger signal.
72	WDOUT	NA	I, 3.3V CMOS 100K PU	Watchdog event indicator.
64	SMBUS_ALERT(GPIO1_15)	LVDS1_I2C1_SDA/BN35	IO, 3.3V CMOS	System Management Bus Alert input
194	PWM2(GPIO0_19)	LSIO.GPIO0.IO19/ BA51	O, 3.3V CMOS	PWM1 Output.
196	PWM3(GPIO0_16)	PWM3(GPIO0_16)/ AW53	O, 3.3V CMOS	PWM2 Output.
22	GPII_0(GPIO3_03)	SPI0_SDO/AY6	I, 3.3V CMOS	General Purpose Input 0
21	GPII_1(GPIO0_04)	LSIO.GPIO0.IO04/AT48	I, 3.3V CMOS	General Purpose Input 1
27	GPII_2(GPIO0_05)	LSIO.GPIO0.IO05/AP46	I, 3.3V CMOS	General Purpose Input 2
69	THRM#	NA	O, 3.3V CMOS	Thermal Alarm active low signal
71	GPIO_THRMTRIP_Q7(GPIO3_05)	SPI0_CS0/BC1	I, 3.3V CMOS 10K PU	Thermal Trip indicates an overheating condition of the SoC.
195	Q7_FAN_TECHOIN(GPIO0_01)	LSIO.GPIO0.IO01/AP48	I, 3.3V CMOS	Fan tachometer input

2.10.19 Power and GND

The i.MX 8 QM/QP Qseven SOM works with single 5V power input (VCC) from Qseven Edge connector and generates all other required powers internally On-SOM itself. i.MX 8 QM/QP Qseven coin cell power input (VDD_RTC) from Qseven PCB Edge Connector to On-SOM RTC controller for real time clock.

Qseven Pin No.	Qseven Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
219, 220, 221, 222, 223, 224, 225, 226, 227, 228, 229 & 230	VCC_5V	NA	I, 5V Power	Supply Voltage.
1, 2, 23, 24, 25, 34, 39, 40, 57, 58, 73, 74, 97, 98, 117, 118, 135, 136, 141, 142, 147, 148, 159, 160, 165, 166, 183, 184, 197 & 198	GND	NA	Power	Ground.
193	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.11 SOM Expansion Connector1 (Optional)

The i.MX 8 Qseven SOM supports an 80pin Expansion connector1 (J11) as a optional feature to utilise extra interfaces which is not covered under Qseven specification V2.1 edge connector. The SOM Expansion connector is placed on the bottom side of the SOM.

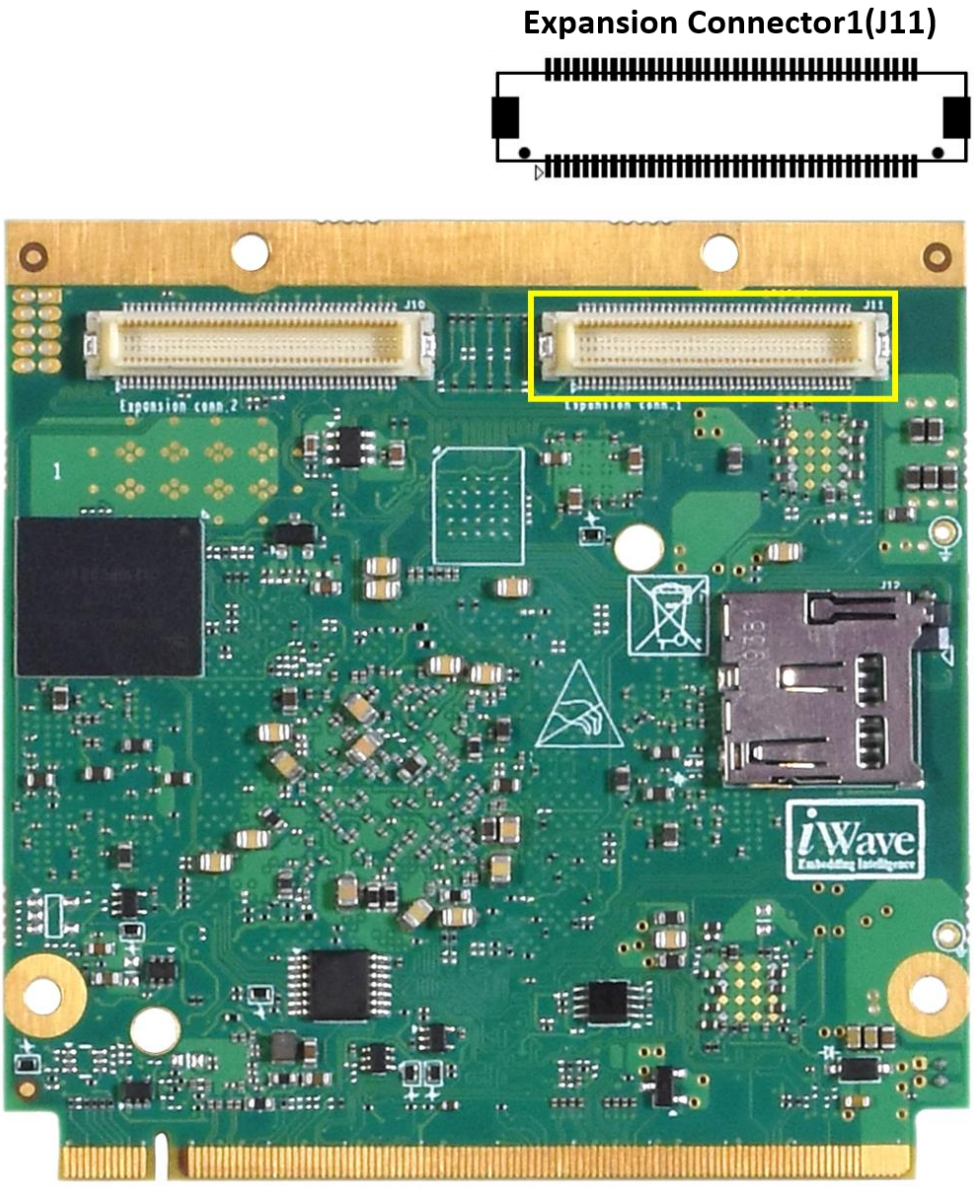


Figure 8: SOM Expansion Connector1

Number of Pins - : 80

Connector Part - : DF17(2.0)-80DP-0.5V(57) from Hirose

Mating Connector - : DF17(3.0)-80DS-0.5V(57) from Hirose

Note: In default configuration Expansion connector is optional, contact iWave Support Team for further information.

Table 6: SOM Expansion Connector1 Pinouts

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
MIPI_DSI0_CLK_P	**1**	**2**	MIPI_DSI1_CLK_P
MIPI_DSI0_CLK_N	**3**	**4**	MIPI_DSI1_CLK_N
GND	**5**	**6**	GND
MIPI_DSI0_DATA0_P	**7**	**8**	MIPI_DSI1_DATA0_P
MIPI_DSI0_DATA0_N	**9**	**10**	MIPI_DSI1_DATA0_N
GND	**11**	**12**	GND
MIPI_DSI0_DATA1_P	**13**	**14**	MIPI_DSI1_DATA1_P
MIPI_DSI0_DATA1_N	**15**	**16**	MIPI_DSI1_DATA1_N
GND	**17**	**18**	GND
MIPI_DSI0_DATA2_P	**19**	**20**	MIPI_DSI1_DATA2_P
MIPI_DSI0_DATA2_N	**21**	**22**	MIPI_DSI1_DATA2_N
GND	**23**	**24**	GND
MIPI_DSI0_DATA3_P	**25**	**26**	MIPI_DSI1_DATA3_P
MIPI_DSI0_DATA3_N	**27**	**28**	MIPI_DSI1_DATA3_N
GND	**29**	**30**	GND
HDMI_RX0_CLK_N	**31**	**32**	MIPI_DSI0_I2C_SDA
HDMI_RX0_CLK_P	**33**	**34**	MIPI_DSI0_I2C_SCL
GND	**35**	**36**	FLEXCAN1_RX
HDMI_RX0_ARC_N	**37**	**38**	FLEXCAN1_TX
HDMI_RX0_ARC_P	**39**	**40**	FLEXCAN2_RX
GND	**41**	**42**	FLEXCAN2_TX
HDMI_RX0_DATA0_N	**43**	**44**	GND
HDMI_RX0_DATA0_P	**45**	**46**	HDMI_RX0_CEC
GND	**47**	**48**	HDMI_RX_HPD
HDMI_RX0_DATA1_N	**49**	**50**	HDMI_RX0_DDC_SDA
HDMI_RX0_DATA1_P	**51**	**52**	HDMI_RX0_DDC_SCL
GND	**53**	**54**	VHDMI_RX_5V
HDMI_RX0_DATA2_N	**55**	**56**	GND
HDMI_RX0_DATA2_P	**57**	**58**	ADC_IN4(GPIO3_22) *(Note: Optionally UART3_RX)*
GND	**59**	**60**	ADC_IN5(GPIO3_23) *(Note: Optionally UART3_TX)*
ENET1_RGMII_TXC	**61**	**62**	VDD_ENET1 *(Note: LCD0_BL_PWM(GPIO1_04))*
ENET1_RGMII_TX_CTL	**63**	**64**	MIPI_DSI1_I2C_SCL(GPIO1_20)
ENET1_RGMII_TXD0	**65**	**66**	MIPI_DSI1_I2C_SDA(GPIO1_21)
ENET1_RGMII_TXD1	**67**	**68**	GND
ENET1_RGMII_TXD2	**69**	**70**	ENET1_RGMII_RXC
ENET1_RGMII_TXD3	**71**	**72**	ENET1_RGMII_RX_CTL
GND	**73**	**74**	ENET1_RGMII_RXD0

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
ENET1_REFCLK_125M_25M	**75**	**76**	ENET1_RGMII_RXD1
ENET1_MDIO	**77**	**78**	ENET1_RGMII_RXD2
ENET1_MDC	**79**	**80**	ENET1_RGMII_RXD3

2.11.1 MIPI-DSI Interface (Optional)

i.MX 8 QM/QP Qseven SOM supports two display interfaces over Expansion1. The i.MX 8 SoCs' MIPI_DSI standard controller is a flexible, high-performance, and easy-to-use digital core that implements all protocol functions defined in the MIPI DSI Specification. The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The MIPI DSI D-PHY is a high frequency, low power, low-cost, source-synchronous, physical layer supporting the MIPI Alliance standard for D-PHY.

For more details on Expansion Connector MIPI_DSI pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
MIPI_DSI0				
1	MIPI_DSI0_CLK_P	MIPI_DSI0_CLK_P/BL27	O, MIPI	MIPI_DSI0 Clock positive.
3	MIPI_DSI0_CLK_N	MIPI_DSI0_CLK_N/BN27	O, MIPI	MIPI_DSI0 Clock negative.
7	MIPI_DSI0_DATA0_P	MIPI_DSI0_DATA0_P/BK28	O, MIPI	MIPI_DSI0 Transmit Lane0 positive.
9	MIPI_DSI0_DATA0_N	MIPI_DSI0_DATA0_N/BM28	O, MIPI	MIPI_DSI0 Transmit Lane0 negative.
13	MIPI_DSI0_DATA1_P	MIPI_DSI0_DATA1_P/BK26	O, MIPI	MIPI_DSI0 Transmit Lane1 positive.
15	MIPI_DSI0_DATA1_N	MIPI_DSI0_DATA1_N/BM26	O, MIPI	MIPI_DSI0 Transmit Lane1 negative.
19	MIPI_DSI0_DATA2_P	MIPI_DSI0_DATA2_P/BL29	O, MIPI	MIPI_DSI0 Transmit Lane2 positive.
21	MIPI_DSI0_DATA2_N	MIPI_DSI0_DATA2_N/BN29	O, MIPI	MIPI_DSI0 Transmit Lane2 negative.
25	MIPI_DSI0_DATA3_P	MIPI_DSI0_DATA3_P/BL25	O, MIPI	MIPI_DSI0 Transmit Lane3 positive.
27	MIPI_DSI0_DATA3_N	MIPI_DSI0_DATA3_N/BN25	O, MIPI	MIPI_DSI0 Transmit Lane3 negative.
MIPI_DSI1				
2	MIPI_DSI1_CLK_P	MIPI_DSI1_CLK_P/BG31	O, MIPI	MIPI_DSI1 Clock positive.
4	MIPI_DSI1_CLK_N	MIPI_DSI1_CLK_N/BH30	O, MIPI	MIPI_DSI1 Clock negative.
8	MIPI_DSI1_DATA0_P	MIPI_DSI1_DATA0_P/BG33	O, MIPI	MIPI_DSI1 Transmit Lane0 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
10	MIPI_DSI1_DATA0_N	MIPI_DSI1_DATA0_N/BH32	O, MIPI	MIPI_DSI1 Transmit Lane0 negative.
14	MIPI_DSI1_DATA1_P	MIPI_DSI1_DATA1_P/BG29	O, MIPI	MIPI_DSI1 Transmit Lane1 positive.
16	MIPI_DSI1_DATA1_N	MIPI_DSI1_DATA1_N/BH28	O, MIPI	MIPI_DSI1 Transmit Lane1 negative.
20	MIPI_DSI1_DATA2_P	MIPI_DSI1_DATA2_P/BG35	O, MIPI	MIPI_DSI1 Transmit Lane2 positive.
22	MIPI_DSI1_DATA2_N	MIPI_DSI1_DATA2_N/BH34	O, MIPI	MIPI_DSI1 Transmit Lane2 negative.
26	MIPI_DSI1_DATA3_P	MIPI_DSI1_DATA3_P/BG27	O, MIPI	MIPI_DSI1 Transmit Lane3 positive.
28	MIPI_DSI1_DATA3_N	MIPI_DSI1_DATA3_N/BH26	O, MIPI	MIPI_DSI1 Transmit Lane3 negative.
MIPI_DSI I2C				
32	MIPI_DSI0_I2C_SDA	MIPI_DSI0_I2C0_SDA/BE31	IO, 3.3V OD/ 2.2K PU	MIPI_DSI0 Serial Data.
34	MIPI_DSI0_I2C_SCL	MIPI_DSI0_I2C0_SCL/BE29	O, 3.3V OD/ 2.2K PU	MIPI_DSI0 Serial clock.
64	MIPI_DSI1_I2C_SCL	MIPI_DSI1_I2C0_SCL/BE27	O, 3.3V OD/ 2.2K PU	MIPI_DSI1 Serial clock.
66	MIPI_DSI1_I2C_SDA	MIPI_DSI1_I2C0_SDA/BG25	IO, 3.3V OD/ 2.2K PU	MIPI_DSI1 Serial Data.

2.11.2 HDMI Receiver (Optional)

The i.MX 8 Processor supports HDMI-RX HDMI 2.0a with HDCP 2.2 and 1.4. In SOM, since Qseven Edge connector support only HDMI TX interface HDMI RX interface is supported via board expansion connector. The HDMI_RX Controller Supports up to 4K2K at 60Hz resolution and Compliant with HDCP2.2 (and backward compatible with HDCP1.4) with up to 600Mhz pixel clock and supports up to 8 (Status and Control Data Channel) SCDC slave addresses.

Note: Currently HDMI Receiver is not supported by NXP.

For more details on Expansion Connector HDMI RX pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
31	HDMI_RX0_CLK_N	HDMI_RX0_CLK_N/BL11	I, HDMI	HDMI RX0 differential Clock negative.
33	HDMI_RX0_CLK_P	HDMI_RX0_CLK_P/BM12	I, HDMI	HDMI RX0 differential Clock positive.
37	HDMI_RX0_ARC_N	HDMI_RX0_ARC_N/BL13	I, HDMI	HDMI RX0 differential Audio Return Channel negative.
39	HDMI_RX0_ARC_P	HDMI_RX0_ARC_P/BM14	I, HDMI/ 0.1uF AC Couple	HDMI RX0 differential Audio Return Channel positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
43	HDMI_RX0_DATA0_N	HDMI_RX0_DATA0_N/BL15	I, HDMI	HDMI RX0 differential data lane 0 negative.
45	HDMI_RX0_DATA0_P	HDMI_RX0_DATA0_P/BM16	I, HDMI	HDMI RX0 differential data lane 0 positive.
49	HDMI_RX0_DATA1_N	HDMI_RX0_DATA1_N/BL17	I, HDMI	HDMI RX0 differential data lane 1 negative.
51	HDMI_RX0_DATA1_P	HDMI_RX0_DATA1_P/BM18	I, HDMI	HDMI RX0 differential data lane 1 positive.
55	HDMI_RX0_DATA2_N	HDMI_RX0_DATA2_N/BL19	I, HDMI	HDMI RX0 differential data lane 2 negative.
57	HDMI_RX0_DATA2_P	HDMI_RX0_DATA2_P/BM20	I, HDMI	HDMI RX0 differential data lane 2 positive.
54	VHDMI_RX_5V	HDMI_RX0_MON_5V/BN11	Power	VHDMI_RX_5V.
46	HDMI_RX0_CEC	HDMI_RX0_CEC/BJ9	IO, 3.3V CMOS	HDMI Consumer Electronics Control.
48	HDMI_RX_HPD	HDMI_RX_HPD/BF14	O, 5V CMOS	HDMI RX0 Hot Plug Detect.
50	HDMI_RX0_DDC_SDA	HDMI_RX0_DDC_SDA/BE13	IO, 5V CMOS/ 2.2K PU	HDMI RX0 I2C Data.
52	HDMI_RX0_DDC_SCL	HDMI_RX0_DDC_SCL/BH10	I, 5V CMOS/ 2.2K PU	HDMI RX0 I2C Clock.

2.11.3 CAN Interface (Optional)

The Flexible Controller Area Network (FLEXCAN) module is a communication controller implementing the CAN protocol according to the CAN 2.0B protocol specification. CAN0 of SoC is connected to Qseven edge connector. CAN1 and CAN2 are connected to Expansion Connector1.

For more details on Expansion Connector CAN pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
36	FLEXCAN1_RX	FLEXCAN1_RX/ E5	I, 3.3V CMOS	CAN1 Receiver.
38	FLEXCAN1_TX	FLEXCAN1_TX/ G7	O, 3.3V CMOS	CAN1 Transmitter.
40	FLEXCAN2_RX	FLEXCAN2_RX/ C3	I, 3.3V CMOS	CAN2 Receiver.
42	FLEXCAN2_TX	FLEXCAN2_TX/ E7	O, 3.3V CMOS	CAN2 Transmitter.

2.11.4 ETH1 Interface (Optional)

Since Qseven Edge connector support only one ethernet, ENET0 of i.MX 8 is connected to GBE port of Qseven edge connector. ENET1 of i.MX 8 interface is supported via board expansion connector. Since for ENET1 only MAC is supported on SOM, PHY is required on the carrier board.

For more details on Expansion Connector ETH1 pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
61	ENET1_RGMII_TXC	ENET1_RGMII_TXC/D46	O, 3.3V CMOS/ 33E Series	ENET1 transmit clock.
63	ENET1_RGMII_TX_CTL	ENET1_RGMII_TX_CTL/B48	O, 3.3V CMOS/ 33E Series	ENET1 data Control line.
65	ENET1_RGMII_TXD0	ENET1_RGMII_TXD0/A49	O, 3.3V CMOS/ 33E Series	ENET1 transmit data0.
67	ENET1_RGMII_TXD1	ENET1_RGMII_TXD1/C47	O, 3.3V CMOS/ 33E Series	ENET1 transmit data1.
69	ENET1_RGMII_TXD2	ENET1_RGMII_TXD2/G47	O, 3.3V CMOS/ 33E Series	ENET1 transmit data2.
71	ENET1_RGMII_TXD3	ENET1_RGMII_TXD3/D48	O, 3.3V CMOS/ 33E Series	ENET1 transmit data3.
70	ENET1_RGMII_RXC	ENET1_RGMII_RXC/B50	I, 3.3V CMOS	ENET1 receive clock.
72	ENET1_RGMII_RX_CTL	ENET1_RGMII_RX_CTL/E49	I, 3.3V CMOS	ENET1 receive Control line.
74	ENET1_RGMII_RXD0	ENET1_RGMII_RXD0/E51	I, 3.3V CMOS	ENET1 receive data0.
76	ENET1_RGMII_RXD1	ENET1_RGMII_RXD1/C51	I, 3.3V CMOS	ENET1 receive data1.
78	ENET1_RGMII_RXD2	ENET1_RGMII_RXD2/D52	I, 3.3V CMOS	ENET1 receive data2.
80	ENET1_RGMII_RXD3	ENET1_RGMII_RXD3/E53	I, 3.3V CMOS	ENET1 receive data3.
75	ENET1_REFCLK_125M_25M	ENET1_REFCLK_125M_25M/A11	I, 3.3V CMOS	Synchronous Ethernet reference clock.
77	ENET1_MDIO	ENET1_MDIO/C13	IO, 3.3V CMOS	Management data.
79	ENET1_MDC	ENET1_MDC/A13	O, 3.3V CMOS	Management data clock.

2.11.5 GPIO (Optional)

Refer GPIO Column under **"i.MX 8 Pin Multiplexing on Expansion Connector"** for details on GPIO options available from Expansion connector.

2.12 SOM Expansion Connector2 (Optional)

The i.MX 8 Qseven SOM supports an 80pin Expansion connector2 (J10) as a optional feature to utilise extra interfaces which is not covered under Qseven specification V2.1 edge connector. The SOM Expansion connector is placed on the bottom side of the SOM.

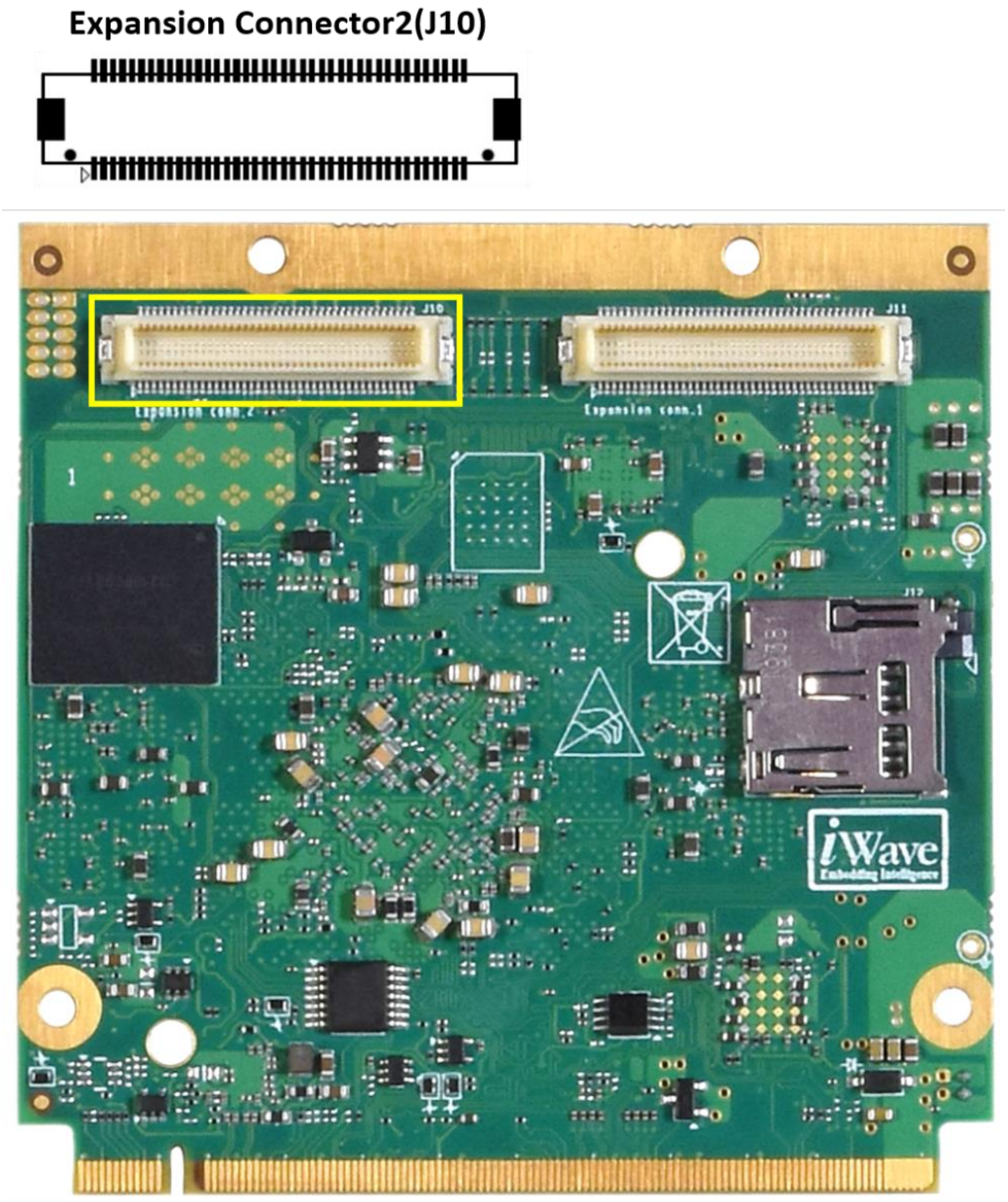


Figure 9: Expansion Connector2

Number of Pins - : 80

Connector Part - : DF17(2.0)-80DP-0.5V(57) from Hirose

Mating Connector - : DF17(3.0)-80DS-0.5V(57) from Hirose

Note: In default configuration Expansion connector is optional, contact iWave Support Team for further information.

Table 7: SOM Expansion Connector2 Pinouts

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
LVDS0_CH1_CLK_N	**1**	**2**	LVDS0_CH0_CLK_P
LVDS0_CH1_CLK_P	**3**	**4**	LVDS0_CH0_CLK_N
GND	**5**	**6**	GND
LVDS0_CH1_TX0_P	**7**	**8**	LVDS0_CH0_TX0_P
LVDS0_CH1_TX0_N	**9**	**10**	LVDS0_CH0_TX0_N
GND	**11**	**12**	GND
LVDS0_CH1_TX1_N	**13**	**14**	LVDS0_CH0_TX1_P
LVDS0_CH1_TX1_P	**15**	**16**	LVDS0_CH0_TX1_N
GND	**17**	**18**	GND
LVDS0_CH1_TX2_N	**19**	**20**	LVDS0_CH0_TX2_P
LVDS0_CH1_TX2_P	**21**	**22**	LVDS0_CH0_TX2_N
GND	**23**	**24**	GND
LVDS0_CH1_TX3_N	**25**	**26**	LVDS0_CH0_TX3_P
LVDS0_CH1_TX3_P	**27**	**28**	LVDS0_CH0_TX3_N
GND	**29**	**30**	GND
LVDS0_I2C0_SDA	**31**	**32**	SNVS_TAMPER_OUT0
LVDS0_I2C0_SCL	**33**	**34**	SNVS_TAMPER_IN0
SPDIF_RX	**35**	**36**	SNVS_TAMPER_IN1
SPDIF_ETX_CLK *(Note: Optionally USB_HUB4_OC)*	**37**	**38**	SNVS_TAMPER_OUT1
SPDIF_TX *(Note: Optionally VDD_SNVS)*	**39**	**40**	GND
MLB_DATA	**41**	**42**	MLB_DATA_P
MLB_CLK	**43**	**44**	MLB_DATA_N
MLB_SIG	**45**	**46**	GND
ESAI1_SCKR	**47**	**48**	MLB_CLK_P
ESAI1_FSR	**49**	**50**	MLB_CLK_N
ESAI1_TX0	**51**	**52**	GND
ESAI1_TX2_RX3	**53**	**54**	MLB_SIG_P
ESAI1_TX3_RX2	**55**	**56**	MLB_SIG_N
ESAI1_TX4_RX1	**57**	**58**	GND
ESAI1_TX5_RX0	**59**	**60**	GND
GND	**61**	**62**	SPI2_SCLK
QSPI1A_SCLK	**63**	**64**	SPI2_CS0
QSPI1A_SS0	**65**	**66**	SPI2_MISO
QSPI1A_DATA0	**67**	**68**	SPI2_MOSI
QSPI1A_DATA1	**69**	**70**	GND
QSPI1A_DATA2	**71**	**72**	USB3_HUB4_RXP
QSPI1A_DATA3	**73**	**74**	USB3_HUB4_RXM
GND	**75**	**76**	GND

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
USB_HUB4OUT_DP	**77**	**78**	USB3_HUB4_TXP
USB_HUB4OUT_DM	**79**	**80**	USB3_HUB4_TXM

2.12.1 LVDS Interface (Optional)

The i.MX 8 Processor's two four lane LVDS channels from LVDS0 interface are connected to Board Expansion connector. Processor has LVDS Display Bridge (LDB) connects to an External LVDS Display Interface. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

For more details on Expansion Connector2 LVDS pinouts, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
LVDS0 Channel0				
2	LVDS0_CH0_CLK_P	LVDS0_CH0_CLK_P/ BN41	O, LVDS	LVDS0 Channel0 Clock positive.
4	LVDS0_CH0_CLK_N	LVDS0_CH0_CLK_N/ BL41	O, LVDS	LVDS0 Channel0 Clock negative.
8	LVDS0_CH0_TX0_P	LVDS0_CH0_TX0_P/ BM42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 positive.
10	LVDS0_CH0_TX0_N	LVDS0_CH0_TX0_N/ BK42	O, LVDS	LVDS0 Channel0 Transmit Lane 0 negative.
14	LVDS0_CH0_TX1_P	LVDS0_CH0_TX1_P/ BN43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 positive.
16	LVDS0_CH0_TX1_N	LVDS0_CH0_TX1_N/ BL43	O, LVDS	LVDS0 Channel0 Transmit Lane 1 negative.
20	LVDS0_CH0_TX2_P	LVDS0_CH0_TX2_P/ BM44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 positive.
22	LVDS0_CH0_TX2_N	LVDS0_CH0_TX2_N/ BK44	O, LVDS	LVDS0 Channel0 Transmit Lane 2 negative.
26	LVDS0_CH0_TX3_P	LVDS0_CH0_TX3_P/ BN45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 positive.
28	LVDS0_CH0_TX3_N	LVDS0_CH0_TX3_N/ BL45	O, LVDS	LVDS0 Channel0 Transmit Lane 3 negative.
LVDS0 Channel1				
1	LVDS0_CH1_CLK_N	LVDS0_CH1_CLK_N/ BG45	O, LVDS	LVDS0 Channel1 Clock negative.
3	LVDS0_CH1_CLK_P	LVDS0_CH1_CLK_P/ BH46	O, LVDS	LVDS0 Channel1 Clock positive.
9	LVDS0_CH1_TX0_N	LVDS0_CH1_TX0_N/ BG43	O, LVDS	LVDS0 Channel1 Transmit Lane 0 negative.
7	LVDS0_CH1_TX0_P	LVDS0_CH1_TX0_P/ BH44	O, LVDS	LVDS0 Channel1 Transmit Lane 0 positive.
13	LVDS0_CH1_TX1_N	LVDS0_CH1_TX1_N/ BG41	O, LVDS	LVDS0 Channel1 Transmit Lane 1 negative.
15	LVDS0_CH1_TX1_P	LVDS1_CH1_TX1_P/ BH42	O, LVDS	LVDS0 Channel1 Transmit Lane 1 positive.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
19	LVDS0_CH1_TX2_N	LVDS0_CH1_TX2_N/ BG39	O, LVDS	LVDS0 Channel1 Transmit Lane 2 negative.
21	LVDS0_CH1_TX2_P	LVDS0_CH1_TX2_P/ BH40	O, LVDS	LVDS0 Channel1 Transmit Lane 2 positive.
25	LVDS0_CH1_TX3_N	LVDS0_CH1_TX3_N/ BG37	O, LVDS	LVDS0 Channel1 Transmit Lane 3 negative.
27	LVDS0_CH1_TX3_P	LVDS0_CH1_TX3_P/ BH38	O, LVDS	LVDS0 Channel1 Transmit Lane 3 positive.
LVDS0 I2C				
31	LVDS0_I2C0_SDA	LVDS0_I2C0_SDA/BD36	IO, 3.3V CMOS/ 2.2K PU	LVDS0 Serial Data.
33	LVDS0_I2C0_SCL	LVDS0_I2C0_SCL/BD38	O, 3.3V CMOS/ 2.2K PU	LVDS0 Serial Clock.

2.12.2 SPDIF Interface (Optional)

The Sony/Philips Digital Interface (SPDIF) audio block is a stereo transceiver that allows the processor to receive and transmit digital audio. The SPDIF is composed of two parts: SPDIF Receiver and SPDIF Transmitter.

The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs. The Channel Status and User Bits are also extracted from each frame and placed in the corresponding registers. The SPDIF receiver also provides a bypass option for direct transfer of the SPDIF input signal to the SPDIF transmitter.

For the SPDIF transmitter, the audio data is provided by the processor via the SPDIF Tx Left and SPDIF Tx Right registers. The Channel Status bits are also provided via the corresponding registers. The SPDIF transmitter generates a SPDIF output bitstream in the bi-phase mark format (IEC60958), which consists of audio data, channel status and user bits.

For more details on SPDIF Expansion Connector2 pinout, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
37	SPDIF_ETX_CLK	SPDIF_ETX_CLK/ BD6	O, 3.3V CMOS	Sony/Philips Digital Interface Clock. *Note: Optionally connected to USB_HUB4_OC*
39	SPDIF_TX	SPDIF_TX/BC9	O, 3.3V CMOS	Sony/Philips Digital Interface Transmit. *Note: Optionally connected to VDD_SNVS*
35	SPDIF_RX	SPDIF_RX/BC7	I, 3.3V CMOS	Sony/Philips Digital Interface Receive.

2.12.3 MLB Interface (Optional)

Media Local Bus Device functionality is implemented with an MediaLB 3-pin interface (single ended) or MediaLB 6-pin interface (differential), however only one interface can be active at a time. The MediaLB interfaces are capable of exchanging data at speeds up to 1024xFs in 3-pin mode or 6144xFs in 6-pin mode. Both MediaLB interfaces provide real-time access to all network data types including streaming, packet, control, and isochronous data.

For more details of MLB on Expansion Connector2, refer below table.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
42	MLB_DATA_P	MLB_DATA_P/ F34	IO, MLB	Media Local Bus DATA positive.
44	MLB_DATA_N	MLB_DATA_N/ E35	IO, MLB	Media Local Bus DATA negative.
48	MLB_CLK_P	MLB_CLK_P/ D32	O, MLB	Media Local Bus Clock positive.
50	MLB_CLK_N	MLB_CLK_N/ E33	O, MLB	Media Local Bus Clock negative.
54	MLB_SIG_P	MLB_SIG_P/ D30	O, MLB	Media Local Bus Signal positive.
56	MLB_SIG_N	MLB_SIG_N/ E31	O, MLB	Media Local Bus Signal negative.
41	MLB_DATA	MLB_DATA/ E3	IO, 1.8V CMOS	Media Local Bus Data.
43	MLB_CLK	MLB_CLK/ D2	O, 1.8V CMOS	Media Local Bus Clock.
45	MLB_SIG	MLB_SIG/E1	O, 1.8V CMOS	Media Local Bus Signal.

2.12.4 ESAI Interface (Optional)

The Enhanced Serial Audio Interface (ESAI) provides a full-duplex serial port for serial communication with a variety of serial devices, the ESAI consists of independent transmitter and receiver sections, each section with its own clock generator. ESAI has three basic operating modes and many data/operation formats. ESAI operating mode are selected by the ESAI control registers.

ESAI1 of i.MX 8 Processor is connected to board expansion connector2, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
47	ESAI1_SCKR	ESAI1_SCKR/ BD12	I, 3.3V CMOS	ESAI1 Clock Input.
49	ESAI1_FSR	ESAI1_FSR/ BE11	I, 3.3V CMOS	ESAI1 Frame Sync Input.
51	ESAI1_TX0	ESAI1_TX0/	O, 3.3V CMOS	ESAI1 Transmit 0.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
		BF10		
57	ESAI1_TX4_RX1	ESAI1_TX4_RX1/ AY12	IO, 3.3V CMOS	ESAI1 Transmit 4 or Receive 1.
55	ESAI1_TX3_RX2	ESAI1_TX3_RX2/ AV10	IO, 3.3V CMOS	ESAI1 Transmit 3 or Receive 2.
53	ESAI1_TX2_RX3	ESAI1_TX2_RX3/ AU11	IO, 3.3V CMOS	ESAI1 Transmit 2 or Receive 3.
59	ESAI1_TX5_RX0	ESAI1_TX5_RX0/ AT10	IO, 3.3V CMOS	ESAI1 Transmit 5 or Receive 0.

2.12.5 QSPI Interface (Optional)

QSPI1A of SoC interface is connected over Expansion Connector2 pins. QSPI1A maximum clock speed very from 60MHz to 200MHZ in different mode which can be supported over SPI pins by contacting iWave support team.

QSPI of i.MX 8 SoC is connected to board expansion connector2, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
63	QSPI1A_SCLK	QSPI1A_SCLK / F10	O, 1.8V CMOS/ 33E Series	QSPI Clock Output.
65	QSPI1A_SS0	QSPI1A_SS0_B/ J11	O, 1.8V CMOS	QSPI Chip select.
67	QSPI1A_DATA0	QSPI1A_DATA0/ D12	IO, 1.8V CMOS	QSPI Data 0.
69	QSPI1A_DATA1	QSPI1A_DATA1/ D14	IO, 1.8V CMOS	QSPI Data 1.
71	QSPI1A_DATA2	QSPI1A_DATA2/ E13	IO, 1.8V CMOS	QSPI Data 2.
73	QSPI1A_DATA3	QSPI1A_DATA3/ E11	IO, 1.8V CMOS	QSPI Data 3.

2.12.6 SPI Interface (Optional)

The i.MX 8 SoC supports low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave with maximum clock speed of 40MHz.

SPI of i.MX 8 SoC is connected to board Expansion Connector2, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
64	SPI2_CS0	SPI2_CS0/ AW1	O, 3.3V CMOS	SPI2 Chip Select 0.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
62	SPI2_SCLK	SPI2_SCK/ AW5	O, 1.8V CMOS/ 33E Series	SPI2 Clock
66	SPI2_MISO	SPI2_SDI/ AY4	I, 3.3V CMOS	SPI2 Master In Slave Out.
68	SPI2_MOSI	SPI2_SDO/ BA1	O, 3.3V CMOS	SPI2 Master Out Slave In

2.12.7 USB Interface (Optional)

On SOM USB3.0 hub USB5744-I/2G from Microchip Hub Feature Controller IC with 4 USB 3.1 Gen 1 / USB 2.0 downstream ports. The upstream ports are connected to Qseven Edge connector and Expansion connector.

For more details on USB expansion signals on expansion connector, refer below table:

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
78	USB3_HUB4_TXP	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Plus.
80	USB3_HUB4_TXM	NA	O, USB SS	USB3.0 Hub Transmit channel 4 Minus.
72	USB3_HUB4_RXP	NA	I, USB SS	USB3.0 Hub Receive channel 4 Plus.
74	USB3_HUB4_RXM	NA	I, USB SS	USB3.0 Hub Receive channel 4 Minus.
77	USB_HUB4OUT_DP	NA	I, USB HS	USB2.0 Hub Receive channel 1 Plus.
79	USB_HUB4OUT_DM	NA	I, USB HS	USB2.0 Hub Receive channel 1 Minus.

2.13 Other Features

2.13.1 Fan Header

The i.MX 8 Qseven SOM supports a Fan Header to connect cooling Fan if required. This Fan Header (J7) is physically located at the top of the board as shown below.

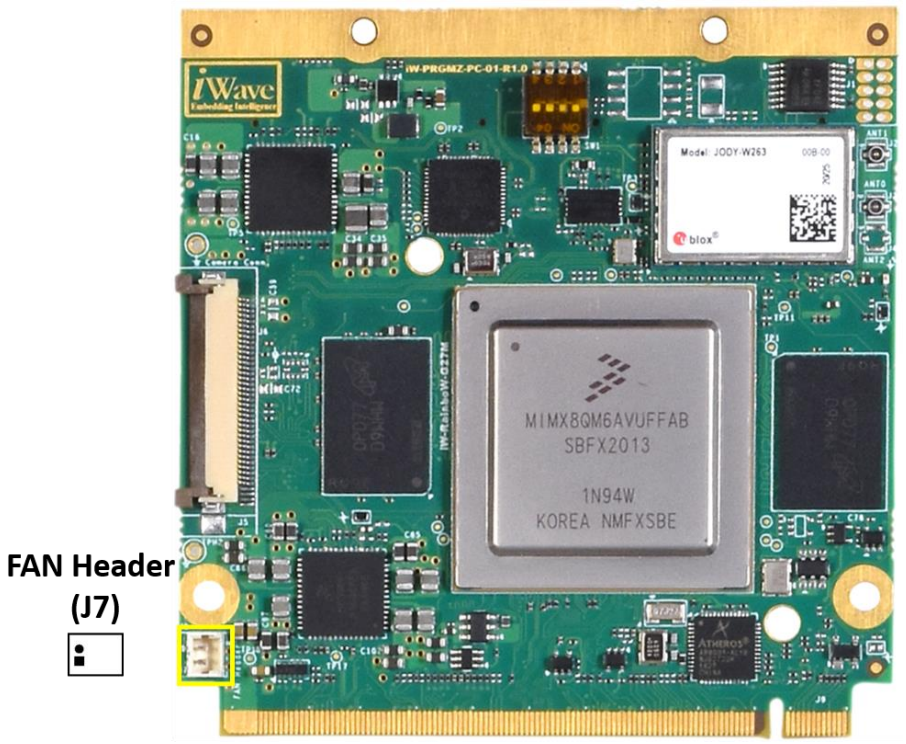


Figure 10: FAN Header

Number of Pins - 2

Connector Part - 10114829-10102LF from Amphenol ICC (FCI)

Mating Connector - 10114826-00002LF from Amphenol ICC (FCI)

Compatible FAN (Example) - MR3010H05B-RSR from Mechatronics Fan Group.

Table 8: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.13.2 UART Header (Optional)

The i.MX 8 SoC SCU_UART0, M4 Core1 & 2 UART and also UART4(Debug UART) can be taken out from J1 header, and using FTDI's UART to USB smart cable UART can be directly connected to Host PC for debugging.

Debug Header (J1) is physically located on topside of the SOM. This is the optional feature and will not be populated in default configuration.

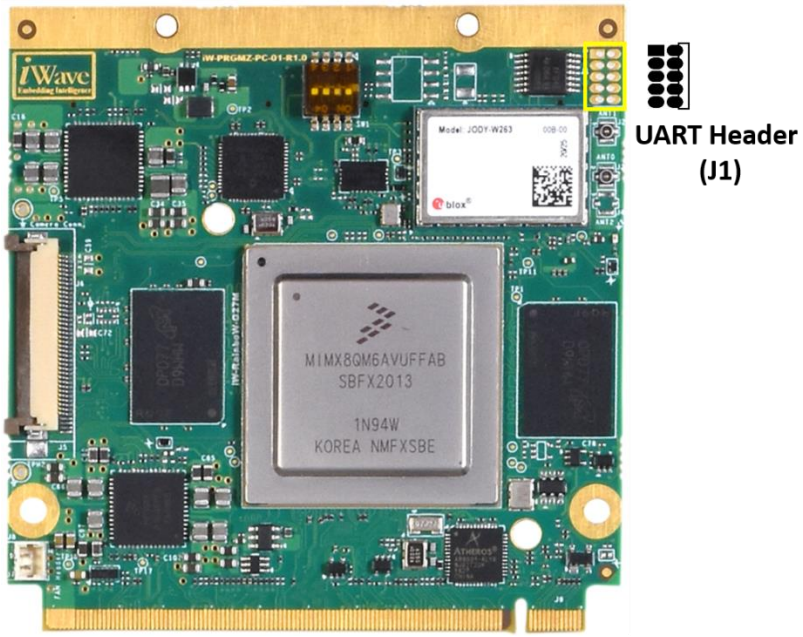


Figure 11: UART Header

Number of Pins - 10

Connector Part - GRPB052MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB052NFSP-RC from Sullins Connector Solutions

For more details on UART signals on J1 Header, refer below table:

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	M41_UART0_TX	M41_I2C0_SDA/ AU49	O, 3.3V CMOS	M4 Core 1 UART TX.
2	UART4_TX	DMA.UART4.TX/ AU53	O, 3.3V CMOS	Debug UART TX. *Note: Directly connected to 209th of Qseven edge.*
3	M41_UART0_RX	M41_I2C0_SCL/ AR45	I, 3.3V CMOS	M4 Core 1 UART RX.
4	UART4_RX	DMA.UART4.RX /AR47	I, 3.3V CMOS	Debug UART RX. *Note: Directly connected to 208th of Qseven edge.*
5	GND	NA	NA	NA
6	GND	NA	NA	NA

Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
7	M40_UART0_RX	M40_I2C0_SCL/ AM44	I, 3.3V CMOS	M4 Core 0 UART TX.
8	SCU_UART0_RX	SCU.UART0.RX/ AU43	I, 1.8V CMOS	System Control Unit UART RX.
9	M40_UART0_TX	M40_I2C0_SDA/ AU51	O, 3.3V CMOS	M4 Core 0 UART RX.
10	SCU_UART0_TX	SCU.UART0.TX/ AV44	O, 1.8V CMOS	System Control Unit UART TX.

2.14 i.MX 8 QM/QP Pin Multiplexing on Qseven Edge

The i.MX 8 QM/QP SoC IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement, also most of the i.MX 8 QM/QP SoC's IO pins can be configured as GPIO if required. The below table provides the details of i.MX 8 QM/QP SoC pin connections to the Qseven edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8 QM/QP Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the Qseven SOM Edge connector for iWave's BSP reusability.

Table 9: i.MX 8 QM/QP SoC IOMUX for Qseven Edge Connector interfaces

Interface/ Function	Qseven Edge Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
HDMI	133	BK2	HDMI_TX0.TX_M_LN_3					HDMI_TX0.TX_M_LN_3
	131	BL3	HDMI_TX0.TX_P_LN_3					HDMI_TX0.TX_P_LN_3
	143	BM4	HDMI_TX0.TX_M_LN_2					HDMI_TX0.TX_M_LN_2
	145	BL5	HDMI_TX0.TX_P_LN_2					HDMI_TX0.TX_P_LN_2
	139	BM6	HDMI_TX0.TX_M_LN_1					HDMI_TX0.TX_M_LN_1
	137	BL7	HDMI_TX0.TX_P_LN_1					HDMI_TX0.TX_P_LN_1
	151	BM8	HDMI_TX0.TX_M_LN_0					HDMI_TX0.TX_M_LN_0
	149	BL9	HDMI_TX0.TX_P_LN_0					HDMI_TX0.TX_P_LN_0
	153	BH8	HDMI_TX0.HPD					HDMI_TX0.HPD
	152	BG1	HDMI_TX0.DDC_SCL					HDMI_TX0.DDC_SCL
	150	BN5	HDMI_TX0.DDC_SDA					HDMI_TX0.DDC_SDA
LVDS1_CH 0	121	BK36	LVDS1_CH0_CLK_N					LVDS1_CH0_CLK_N
	119	BM36	LVDS1_CH0_CLK_P					LVDS1_CH0_CLK_P
	101	BL37	LVDS1_CH0_TX0_N					LVDS1_CH0_TX0_N
	99	BN37	LVDS1_CH0_TX0_P					LVDS1_CH0_TX0_P
	105	BK38	LVDS1_CH0_TX1_N					LVDS1_CH0_TX1_N
	103	BM38	LVDS1_CH0_TX1_P					LVDS1_CH0_TX1_P
	109	BL39	LVDS1_CH0_TX2_N					LVDS1_CH0_TX2_N
	107	BN39	LVDS1_CH0_TX2_P					LVDS1_CH0_TX2_P
	115	BK40	LVDS1_CH0_TX3_N					LVDS1_CH0_TX3_N
	113	BM40	LVDS1_CH0_TX3_P					LVDS1_CH0_TX3_P

Interface/ Function	Qseven Edge Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	127	BL35	LVDS1.I2C0.SCL	LVDS1.GPIO0.IO02		LSIO.GPIO1.IO12	GPIO1_12	LVDS1.I2C0.SCL
	125	BE33	LVDS1.I2C0.SDA	LVDS1.GPIO0.IO03		LSIO.GPIO1.IO13	GPIO1_13	LVDS1.I2C0.SDA
	111	BD32	LVDS1.I2C1.SCL	DMA.UART3.TX		LSIO.GPIO1.IO14	GPIO1_14	LSIO.GPIO1.IO14
	123	BD34	LVDS1.GPIO0.IO00	LVDS1.PWM0.OUT		LSIO.GPIO1.IO10	GPIO1_10	LVDS1.PWM0.OUT
	112	BE35	LVDS0.I2C1.SDA	DMA.UART2.RX		LSIO.GPIO1.IO09	GPIO1_09	LSIO.GPIO1.IO09
LVDS1_CH 1	122	BK34	LVDS1_CH1_CLK_N					LVDS1_CH1_CLK_N
	120	BM34	LVDS1_CH1_CLK_P					LVDS1_CH1_CLK_P
	102	BL33	LVDS1_CH1_TX0_N					LVDS1_CH1_TX0_N
	100	BN33	LVDS1_CH1_TX0_P					LVDS1_CH1_TX0_P
	106	BK32	LVDS1_CH1_TX1_N					LVDS1_CH1_TX1_N
	104	BM32	LVDS1_CH1_TX1_P					LVDS1_CH1_TX1_P
	110	BL31	LVDS1_CH1_TX2_N					LVDS1_CH1_TX2_N
	108	BN31	LVDS1_CH1_TX2_P					LVDS1_CH1_TX2_P
	116	BK30	LVDS1_CH1_TX3_N					LVDS1_CH1_TX3_N
	114	BM30	LVDS1_CH1_TX3_P					LVDS1_CH1_TX3_P
Carrier SD Interface	42	J39	CONN.USDHC1.CLK					CONN.USDHC1.CLK
	45	G41	CONN.USDHC1.CMD			LSIO.GPIO5.IO14	GPIO5_14	CONN.USDHC1.CMD
	49	E37	CONN.USDHC1.DATA0	CONN.NAND.RE_N		LSIO.GPIO5.IO15	GPIO5_15	CONN.USDHC1.DATA0
	48	F38	CONN.USDHC1.DATA1	CONN.NAND.RE_P		LSIO.GPIO5.IO16	GPIO5_16	CONN.USDHC1.DATA1
	51	E39	CONN.USDHC1.DATA2	CONN.NAND.DQS_N		LSIO.GPIO5.IO17	GPIO5_17	CONN.USDHC1.DATA2
	50	F40	CONN.USDHC1.DATA3	CONN.NAND.DQS_P		LSIO.GPIO5.IO18	GPIO5_18	CONN.USDHC1.DATA3
	47	BD28	MIPI_DSI0.GPIO0.IO01			LSIO.GPIO1.IO19	GPIO1_19	LSIO.GPIO1.IO19
	46	BM24	MIPI_DSI1.GPIO0.IO00	MIPI_DSI1.PWM0.OUT		LSIO.GPIO1.IO22	GPIO1_22	LSIO.GPIO1.IO22
	43	BK24	MIPI_DSI1.GPIO0.IO01			LSIO.GPIO1.IO23	GPIO1_23	LSIO.GPIO1.IO23
PCIe	179	B26	PCIE0_TX0_P					PCIE0_TX0_P
	151	C27	PCIE0_TX0_N					PCIE0_TX0_N
	180	A29	PCIE0_RX0_P					PCIE0_RX0_P
	182	B30	PCIE0_RX0_N					PCIE0_RX0_N
	173	B24	PCIE1_TX0_P					PCIE1_TX0_P
	175	C25	PCIE1_TX0_N					PCIE1_TX0_N
	174	A21	PCIE1_RX0_P					PCIE1_RX0_P
	176	B22	PCIE1_RX0_N					PCIE1_RX0_N

Interface/ Function	Qseven Edge Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	156	A15	HSIO.PCIE0.WAKE_B			LSIO.GPIO4.IO28	GPIO4_28	LSIO.GPIO4.IO28
	158	D20	HSIO.PCIE0.PERST_B			LSIO.GPIO4.IO29	GPIO4_29	LSIO.GPIO4.IO29
SATA	29	B16	PCIE_SATA0_TX0_P					PCIE_SATA0_TX0_P
	31	C17	PCIE_SATA0_TX0_N					PCIE_SATA0_TX0_N
	35	A19	PCIE_SATA0_RX0_P					PCIE_SATA0_RX0_P
	37	B20	PCIE_SATA0_RX0_N					PCIE_SATA0_RX0_N
	33	BD30	MIPI_DSI0.GPIO0.IO00	MIPI_DSI0.PWM0.OUT		LSIO.GPIO1.IO18	GPIO1_18	LSIO.GPIO1.IO18
SPI	203	BF6	DMA.SPI3.SCK			LSIO.GPIO2.IO17	GPIO2_17	DMA.SPI3.SCK
	201	BE5	DMA.SPI3.SDI	DMA.FTM.CH1		LSIO.GPIO2.IO19	GPIO2_19	DMA.SPI3.SDI
	199	BF2	DMA.SPI3.SDO	DMA.FTM.CH0		LSIO.GPIO2.IO18	GPIO2_18	DMA.SPI3.SDO
	200	BG5	DMA.SPI3.CS0	DMA.FTM.CH2		LSIO.GPIO2.IO20	GPIO2_20	DMA.SPI3.CS0
	202	BD8	DMA.SPI3.CS1			LSIO.GPIO2.IO21	GPIO2_21	DMA.SPI3.CS1
PWM	196	AW53	LSIO.GPT0.COMPARE	LSIO.PWM3.OUT	LSIO.KPP0.COL6	LSIO.GPIO0.IO16	GPIO0_16	LSIO.PWM3.OUT
	194	BA51	LSIO.GPT1.COMPARE	LSIO.PWM2.OUT	LSIO.KPP0.ROW5	LSIO.GPIO0.IO19	GPIO0_19	LSIO.PWM2.OUT
DMA_I2C 1	60	AY52	LSIO.GPT0.CLK	DMA.I2C1.SCL	LSIO.KPP0.COL4	LSIO.GPIO0.IO14	GPIO0_14	DMA.I2C1.SCL
	60	AV52	LSIO.GPT0.CAPTURE	DMA.I2C1.SDA	LSIO.KPP0.COL5	LSIO.GPIO0.IO15	GPIO0_15	DMA.I2C1.SDA
DMA_I2C 2	66	BA53	LSIO.GPT1.CLK	DMA.I2C2.SCL	LSIO.KPP0.COL7	LSIO.GPIO0.IO17	GPIO0_17	DMA.I2C2.SCL
	68	AY50	LSIO.GPT1.CAPTURE	DMA.I2C2.SDA	LSIO.KPP0.ROW4	LSIO.GPIO0.IO18	GPIO0_18	DMA.I2C2.SDA
UART0	177	AV50	DMA.UART0.RX			LSIO.GPIO0.IO20	GPIO0_20	DMA.UART0.RX
	171	AV48	DMA.UART0.TX			LSIO.GPIO0.IO21	GPIO0_21	DMA.UART0.TX
	172	AU45	DMA.UART0.RTS_B	LSIO.PWM0.OUT	DMA.UART2.RX	LSIO.GPIO0.IO22	GPIO0_22	DMA.UART0.RTS_B
	178	AW49	DMA.UART0.CTS_B	LSIO.PWM1.OUT	DMA.UART2.TX	LSIO.GPIO0.IO23	GPIO0_23	DMA.UART0.CTS_B
CAN	130	C5	DMA.FLEXCAN0.RX			LSIO.GPIO3.IO29	GPIO3_29	DMA.FLEXCAN0.RX
	129	H6	DMA.FLEXCAN0.TX			LSIO.GPIO3.IO30	GPIO3_30	DMA.FLEXCAN0.TX
UART4 (Debug)	209	AR47	M40.GPIO0.IO00	M40.TPM0.CH0	DMA.UART4.RX	LSIO.GPIO0.IO08	GPIO0_08	DMA.UART4.RX
	208	AU53	M40.GPIO0.IO01	M40.TPM0.CH1	DMA.UART4.TX	LSIO.GPIO0.IO09	GPIO0_09	DMA.UART4.TX
USB1 2.0 OTG	91	A39	CONN.USB_OTG1.VBUS					CONN.USB_OTG1.VBUS
	91	A37	CONN.USB_OTG1.ID					CONN.USB_OTG1.ID
	95	B40	CONN.USB_OTG1.DP					CONN.USB_OTG1.DP
	93	C39	CONN.USB_OTG1.DN					CONN.USB_OTG1.DN
	86	AL43	DMA.SIM0.PD	DMA.I2C3.SCL		LSIO.GPIO0.IO03	GPIO0_03	LSIO.GPIO0.IO03
	56	J9	DMA.I2C1.SCL	CONN.USB_OTG1.PWR		LSIO.GPIO4.IO03	GPIO4_03	CONN.USB_OTG1.PWR

Interface/ Function	Qseven Edge Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
SAI1 Audio	65	AV4	AUD.SAI1.RXD	AUD.SAI0.TXFS		LSIO.GPIO3.IO13	GPIO3_13	AUD.SAI1.RXD
	63	AU5	AUD.SAI1.TXC	AUD.SAI0.TXC		LSIO.GPIO3.IO15	GPIO3_15	AUD.SAI1.TXFS
	67	AU1	AUD.SAI1.TXD	AUD.SAI1.RXC		LSIO.GPIO3.IO16	GPIO3_16	AUD.SAI1.TXFS
	59	AV2	AUD.SAI1.TXFS	AUD.SAI1.RXFS		LSIO.GPIO3.IO17	GPIO3_17	AUD.SAI1.TXFS
	61	BD40	LVDS0.GPIO0.IO01			LSIO.GPIO1.IO05	GPIO1_05	LVDS0.GPIO0.IO01
JTAG	207	BC51	SCU.JTAG.TCK					SCU.JTAG.TCK
	210	BA49	SCU.JTAG.TMS					SCU.JTAG.TMS
	209	BD52	SCU.JTAG.TDO					SCU.JTAG.TDO
	208	BE51	SCU.JTAG.TDI					SCU.JTAG.TDI
GPIOs	185	AV6	AUD.SAI1.RXC	AUD.SAI0.TXD		LSIO.GPIO3.IO12	GPIO3_12	LSIO.GPIO3.IO12
	186	BB4	DMA.SPI0.SCK	AUD.SAI0.RXC		LSIO.GPIO3.IO02	GPIO3_02	LSIO.GPIO3.IO02
	187	AU3	AUD.SAI1.RXFS	AUD.SAI0.RXD		LSIO.GPIO3.IO14	GPIO3_14	LSIO.GPIO3.IO14
	188	AY2	DMA.SPI2.CS1	AUD.SAI0.TXFS		LSIO.GPIO3.IO11	GPIO3_11	LSIO.GPIO3.IO11
	189	BE37	LVDS0.I2C1.SCL	DMA.UART2.TX		LSIO.GPIO1.IO08	GPIO1_08	LSIO.GPIO1.IO08
	190	BH36	LVDS1.GPIO0.IO01			LSIO.GPIO1.IO11	GPIO1_11	LSIO.GPIO1.IO11
	191	G25	HSIO.PCIE1.PERST_B			LSIO.GPIO5.IO00	GPIO5_00	LSIO.GPIO5.IO00
	192	AL45	DMA.SIM0.CLK			LSIO.GPIO0.IO00	GPIO0_00	LSIO.GPIO0.IO00

2.15 i.MX 8 Pin Multiplexing on Expansion connector1

The below table provides the details of i.MX 8 SoC pin connections to the Expansion connector with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the Qseven SOM Edge connector for iWave's BSP reusability

Table 10: i.MX 8 Pin Multiplexing on Expansion Connector1 interfaces

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
MIPI DSI0	3	BN27	MIPI_DSI0.CKN					MIPI_DSI0.CKN
	1	BL27	MIPI_DSI0.CKP					MIPI_DSI0.CKP
	3	BM28	MIPI_DSI0.DN0					MIPI_DSI0.DN0
	7	BK28	MIPI_DSI0.DP0					MIPI_DSI0.DP0
	15	BM26	MIPI_DSI0.DN1					MIPI_DSI0.DN1
	13	BK26	MIPI_DSI0.DP1					MIPI_DSI0.DP1
	21	BN29	MIPI_DSI0.DN2					MIPI_DSI0.DN2
	19	BL29	MIPI_DSI0.DP2					MIPI_DSI0.DP2
	27	BN25	MIPI_DSI0.DN3					MIPI_DSI0.DN3
	25	BL25	MIPI_DSI0.DP3					MIPI_DSI0.DP3
MIPI DSI1	32	BE31	MIPI_DSI0.I2C0.SDA			LSIO.GPIO1.IO17	GPIO1_17	MIPI_DSI0.I2C0.SDA
	34	BE29	MIPI_DSI0.I2C0.SCL			LSIO.GPIO1.IO16	GPIO1_16	MIPI_DSI0.I2C0.SCL
	4	BH30	MIPI_DSI1.CKN					MIPI_DSI1.CKN
	2	BG31	MIPI_DSI1.CKP					MIPI_DSI1.CKP
	10	BH32	MIPI_DSI1.DN0					MIPI_DSI1.DN0
	8	BG33	MIPI_DSI1.DP0					MIPI_DSI1.DP0
	16	BH28	MIPI_DSI1.DN1					MIPI_DSI1.DN1
	14	BG29	MIPI_DSI1.DP1					MIPI_DSI1.DP1
	22	BH34	MIPI_DSI1.DN2					MIPI_DSI1.DN2
	20	BG35	MIPI_DSI1.DP2					MIPI_DSI1.DP2
HDMI RX	28	BH26	MIPI_DSI1.DN3					MIPI_DSI1.DN3
	26	BG27	MIPI_DSI1.DP3					MIPI_DSI1.DP3
	46	BJ9	HDMI_RX0_CEC					HDMI_RX0_CEC
	31	BL11	HDMI_RX0_CLK_N					HDMI_RX0_CLK_N
	33	BM12	HDMI_RX0_CLK_P					HDMI_RX0_CLK_P
	43	BL15	HDMI_RX0_DATA0_N					HDMI_RX0_DATA0_N

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	45	BM16	HDMI_RX0_DATA0_P					HDMI_RX0_DATA0_P
	49	BL17	HDMI_RX0_DATA1_N					HDMI_RX0_DATA1_N
	51	BM18	HDMI_RX0_DATA1_P					HDMI_RX0_DATA1_P
	55	BL19	HDMI_RX0_DATA2_N					HDMI_RX0_DATA2_N
	57	BM20	HDMI_RX0_DATA2_P					HDMI_RX0_DATA2_P
	37	BL13	HDMI_RX0_ARC_N					HDMI_RX0_ARC_N
	39	BM14	HDMI_RX0_ARC_P					HDMI_RX0_ARC_P
	48	BF14	HDMI_RX0_HPD					HDMI_RX0_HPD
	50	BE13	HDMI_RX0_DDC_SDA					HDMI_RX0_DDC_SDA
	50	BH10	HDMI_RX0_DDC_SCL					HDMI_RX0_DDC_SCL
	54	BN11	HDMI_RX0_MON_5V					HDMI_RX0_MON_5V
CAN	36	E5	DMA.FLEXCAN1.RX			LSIO.GPIO3.IO31	GPIO3_31	DMA.FLEXCAN1.RX
	38	G7	DMA.FLEXCAN1.TX			LSIO.GPIO4.IO00	GPIO4_00	DMA.FLEXCAN1.TX
	40	C3	DMA.FLEXCAN2.RX			LSIO.GPIO4.IO01	GPIO4_01	DMA.FLEXCAN2.RX
	42	E7	DMA.FLEXCAN2.TX			LSIO.GPIO4.IO02	GPIO4_02	DMA.FLEXCAN2.TX
ENET1	61	D46	CONN.ENET1.RGMII_TXC	CONN.ENET1.RCLK50M_OUT	CONN.ENET1.RCLK50M_IN	LSIO.GPIO6.IO10	GPIO6_10	CONN.ENET1.RGMII_TXC
	63	B48	CONN.ENET1.RGMII_TX_CTL			LSIO.GPIO6.IO11	GPIO6_11	CONN.ENET1.RGMII_TX_CTL
	65	A49	CONN.ENET1.RGMII_TXD0			LSIO.GPIO6.IO12	GPIO6_12	CONN.ENET1.RGMII_TXD0
	67	C47	CONN.ENET1.RGMII_TXD1			LSIO.GPIO6.IO13	GPIO6_13	CONN.ENET1.RGMII_TXD1
	69	G47	CONN.ENET1.RGMII_TXD2	DMA.UART3.TX	VPU.TSI_S1.VID	LSIO.GPIO6.IO14	GPIO6_14	CONN.ENET1.RGMII_TXD2
	71	D48	CONN.ENET1.RGMII_TXD3	DMA.UART3.RTS_B	VPU.TSI_S1.SYNC	LSIO.GPIO6.IO15	GPIO6_15	CONN.ENET1.RGMII_TXD3
	70	B50	CONN.ENET1.RGMII_RXC	DMA.UART3.CTS_B	VPU.TSI_S1.DATA	LSIO.GPIO6.IO16	GPIO6_16	CONN.ENET1.RGMII_RXC
	72	E49	CONN.ENET1.RGMII_RX_CTL		VPU.TSI_S0.VID	LSIO.GPIO6.IO17	GPIO6_17	CONN.ENET1.RGMII_RX_CTL
	74	E51	CONN.ENET1.RGMII_RXD0		VPU.TSI_S0.SYNC	LSIO.GPIO6.IO18	GPIO6_18	CONN.ENET1.RGMII_RXD0
	76	C51	CONN.ENET1.RGMII_RXD1		VPU.TSI_S0.DATA	LSIO.GPIO6.IO19	GPIO6_19	CONN.ENET1.RGMII_RXD1

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	78	D52	CONN.ENET1.RGMII_RXD2	CONN.ENET1.RMII_RX_ER	VPU.TSI_S0.CLK	LSIO.GPIO6.IO20	GPIO6_20	CONN.ENET1.RGMII_RXD2
	80	E53	CONN.ENET1.RGMII_RXD3	DMA.UART3.RX	VPU.TSI_S1.CLK	LSIO.GPIO6.IO21	GPIO6_21	CONN.ENET1.RGMII_RXD3
	75	A11	CONN.ENET1.REFCLK_125M_25M	CONN.ENET1.PPS		LSIO.GPIO4.IO16	GPIO4_16	CONN.ENET1.REFCLK_125M_25M
	77	C13	CONN.ENET1.MDIO	DMA.I2C4.SDA		LSIO.GPIO4.IO17	GPIO4_17	CONN.ENET1.MDIO
	79	A13	CONN.ENET1.MDC	DMA.I2C4.SCL		LSIO.GPIO4.IO18	GPIO4_18	CONN.ENET1.MDC
ADC/UART	58	AN9	DMA.ADC.IN4	DMA.SPI1.SDO	LSIO.KPP0.ROW0	LSIO.GPIO3.IO22	GPIO3_22	DMA.ADC.IN4
		AP44	M41.GPIO0.IO00	M41.TPM0.CH0	DMA.UART3.RX	LSIO.GPIO0.IO12	GPIO0_12	DMA.UART3.RX
	60	AR7	DMA.ADC.IN5	DMA.SPI1.SDI	LSIO.KPP0.ROW1	LSIO.GPIO3.IO23	GPIO3_23	DMA.ADC.IN5
		AU47	M41.GPIO0.IO01	M41.TPM0.CH1	DMA.UART3.TX	LSIO.GPIO0.IO13	GPIO0_13	DMA.UART3.TX
GPIO's	64	BE27	MIPI_DSI1.I2C0.SCL			LSIO.GPIO1.IO20	GPIO1_20	LSIO.GPIO1.IO20
	66	BG25	MIPI_DSI1.I2C0.SDA			LSIO.GPIO1.IO21	GPIO1_21	LSIO.GPIO1.IO21
PWM	62	BE39	LVDS0.GPIO0.IO00	LVDS0.PWM0.OUT		LSIO.GPIO1.IO04	GPIO1_04	LVDS0.PWM0.OUT

2.16 i.MX 8 Pin Multiplexing on Expansion connector2

The below table provides the details of i.MX 8 SoC pin connections to the Expansion connector with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX 8 Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the Qseven SOM Edge connector for iWave's BSP reusability

Table 11: i.MX 8 Pin Multiplexing on Expansion Connector2 interfaces

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
LVDS0 Channel0	4	BL41	LVDS0_CH0_CLK_N					LVDS0_CH0_CLK_N
	2	BN41	LVDS0_CH0_CLK_P					LVDS0_CH0_CLK_P
	10	BK42	LVDS0_CH0_TX0_N					LVDS0_CH0_TX0_N
	8	BM42	LVDS0_CH0_TX0_P					LVDS0_CH0_TX0_P

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	16	BL43	LVDS0_CH0_TX1_N					LVDS0_CH0_TX1_N
	14	BN43	LVDS0_CH0_TX1_P					LVDS0_CH0_TX1_P
	22	BK44	LVDS0_CH0_TX2_N					LVDS0_CH0_TX2_N
	20	BM44	LVDS0_CH0_TX2_P					LVDS0_CH0_TX2_P
	28	BL45	LVDS0_CH0_TX3_N					LVDS0_CH0_TX3_N
	26	BN45	LVDS0_CH0_TX3_P					LVDS0_CH0_TX3_P
	33	BD38	LVDS0.I2C0.SCL	LVDS0.GPIO0.IO02		LSIO.GPIO1.IO06	GPIO1_06	LVDS0.I2C0.SCL
	31	BD36	LVDS0.I2C0.SDA	LVDS0.GPIO0.IO03		LSIO.GPIO1.IO07	GPIO1_07	LVDS0.I2C0.SDA
LVDS0 Channel1	1	BG45	LVDS0_CH1_CLK_N					LVDS0_CH1_CLK_N
	3	BH46	LVDS0_CH1_CLK_P					LVDS0_CH1_CLK_P
	9	BG43	LVDS0_CH1_TX0_N					LVDS0_CH1_TX0_N
	7	BH44	LVDS0_CH1_TX0_P					LVDS0_CH1_TX0_P
	13	BG41	LVDS0_CH1_TX1_N					LVDS0_CH1_TX1_N
	15	BH42	LVDS0_CH1_TX1_P					LVDS0_CH1_TX1_P
	19	BG39	LVDS0_CH1_TX2_N					LVDS0_CH1_TX2_N
	21	BH40	LVDS0_CH1_TX2_P					LVDS0_CH1_TX2_P
	25	BG37	LVDS0_CH1_TX3_N					LVDS0_CH1_TX3_N
	27	BH38	LVDS0_CH1_TX3_P					LVDS0_CH1_TX3_P
SPDIF	35	BC7	AUD.SPDIF0.RX	AUD.MQS.R	AUD.ACM.MCLK_IN1	LSIO.GPIO2.IO14	GPIO2_14	AUD.SPDIF0.RX
	39	BC9	AUD.SPDIF0.TX	AUD.MQS.L	AUD.ACM.MCLK_OUT1	LSIO.GPIO2.IO15	GPIO2_15	AUD.SPDIF0.TX
	37	BD6	AUD.SPDIF0.EXT_CLK	DMA.DMA0.REQ_IN0		LSIO.GPIO2.IO16	GPIO2_16	AUD.SPDIF0.EXT_CLK
MLB	48	D32	CONN.MLB.PADP_CLK					CONN.MLB.PADP_CLK
	50	E33	CONN.MLB.PADN_CLK					CONN.MLB.PADN_CLK
	54	D30	CONN.MLB.PADP_S					CONN.MLB.PADP_S
	56	E31	CONN.MLB.PADN_S					CONN.MLB.PADN_S
	42	F34	CONN.MLB.PADP_D					CONN.MLB.PADP_D
	44	E35	CONN.MLB.PADN_D					CONN.MLB.PADN_D
	45	E1	CONN.MLB.SIG	AUD.SAI3.RXD		LSIO.GPIO3.IO26	GPIO3_28	CONN.MLB.SIG
	43	D2	CONN.MLB.CLK	AUD.SAI3.RXD		LSIO.GPIO3.IO27	GPIO3_28	CONN.MLB.CLK
	41	E3	CONN.MLB.DATA	AUD.SAI3.RXD		LSIO.GPIO3.IO28	GPIO3_28	CONN.MLB.DATA
ESAI1	49	BE11	AUD.ESAI1.FSR			LSIO.GPIO2.IO04	GPIO2_04	AUD.ESAI1.FSR
	47	BD12	AUD.ESAI1.SCKR			LSIO.GPIO2.IO06	GPIO2_06	AUD.ESAI1.SCKR
	51	BF10	AUD.ESAI1.TX0	AUD.SAI2.RXD		LSIO.GPIO2.IO08	GPIO2_08	AUD.ESAI1.TX0

Interface/ Function	Expansion2 Pin Number	i.MX 8 QM/QP SoC Pin Number	Function 0	Function 1	Function 2	Function 3	GPIO	Default State
	53	AU11	AUD.ESAI1.TX2_RX3			LSIO.GPIO2.IO10	GPIO2_10	AUD.ESAI1.TX2_RX3
	55	AV10	AUD.ESAI1.TX3_RX2			LSIO.GPIO2.IO11	GPIO2_11	AUD.ESAI1.TX3_RX2
	57	AY12	AUD.ESAI1.TX4_RX1			LSIO.GPIO2.IO12	GPIO2_12	AUD.ESAI1.TX4_RX1
	59	AT10	AUD.ESAI1.TX5_RX0			LSIO.GPIO2.IO13	GPIO2_13	AUD.ESAI1.TX5_RX0
QSPI	63	F10	LSIO.QSPI1A.SCLK			LSIO.GPIO4.IO21	GPIO4_21	LSIO.QSPI1A.SCLK
	65	J11	LSIO.QSPI1A.SS0_B			LSIO.GPIO4.IO19	GPIO4_19	LSIO.QSPI1A.SS0_B
	67	D12	LSIO.QSPI1A.DATA0			LSIO.GPIO4.IO26	GPIO4_26	LSIO.QSPI1A.DATA0
	69	D14	LSIO.QSPI1A.DATA1			LSIO.GPIO4.IO25	GPIO4_25	LSIO.QSPI1A.DATA1
	71	E13	LSIO.QSPI1A.DATA2			LSIO.GPIO4.IO24	GPIO4_24	LSIO.QSPI1A.DATA2
	73	E11	LSIO.QSPI1A.DATA3			LSIO.GPIO4.IO23	GPIO4_23	LSIO.QSPI1A.DATA3
SPI	62	AW5	DMA.SPI2.SCK			LSIO.GPIO3.IO07	GPIO3_07	DMA.SPI2.SCK
	64	AW1	DMA.SPI2.CS0			LSIO.GPIO3.IO10	GPIO3_10	DMA.SPI2.CS0
	68	BA1	DMA.SPI2.SDO			LSIO.GPIO3.IO08	GPIO3_08	DMA.SPI2.SDO
	66	AY4	DMA.SPI2.SDI			LSIO.GPIO3.IO09	GPIO3_09	DMA.SPI2.SDI
TAMPER	34	BE41	SNVS_TAMPER_IN0					SNVS_TAMPER_IN0
	36	BE43	SNVS_TAMPER_IN1					SNVS_TAMPER_IN1
	32	BD46	SNVS_TAMPER_OUT0					SNVS_TAMPER_OUT0
	38	BD42	SNVS_TAMPER_OUT1					SNVS_TAMPER_OUT1

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX 8 QM/QP Qseven SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the VCC_5V pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VCC_5V that 4.75V to 5.25V range. 12 pins are allocated to VCC_5V. The connector pin current rating is 0.5A per pin. This works out to 6A total for the 12 pins.

Table 12: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_5V[1]	4.75	5V	5.25V	±50mV
2	VCC_RTC[2]	2.4V	3V	3.3V	±20 mV

[1] *i.MX 8 QM/QP Qseven SOM is designed to work with VCC_5V input power rail from Qseven Edge connector.*

[2] *i.MX 8 QM/QP Qseven SOM uses this voltage as backup power source to RTC controller when VCC is off. This power is an optional power and can be left open if RTC functionality is not required.*

3.1.1 Power Input Sequencing

The i.MX 8 QM/QP Qseven SOM's Power Input sequence requirement is explained below.

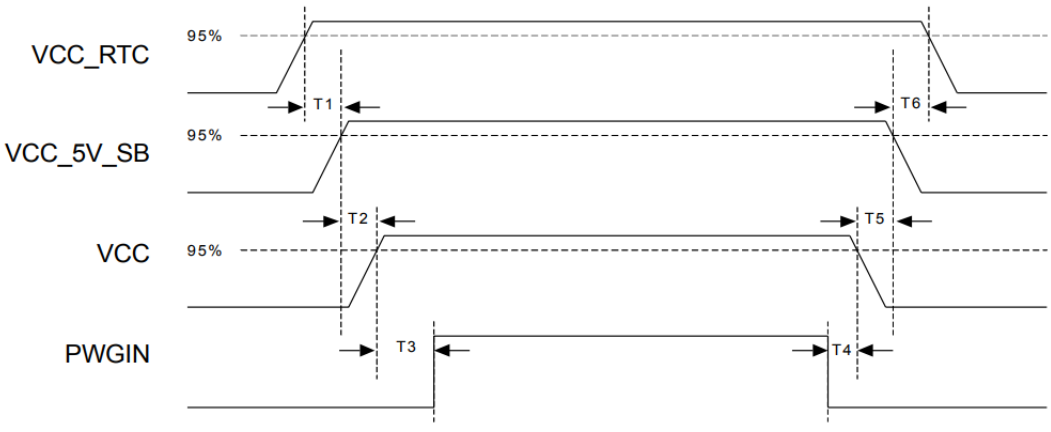


Figure 12: Power Input Sequencing

Table 13: Power Sequence Timing

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms
T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. Also make sure that all Carrier board interface peripherals' power supply must be OFF if SOM is powered OFF, otherwise it can cause internal latch-up and malfunctions/boot up issues due to reverse current flows.NXP recommends customers to remove power (Voltage source) to all components on the board in the event of a processor reset.

3.2 Power Consumption

Table 14: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Video run in MIPI display (Gstreamer)	VCC_5V	TBD
Play Video run in MIPI display (Gplay)	VCC_5V	TBD
Camera Streaming	VCC_5V	TBD
Play 4K Video run in HDMI display (Gplay)	VCC_5V	TBD
Play Audio	VCC_5V	TBD
Ping Bluetooth	VCC_5V	TBD
Ping Wi-Fi	VCC_5V	TBD
Ping Ethernet (Eth0)	VCC_5V	TBD
eMMC to Standard SD file transfer	VCC_5V	TBD
eMMC to USB3.0 file transfer	VCC_5V	TBD
eMMC to SATA file transfer	VCC_5V	TBD
Bluetooth file transfer	VCC_5V	TBD
Wi-Fi file transfer	VCC_5V	TBD
Ethernet Streaming (Video Play)	VCC_5V	TBD
GPU Processor -Graphics 3D Test	VCC_5V	TBD
Dhrystone	VCC_5V	TBD
Maximum Power Test: • Run the below during Maximum Power Test, • Play Video run in MIPI display (Gplay) • Camera Streaming • Ethernet (eth0) Run the ping (65500 packet size) • Wi-Fi- Run the ping teston back ground • FileTransfer - Transfer the 1GB files in storage devices • Run the dry2 application on back ground • GPU Processor -Graphics 3D Test	VCC_5V	TBD
Low Power Mode Power Consumption		

Task/Status	Power Rail	Current Drawn/ Power Consumption
System Idle Mode.	VCC_5V	TBD
Deep Sleep Mode.	VCC_5V	TBD
RTC power when no VIN_3V3 supply is provided	VDD_RTC	TBD

[1] Power consumption measurements have been done in iWave's i.MX 8 QM/QP CPU based Qseven Development platform with iWave's TBD.

3.3 EnvironmentalCharacteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of i.MX 8 QM/QP Qseven SOM.

Table 15: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

3.3.2 Heat Sink/ Heat Spreader

For any highly integrated System On Modules, thermal design is a very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management techniques like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the SoC.

Heat spreader acts as thermal coupling device between Module and external thermal solution. Heat spreader also provides thermal coupling to SoC via gap filler for better heat exchange. Heat spreader is not a complete thermal solution by itself. Heat spreader has to be used with application specific thermal solutions like heat sinks, Chassis, fans, Heat pipes etc.

Note: iWave supports Heat Sink/ Heat Spreader Solution for i.MX 8 Qseven SOM SOM. For more information on Heat Sink/ Heat Spreader contact iWave support team. Do not Power On the SOM without a proper thermal solution.

3.3.3 RoHS Compliance

iWave's i.MX 8 QM/QP Qseven SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.4 Electrostatic Discharge

iWave's i.MX 8 QM/QP Qseven SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage SOM e of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 i.MX 8 QM/QP Qseven SOM Mechanical Dimensions

i.MX 8 QM/QP Qseven SOM PCB size is 70mm x 70mm x 1.2mm. Qseven SOM mechanical dimension is shown below. (All dimensions are shown in mm)

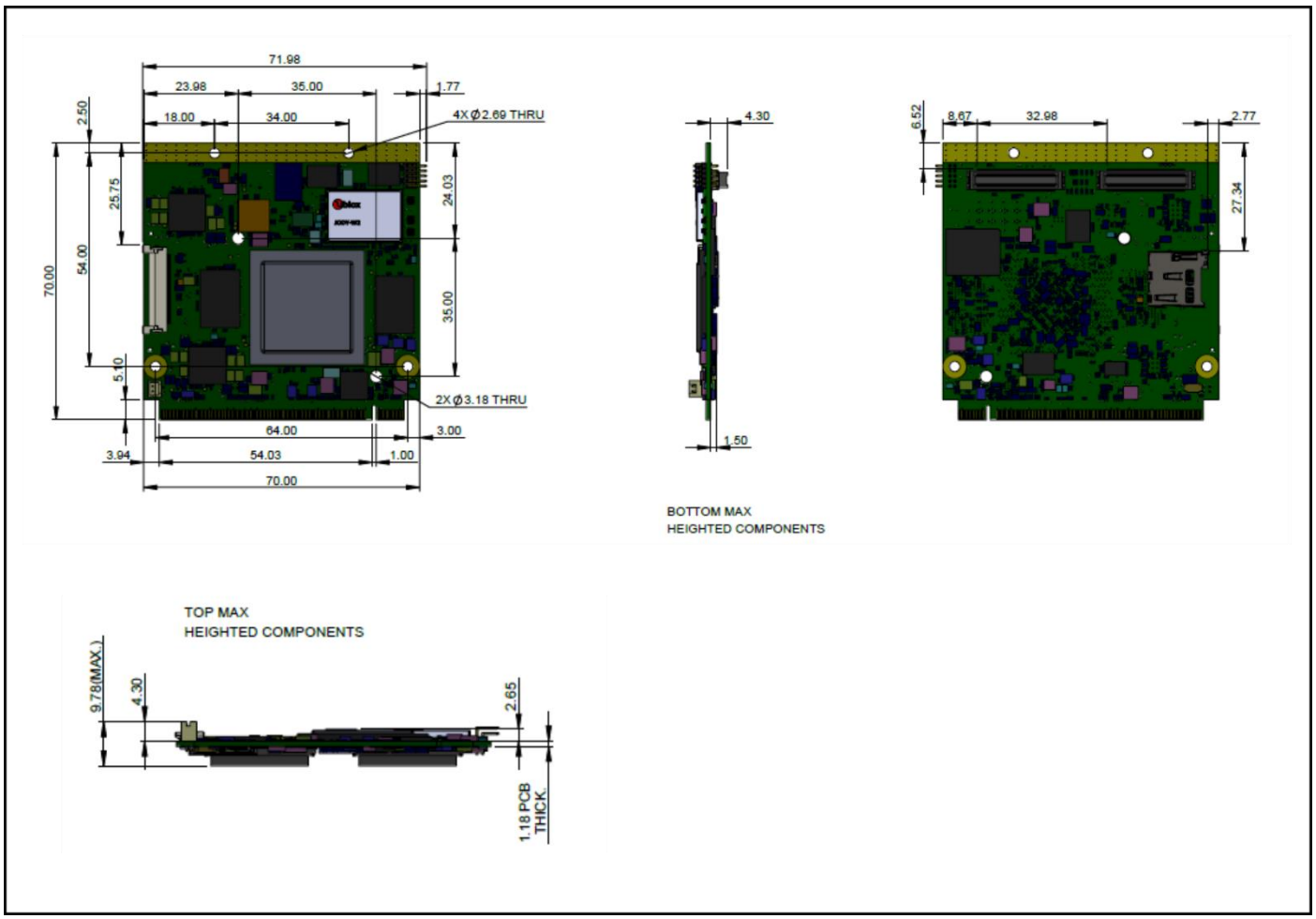


Figure 13: Mechanical dimension of i.MX 8 QM/QP Qseven SOM

The i.MX 8 QM/QP Qseven SOM PCB thickness is 1.2mm±0.1mm, top side maximum height component is Fan Header (4.3mm) followed by Boot Media Switch (2.65mm) and bottom side maximum height component are Expansion Connectors (4.3mm) followed by Bulk capacitors(1.5mm). Please refer the above figure which gives height details of the i.MX 8 QM/QP Qseven SOM.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX 8 QM/QP Qseven SOM variations. Please contact iWave for orderable part number of higher RAM memory size or Flash memory size SOM configurations. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, please contact iWave.

Table 16: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G27M - i.MX 8 Qseven SOM (Industrial grade) with Expansion Connector		
iW-G27M-Q7QM-4L004G-E016G-BIA	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L004G-E016G-BIB	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L008G-E032G-BIA	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L008G-E032G-BIB	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C
iW-Rainbow G27M - i.MX 8 Qseven SOM (Industrial grade) without Expansion Connector		
iW-G27M-Q7QM-4L004G-E016G-BIC	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L004G-E016G-BID	i.MX 8 Quad Max, 4GB LPDDR4, 16GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L008G-E032G-BIC	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - With Wi-Fi, BT	-40°C to 85°C
iW-G27M-Q7QM-4L008G-E032G-BID	i.MX 8 Quad Max, 8GB LPDDR4, 32GB eMMC flash with boot code - Without Wi-Fi, BT	-40°C to 85°C

Note: Some Product Part Numbers are subject to MOQ, please contact iWave Support Team for further information.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with QR Code on SOM

5. APPENDIX I

5.1 i.MX 8 QM/QP Qseven SOM Development Platform

iWave Systems supports iW-RainboW-27D-i.MX 8 QM/QP Qseven SOM Development Platform which is targeted for quick validation of i.MX 8 QM/QP SoC based Qseven SOM and its features. Being a Pico-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete supported features.

https://www.iwavesystems.com/product/i-mx-8-qm-qp-qseven-som/

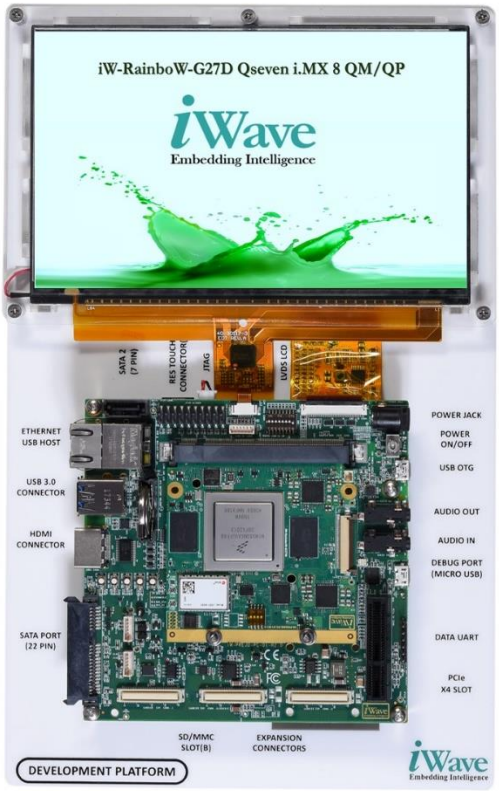


Figure 14: i.MX 8 QM/QP Qseven SOM Development Platform