iW-RainboW-G33M
i.MX8M Quad/QuadLite/Dual SMARC System On Module Hardware User Guide

Embedding Intelligence

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1. INTRODUCTION

1.1 Purpose

This document is the Hardware User Guide for the i.MX8M SMARC System On Module based on the NXP's i.MX8M Quad/QuadLite/Dual (Q/QL/D) Application processor. This board is fully supported by iWave Systems Technologies Pvt. Ltd. This Guide provides detailed information on the overall design and usage of the i.MX8M SMARC SOM from a Hardware Systems perspective.

1.2 SMARC SOM Overview

The SMARC ("Smart Mobility ARChitecture") is a versatile small form factor computer Module targeting application that require low power, low costs, and high performance. The SMARC modules have a standardized form factor of 85mm x 50mm and have specified pin outs based on the high speed MXM system connector that has a standardized pin out regardless of the vendor. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the SMARC module.

The Module PCBs have 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector. The Modules are used as building blocks for portable and stationary embedded systems. The core CPU and support circuits, including DRAM, boot flash, power sequencing, CPU power supplies, Dual Gigabit Ethernet are concentrated on the Module. The Modules are used with application specific Carrier Boards that implement other features such as audio CODECs, touch controllers, wireless devices, etc. The modular approach allows scalability, fast time to market and upgradability while still maintaining low costs, low power and small physical size.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
BT	Bluetooth
CPU	Central Processing Unit
CSI	Camera Serial Interface
DSI	Display Serial Interface
eMMC	Enhanced Multi Media Card
GB	Giga Byte
Gbps	Gigabits per sec
GPIO	General Purpose Input Output
I2C	Inter-Integrated Circuit
I2S	Inter-Integrated Sound

Acronyms	Abbreviations
IC	Integrated Circuit
LPDDR4	Low Power Double Data Rate4
MHz	Mega Hertz
MIPI	Mobile Industry Processor Interface
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
SAI	Serial Audio Interface
SD	Secure Digital
SMARC	Smart Mobility ARChitecture
SOM	System On Module
TBD	To Be Defined
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
Wi-Fi	Wireless Fidelity

1.4 Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
HCSL	High speed Current Steering Logic
LVDS	Low Voltage Differential Signal
TMDS	Transition-minimized differential signalling for HDMI
GBE MDI	Differential Analog signalling for Gigabit Media Dependent Interface
PCIe	PCIe differential pair signals
USB	Differential signalling used for traditional (non- Super-Speed) USB signals
USB SS	Differential signalling used for Super Speed USB 3.0
MIPI	Mobile Industry Processor Interface differential pair signals
OD	Open Drain Signal
OC	Open Collector Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented On-SMARC SOM.

1.5 References

- IMX8MDQLQIEC.pdf
- IMX8MDQLQRM.pdf
- SMARC Specification V2.0

1.6 Important Note

In this document, wherever i.MX8M CPU signal name is mentioned, it is followed as per below format for easy understanding.

- If CPU pin doesn't have multiplexing option or used for dedicated functionality then the signal name is mentioned as functionality name.

  "*Functionality Name*"

  Example: MIPI_DSI_D0_P

  In this signal, ***MIPI_DSI_D0_P*** pad is used for same functionality.

- If CPU pin has multiplexing option and selected particular function other than default option, then the signal name is mentioned as

  "Selected Function Name (CPU Pad name)"

  Example: UART2_CTS_B(UART4_RXD)

  In this signal, ***UART2_CTS_B*** is the functionality which we are using and ***UART4_RXD*** is the CPU Pad name.

- If CPU pin selected as GPIO function, then the signal name is mentioned as

  "*GPIO_Functionality* Description (GPIO Number)"

  Example: GPIO_LCD0_BKLT_EN(GPIO3_17)

  In this signal, ***LCD0_BKLT_EN*** is the GPIO functionality which we are using and ***GPIO3_17*** is the GPIO number.

Note: The above naming is not applicable for other signals which are not connected to CPU.

2. ARCHITECTURE AND DESIGN

This section provides detailed information about i.MX8M SMARC SOM features and Hardware architecture with high level block diagram.

2.1 i.MX8M SMARC SOM Block Diagram

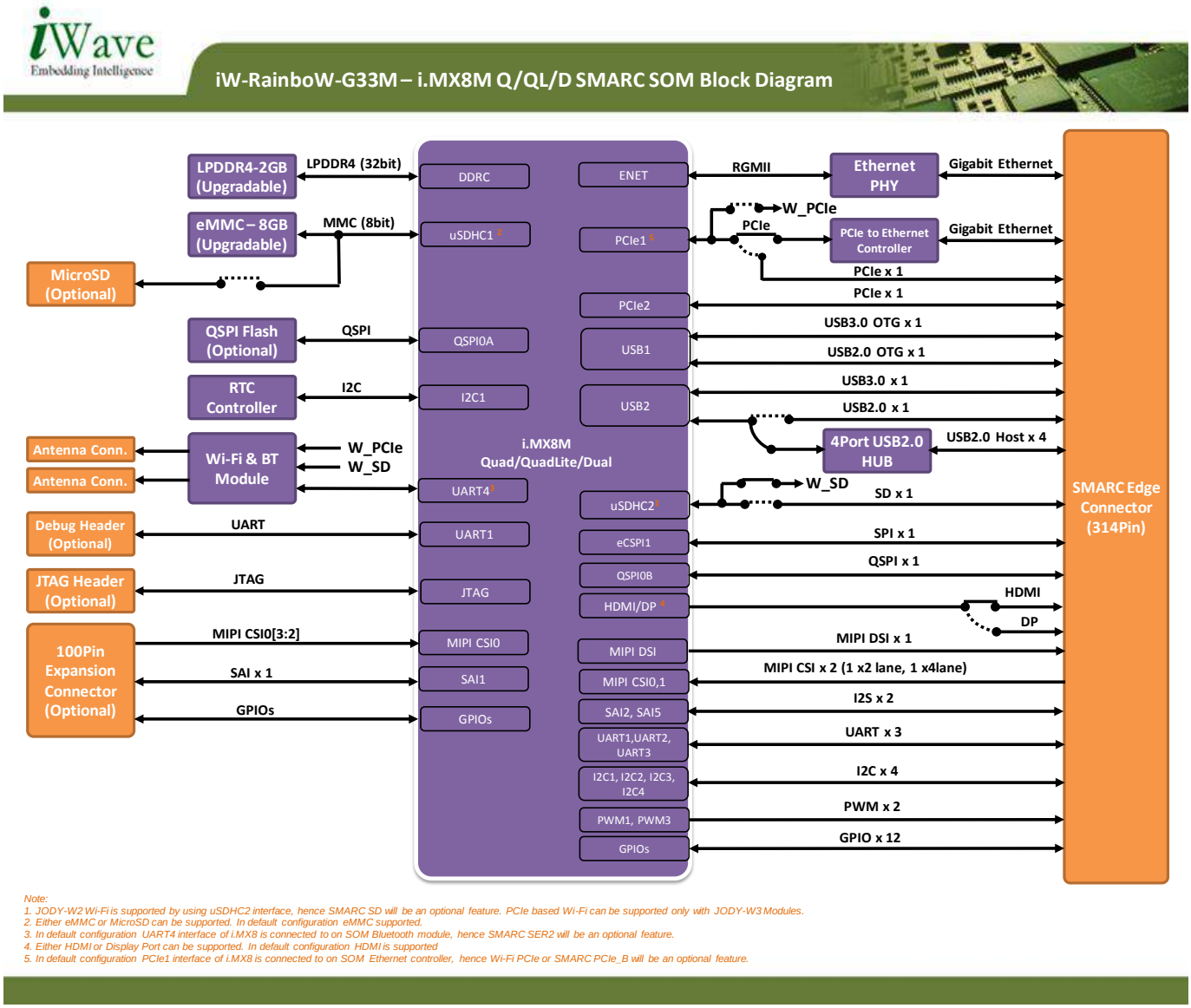

Figure 1: i.MX8M SMARC SOM Block Diagram

2.2 i.MX8M SMARC SOM Features

The i.MX8M SMARC SOM supports the following features.

CPU

- i.MX8M Q/QL/D Core Processor:
  - i.MX8MQuad Core : 4 x Cortex-A53 & 1 x Cortex-M4F
  - i.MX8MQuadLite : 4 x Cortex-A53 & 1 x Cortex-M4F (VPU Decoder not supported)
  - i.MX8MDual Core : 2 x Cortex-A53 & 1 x Cortex-M4F

Power

- PF4210 PMIC

Memory

- LPDDR4 - 2GB (Expandable)
- eMMC Flash - 8GB (Expandable)[1]
- Micro SD slot (Optional)[1]
- QSPI Flash (Optional)

Other On-SOM Features

- Wi-Fi & BT Module[2]
- Gigabit Ethernet PHY Transceiver x 1
- PCIe to Gigabit Ethernet Transceiver x 1[3]
- USB 2.0 High Speed 2-Port Hub
- RTC Controller
- FAN Header
- Debug UART Header (Optional)
- JTAG Header (Optional)

SMARC PCB Edge Interfaces

- MIPI DSI x 1 Channel
- HDMI/DP x 1 Port[4]
- MIPI CSI x 2 Channel (1x2lane and 1x4lane)[5]
- SD (4bit) x 1 Port (Optional)[3]
- SPI x 2 Port
- SAI/I2S (Audio Interface) x 2 Ports
- I2C x 4 Ports

- Data UART (with CTS & RTS) x 1 Port (One more optional port available)
- Data UART (without CTS & RTS) x 2 Ports
- USB 3.0 OTG x 1 Port
- USB 3.0 Host x 1 Ports
- USB 2.0 Host x 4Ports (through On-SOM USB Hub)
- PCIe x 1 Port[2]
- Gigabit Ethernet x 2 Ports[2]
- Watchdog Output x 1 Port
- GPIO x 12 pins
- Boot Select Signals
- Power & Management Signals

Expansion Connector Interfaces (Optional)

- SAI x 1 Port
- MIPI CSI0 (Lane2 & Lane3)[5]
- GPIOs

General Specification

- Power Supply : 5V, 3A
- Form Factor : 82mm X 50mm (SMARC V2.0 Specification)

[1] In i.MX8M SMARC SOM, SD1 interface signals are connected to both eMMC Flash and MicroSD connector. So either one feature only can be supported at a time in the SOM and by default, eMMC is supported.

[2] In i.MX8M SMARC SOM, PCIe2 interface signals are connected to Wi-Fi Module, PCIe to Ethernet controller and also to SMARC PCB Edge Connector. By default, PCIe2 is connected to PCIe to Ethernet controller and only PCIe1 is supported at SMARC PCB Edge connector in the SOM. and PCIe based Wi-Fi Can be supported only with JODY-W3 Module.

[3] In i.MX8M SMARC SOM, SD2 interface signals are connected to both SMARC PCB Edge Connector and Wi-Fi Module. By default, SD2 is connected to Wi-Fi Module.

[4] In i.MX8M CPU, HDMI & DP interface are multiplexed in same pins and so either one interface only can be used at a time. By default, HDMI interface is supported in i.MX8M SMARC SOM.

[5] The i.MX8M CPU supports two 4 lane MIPI_CSI interface. But SMARC support only two lanes for MIPI_CSI0 over Edge connector and so remaining two lanes of MIPI_CSI0 are connected to Expansion connector.

2.3 i.MX8M CPU

iW-RainboW-G33M SMARC SOM supports i.MX8M CPUs from NXP. The i.MX8M Family consists of three processors: i.MX8M Quad Core, i.MX8M QuadLite & i.MX8M Dual Core. The Major Difference between i.MX8M CPUs are:

- i.MX8M Quad Core : 4 x Cortex-A53 & 1 x Cortex-M4F
- i.MX8M QuadLite : 4 x Cortex-A53 & 1 x Cortex-M4F (VPU Decoder not supported)
- i.MX8M Dual Core : 2 x Cortex-A53 & 1 x Cortex-M4F

The i.MX 8M Quad/QuadLite/Dual processors feature advanced implementation of a quad/dual Arm® Cortex®-A53 core, which operates at speeds of up to 1.5 GHz. A general-purpose Cortex®-M4 core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. There are a number of other interfaces for connecting peripherals, such as WLAN, Bluetooth, GPS, displays, and camera sensors. The i.MX 8M Quad and i.MX 8M Dual processors have hardware acceleration for video playback up to 4K, and can drive the video outputs up to 60 fps. Although the i.MX 8M QuadLite processor does not have hardware acceleration for video decode, it allows for video playback with software decoders if needed.

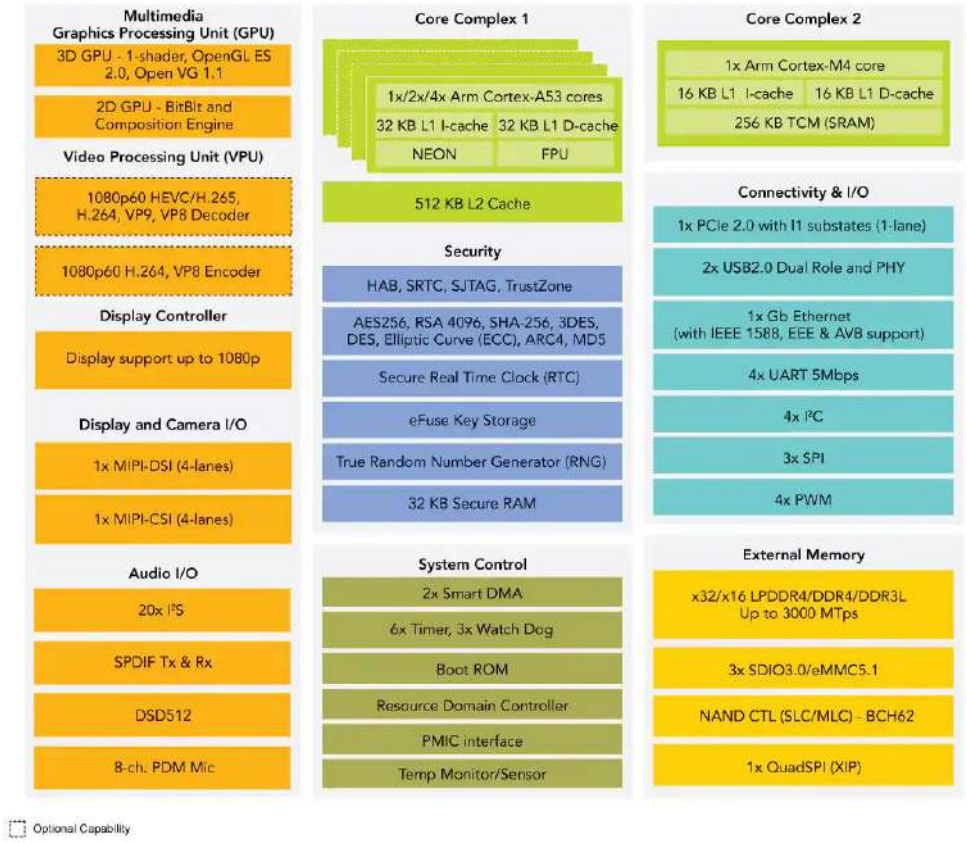

Figure 2: i.MX8MBlock Diagram

Note: The i.MX8M processor offers numerous advanced features, Refer the latest i.MX8M Datasheet & Reference Manual for Electrical characteristics and other information, which may be revised from time to time.

2.4 PF4210 PMIC

The i.MX8M SMARC SOM uses one PF4210 PMIC(U12) for SOM Power management. The PF4210 high performance power management integrated circuit (PMIC) provides a highly programmable/configurable architecture with fully integrated power devices and minimal external components The PF4210 PMIC are programmed with standard A1 Sequence.

2.5 Memory

2.5.1 LPDDR4 RAM

The i.MX8M SMARC SOM supports 2GB LPDDR4 RAM memory by default using 32bit DDR_CH0 channel of i.MX8M CPU to support LPDDR4 up to 1.6 GHz. LPDDR4 part U14 is placed on Top side of the SOM. The RAM size can be expandable up to maximum of 4GB. To customize the LPDDR4 memory size, contact iWave.

2.5.2 eMMC Flash

The i.MX8M SMARC SOM supports 8GB eMMC as default boot device and storage device. This is directly connected to uSDHC1 controller of the i.MX8M CPU and operates at 1.8V (I/O supply) and 3.3V (Core supply) Voltage levels. The eMMC flash memory is physically located on Top side of the SMARC SOM. The memory size of the eMMC Flash can be customised. To customize the eMMC memory size, contact iWave.

2.5.3 Micro SD Connector (Optional)

The i.MX8M SMARC SOM optionally supports Micro SD slot which can be used to connect Micro SD card as optional boot device as well as Mass storage device. Micro SD card connector (J4) and eMMC both share uSDHC1 controller of the i.MX8M CPU, hence either eMMC or microSD can be used at a time.

The main power to Micro SD Card Connector is 3.3 Voltage. The i.MX8M SMARC SOM supports configurable IO voltage levels for uSDHC1 lines through GPIO4_3. If GPIO4_3 is set to low, then 3.3V IO level is selected for uSDHC1 lines. If GPIO4_3 is set to high, then 1.8V IO level is selected for uSDHC1 lines. Micro SD Connector is physically located on Top side of the i.MX8M SMARC SOM.

Note: In default configuration, uSDHC1 is used for on board eMMC Flash. Contact iWave if MicroSD feature is required.

2.5.4 QSPI Flash (Optional)

The i.MX8M SMARC SOM optionally supports 2MB QSPI Flash. This is connected to QSPI_A controller of the i.MX8M processor and operates at 1.8V Voltage levels. The QSPI flash part U27 is physically located on Bottom side of the SMARC SOM. The QSPI Flash size can be expandable. For customised QSPI Flash support, contact iWave.

2.6 Network & Communication

2.6.1 Wi-Fi and Bluetooth Module

The i.MX8M SMARC SOM is integrated with u-blox's "JODY-W263" based Wi-Fi & Bluetooth module. The JODY-W2 series are compact modules based on the Marvell 88W8987 AEC-Q100 compliant chipset. They enable Wi-Fi, Bluetooth, and Bluetooth low energy communication. The JODY-W2 modules can be operated in the following modes:

• Wi-Fi 1x1 802.11a/b/g/n/ac in 2.4 GHz or 5 GHz

• Dual-mode Bluetooth 5, including audio, can be operated fully simultaneous with Wi-Fi

The JODY-W2(U16) undergoes extended automotive qualification according to ISO 16750-4 and is manufactured in line with ISO/TS 16949. Connection to a host processor is through SDIO, or High-Speed UART interfaces. The i.MX8M SMARC SOM uses processor's UART4 interface for Bluetooth and USDHC2 interface for Wi-Fi in a default configuration.

In i.MX8M SMARC SOM, antenna pins of JODY-W263 Bluetooth and Wi-Fi are connected to J7 and J8 connector respectively.

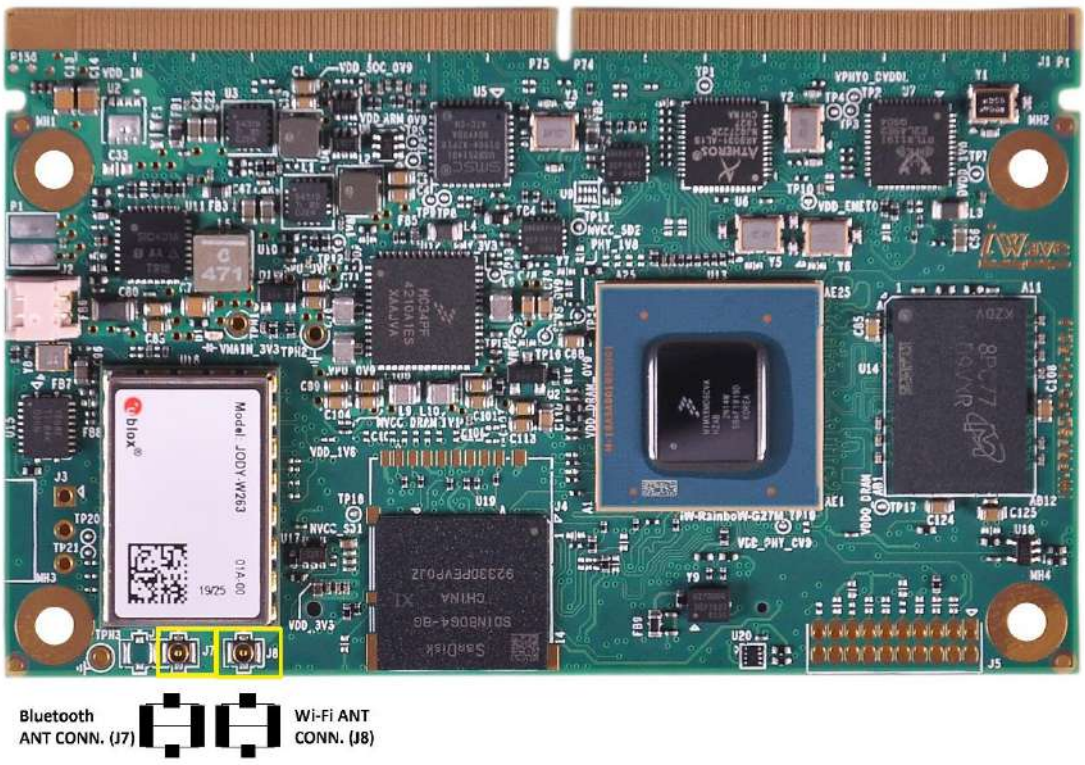

Figure 3: Wi-Fi and Bluetooth Antenna Connector

Connector Part Number : RECE-20449-001E-01 From Taoglas Limited.

Antenna Part Number : FXP830.24.0100B From Taoglas Limited.

2.7 RTC Controller

The i.MX8M SMARC SOM by supports external RTC Controller “PCF85263” On-SOM for Real time clock support. This external RTC Controller is connected to i.MX8M CPU through I2C1 Interface and operates at 3.3V voltage level. In SOM power off condition, this device will take power from SMARC PCB Edge (VDD_RTC) coin cell power input (Pin S147) and continues to keep the current time.

2.8 SMARC PCB Edge Connector

The i.MX8M SMARC SOM's SMARC PCB edge connector has standard pin out as per SMARC Specification V2.0. The interfaces which are available at 314pin SMARC Edge connector are explained in the following sections.

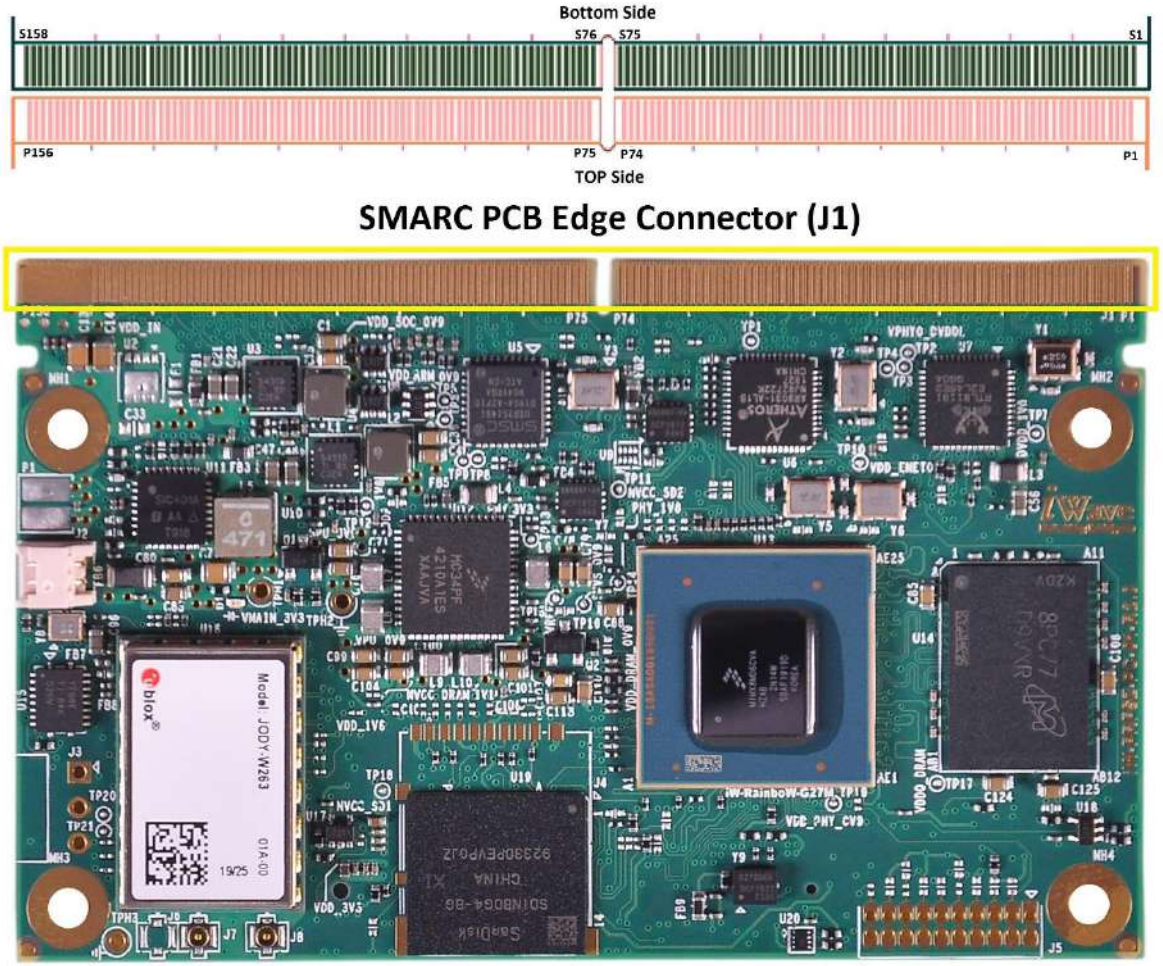

Figure 4: SMARC Edge Connector

Number of Pins - : 314

Connector Part - : Not Applicable (On Board PCB Edge connector)

Mating Connector - : 91782-3140M-001 from Aces

Table 3: SMARC Edge Connector Pinouts

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
GPIO_SMB_ALERT(GPIO1_00)	P1	S1	I2C1_SCL
GND	P2	S2	I2C1_SDA
MIPI_CSI2_CLK_P	P3	S3	GND
MIPI_CSI2_CLK_N	P4	S4	NC
NC	P5	S5	I2C3_SCL
NC	P6	S6	MCLK
MIPI_CSI2_DATA0_P	P7	S7	I2C3_SDA
MIPI_CSI2_DATA0_N	P8	S8	MIPI_CSI1_CLK_P
GND	P9	S9	MIPI_CSI1_CLK_N
MIPI_CSI2_DATA1_P	P10	S10	GND
MIPI_CSI2_DATA1_N	P11	S11	MIPI_CSI1_DATA0_P
GND	P12	S12	MIPI_CSI1_DATA0_N
MIPI_CSI2_DATA2_P	P13	S13	GND
MIPI_CSI2_DATA2_N	P14	S14	MIPI_CSI1_DATA1_P
GND	P15	S15	MIPI_CSI1_DATA1_N
MIPI_CSI2_DATA3_P	P16	S16	GND
MIPI_CSI2_DATA3_N	P17	S17	GBE1_MDI0+
GND	P18	S18	GBE1_MDI0-
GBE0_MDI3-	P19	S19	GBE1_LINK100#
GBE0_MDI3+	P20	S20	GBE1_MDI1+
GBE0_LINK100#	P21	S21	GBE1_MDI1-
GBE0_LINK1000#	P22	S22	GBE1_LINK1000#
GBE0_MDI2-	P23	S23	GBE1_MDI2+
GBE0_MDI2+	P24	S24	GBE1_MDI2-
GBE0_LINK_ACT#	P25	S25	GND
GBE0_MDI1-	P26	S26	GBE1_MDI3+
GBE0_MDI1+	P27	S27	GBE1_MDI3-
VPHY0_DVDDL	P28	S28	NC
GBE0_MDI0-	P29	S29	NC
GBE0_MDI0+	P30	S30	NC
NC	P31	S31	GBE1_LINK_ACT#
GND	P32	S32	NC
SD2_WP*	P33	S33	NC
SD2_CMD*	P34	S34	GND
SD2_CD_B*	P35	S35	USB_HUB3OUT_DP
SD2_CLK*	P36	S36	USB_HUB3OUT_DM
GPIO_SDIO_PWR_EN(GPIO2_19)*	P37	S37	VBUS_OTG
GND	P38	S38	SAI2_MCLK
SD2_DATA0*	P39	S39	SAI2_TXFS
SD2_DATA1*	P40	S40	SAI2_TXD0

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
SD2_DATA2*	P41	S41	SAI2_RXD0
SD2_DATA3*	P42	S42	SAI2_TXC
eCSPI1_SS0	P43	S43	NC
eCSPI1_SCLK	P44	S44	NC
eCSPI1_MISO	P45	S45	NC
eCSPI1_MOSI	P46	S46	NC
GND	P47	S47	GND
NC	P48	S48	I2C2_SCL
NC	P49	S49	I2C2_SDA
GND	P50	S50	SAI3_TXFS
NC	P51	S51	SAI3_TXD0
NC	P52	S52	SAI3_RXD0
GND	P53	S53	SAI3_TXC
QSPIB_SS0_B(NAND_CE2_B)	P54	S54	NC
QSPIB_SS1_B(NAND_CE3_B)	P55	S55	USB_HUB4_OC
QSPI_B_SCLK(NAND_CLE)	P56	S56	QSPI_B_DATA2(NAND_DATA06)
QSPI_B_DATA0(NAND_DATA04)	P57	S57	QSPI_B_DATA3(NAND_DATA07)
QSPI_B_DATA1(NAND_DATA05)	P58	S58	QSPI_B_DQS(NAND_RE_B)
GND	P59	S59	USB_HUB4OUT_DP
USB_OTG1_DP*	P60	S60	USB_HUB4OUT_DM
USB_OTG1_DM*	P61	S61	GND
USB3_EN_OC(GPIO3_19)*	P62	S62	USB1_TX_P
VBUS_OTG*	P63	S63	USB1_TX_N
USB_OTG1_ID*	P64	S64	GND
USB_HUB1OUT_DP	P65	S65	USB1_RX_P
USB_HUB1OUT_DM	P66	S66	USB1_RX_N
USB_HUB1_OC	P67	S67	GND
GND	P68	S68	USB_OTG1_DP
USB_HUB2OUT_DP	P69	S69	USB_OTG1_DM
USB_HUB2OUT_DM	P70	S70	GND
USB_HUB2_OC	P71	S71	USB2_TX_P
NC	P72	S72	USB2_TX_N
NC	P73	S73	GND
GPIO_USB3_EN_OC(GPIO3_19)	P74	S74	USB2_RX_P
		S75	USB2_RX_N
KEY			
GPIO_PCIE_RST(GPIO5_4)	P75	S76	GBE_PERST_N(GPIO5_4)*
USB_HUB3_OC	P76	S77	NC
NC	P77	S78	NC
NC	P78	S79	NC
GND	P79	S80	GND

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
NC	P80	S81	NC
NC	P81	S82	NC
GND	P82	S83	GND
PCIE1_REFCLK_P	P83	S84	PCIE2_REFCLK_P*
PCIE1_REFCLK_N	P84	S85	PCIE2_REFCLK_N*
GND	P85	S86	GND
PCIE1_RXP	P86	S87	PCIE2_RXP*
PCIE1_RXN	P87	S88	PCIE2_RXN*
GND	P88	S89	GND
PCIE1_TXP	P89	S90	PCIE2_TXP*
PCIE1_TXN	P90	S91	PCIE2_TXN*
GND	P91	S92	GND
HDMI_TX_DATA2_P	P92	S93	HDMI_TX_DATA0_P*
HDMI_TX_DATA2_N	P93	S94	HDMI_TX_DATA0_N*
GND	P94	S95	NC
HDMI_TX_DATA1_P	P95	S96	HDMI_TX_DATA1_P*
HDMI_TX_DATA1_N	P96	S97	HDMI_TX_DATA1_N*
GND	P97	S98	HDMI_HPD*
HDMI_TX_DATA0_P	P98	S99	HDMI_TX_DATA2_P*
HDMI_TX_DATA0_N	P99	S100	HDMI_TX_DATA2_N*
GND	P100	S101	GND
HDMI_CLK_P	P101	S102	HDMI_CLK_P*
HDMI_CLK_N	P102	S103	HDMI_CLK_N*
GND	P103	S104	USB_OTG1_ID
HDMI_HPD	P104	S105	HDMI_AUX_P*
HDMI_CTRL_SCL	P105	S106	HDMI_AUX_N*
HDMI_CTRL_SDA	P106	S107	NC
HDMI_CEC*	P107	S108	NC
SMARC_GPIO_0(GPIO3_16)	P108	S109	NC
SMARC_GPIO_1(GPIO1_12)	P109	S110	GND
SMARC_GPIO_2(GPIO1_15)	P110	S111	NC
SMARC_GPIO_3(GPIO1_11)	P111	S112	NC
SMARC_GPIO_4(GPIO1_10)	P112	S113	NC
SMARC_GPIO_5(GPIO1_01)	P113	S114	NC
SMARC_GPIO_6(GPIO1_09)	P114	S115	NC
SMARC_GPIO_7(GPIO1_06)	P115	S116	NC
SMARC_GPIO_8(GPIO1_08)	P116	S117	NC
SMARC_GPIO_9(GPIO1_03)	P117	S118	NC
SMARC_GPIO_10(GPIO1_07)	P118	S119	GND
SMARC_GPIO_11(GPIO1_04)	P119	S120	NC
GND	P120	S121	NC

Signal	SMARC Pin (Top)	SMARC Pin (Bottom)	Signal
I2C1_SCL*	P121	S122	NC
I2C1_SDA*	P122	S123	NC
BOOT_SEL0#	P123	S124	GND
BOOT_SEL1#	P124	S125	MIPI_DSI_DATA0_P
BOOT_SEL2#	P125	S126	MIPI_DSI_DATA0_N
GPIO_RESET_OUT(GPIO3_25)	P126	S127	GPIO_LCD0_1_EN(GPIO3_17)
RESET_IN#	P127	S128	MIPI_DSI_DATA1_P
POWER_BUTTON	P128	S129	MIPI_DSI_DATA1_N
UART2_TXD	P129	S130	GND
UART2_RXD	P130	S131	MIPI_DSI_DATA2_P
UART2_CTS_B(UART4_TXD)	P131	S132	MIPI_DSI_DATA2_N
UART2_RTS_B(UART4_RXD)	P132	S133	GPIO_LCD0_VDD_EN(GPIO3_18)
GND	P133	S134	MIPI_DSI_CLK_P
UART3_TXD	P134	S135	MIPI_DSI_CLK_N
UART3_RXD	P135	S136	GND
UART4_TX*	P136	S137	MIPI_DSI_DATA3_P
UART4_RX*	P137	S138	MIPI_DSI_DATA3_N
UART4_CTS_B*	P138	S139	I2C4_SCL
UART4_RTS_B*	P139	S140	I2C4_SDA
UART1_TXD	P140	S141	GPIO_LCD0_BL_PWM(GPIO1_14)
UART1_RXD	P141	S142	NC
GND	P142	S143	GND
NC	P143	S144	GPIO_WDT_OUT(GPIO1_02)*
NC	P144	S145	GPIO_WDT_OUT(GPIO1_02)
NC	P145	S146	GPIO_PCIe_Wake(GPIO5_5)
NC	P146	S147	VDD_RTC
VDD_IN	P147	S148	NC
VDD_IN	P148	S149	NC
VDD_IN	P149	S150	VIN_PWR_BAD#
VDD_IN	P150	S151	NC
VDD_IN	P151	S152	NC
VDD_IN	P152	S153	CARRIER_STBY#
VDD_IN	P153	S154	CARRIER_PWR_ON
VDD_IN	P154	S155	FORCE_RECOV#
VDD_IN	P155	S156	NC
VDD_IN	P156	S157	TEST#
		S158	GND

** Optional feature, by default not supported.*

2.8.1 MIPI DSI Display Interface

The i.MX8M SMARC SOM supports one four lane MIPI DSI display interfaces on SMARC PCB Edge connector. i.MX8M CPU's MIPI DSI controller with integrated D-PHY is directly connected to DSI0 interface of SMARC PCB Edge connector. Also it supports two I2C interface (I2C4) on SMARC PCB Edge connector for display configuration.

The i.MX8M CPU MIPI DSI is MIPI Alliance Specification for Display Serial Interface Version 1.1 compliant The MIPI DSI controller provides an interface that allows communication with MIPI DSI-compliant peripherals. The DSI Host Controller Core implements all three layers defined by the DSI Specification: Pixel to Byte Packing in the Application layer, Low Level Protocol, and Lane Management. The D-PHY interface of the DSI Host Controller Core supports up to four PHY Protocol Interface (PPI) compatible MIPI D-PHYs.

For more details on DSI pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S125	LVDS0_0+ / eDP0_TX0+/ DSI0_D0+	MIPI_DSI_DATA0_P	MIPI_DSI_D0_P/ B17	O, MIPI	MIPI DSI differential data lane0 positive.
S126	LVDS0_0- / eDP0_TX0-/ DSI0_D0-	MIPI_DSI_DATA0_N	MIPI_DSI_D0_N /A17	O, MIPI	MIPI DSI differential data lane0 negative.
S127	LCD0_BKLT_EN	GPIO_LCD0_1_EN(GPIO3_17)	NAND_WE_B/ K22	O, 1.8V CMOS	LCD0 Backlight Enable. *Note: GPIO3_17 is connected to this pin as GPIO for implementing LCD0 Backlight enable.*
S128	LVDS0_1+ / eDP0_TX1+/ DSI0_D1+	MIPI_DSI_DATA1_P	MIPI_DSI_D1_P/ B16	O, MIPI	MIPI DSI differential data lane1 positive.
S129	LVDS0_1- / eDP0_TX1-/ DSI0_D1-	MIPI_DSI_DATA1_N	MIPI_DSI_D1_N /A16	O, MIPI	MIPI DSI differential data lane1 negative.
S131	LVDS0_2+ / eDP0_TX2+/ DSI0_D2+	MIPI_DSI_DATA2_P	MIPI_DSI_D2_P/ B18	O, MIPI	MIPI DSI differential data lane2 positive.
S132	LVDS0_2- / eDP0_TX2-/ DSI0_D2-	MIPI_DSI_DATA2_N	MIPI_DSI_D2_N /A18	O, MIPI	MIPI DSI differential data lane2 negative.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S133	LCD0_VDD_EN	GPIO_LCD0_VDD_EN(GPIO3_18)	NAND_WP_B/ K21	O, 1.8V CMOS	LCD0 Power Enable. *Note: GPIO3_18 is connected to this pin as GPIO for implementing LCD0 Power enable.*
S134	LVDS0_CK+ / eDP0_AUX+/ DSI0_CLK+	MIPI_DSI_CLK_P	MIPI_DSI_CLK_P /D16	O, DSI	MIPI DSI differential Clock positive.
S135	LVDS0_CK- / eDP0_AUX-/ DSI0_CLK-	MIPI_DSI_CLK_N	MIPI_DSI_CLK_N/C16	O, DSI	MIPI DSI differential Clock negative.
S137	LVDS0_3+ / eDP0_TX3+/ DSI0_D3+	MIPI_DSI_DATA3_P	MIPI_DSI_D3_P/ B15	O, DSI	MIPI DSI differential data lane3 positive.
S138	LVDS0_3- / eDP0_TX3-/ DSI0_D3-	MIPI_DSI_DATA3_N	MIPI_DSI_D3_N /A15	O, DSI	MIPI DSI differential data lane3 negative.
S139	I2C_LCD_CK	I2C4_SCL	I2C4_SCL/ F8	O, 1.8V OD/ 4.7K PU	I2C4 Clock for Display.
S140	I2C_LCD_DAT	I2C4_SDA	I2C4_SDA/ F9	IO, 1.8V OD/ 4.7K PU	I2C4 Data for Display.
S141	LCD0_BKLT_PWM	GPIO_LCD0_BL_PWM(GPIO1_14)	GPIO1_IO14/ K7	O, 1.8V CMOS	LCD Back Light Brightness control through PWM.

2.8.2 HDMI/DP Interface

The i.MX8M SMARC SOM supports one HDMI Interface on SMARC PCB Edge connector. i.MX8M CPU's HD Display Transmitter Controller with integrated PHY is directly connected to HDMI port of SMARC PCB Edge connector. It supports dedicated DDC interface on SMARC PCB Edge connector for HDMI EDID read and to carry the HDCP & SCDC commands. i.MX8M CPU supports HDMI 1.4 Specification & HDMI 2.0a Specification.

Note: i.MX8M CPU supports HDMI CEC functionality and it is connected to 100Pin SOM Expansion connector because SMARC V2.0 specification doesn't support this.

i.MX8M CPU's HD Display Transmitter Controller IP offers multi-protocol support of standards such as High Definition Multimedia Interface (HDMI), DisplayPort, embedded DisplayPort (eDP), with one of these standards supported at a time. These protocols enable switching between the modes to be applied on a system level and performed by means of software configuration. The i.MX8M SMARC SOM by default supports HDMI interface on SMARC PCB Edge connector.

For more details on HDMI pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P92	HDMI_D2+/ DP1_LANE0+	HDMI_TX_DATA2_P	HDMI_TX_P_LN_2/N2	O, TMDS/ 0.1uf AC Coupled	HDMI Transceiver2 Positive.
P93	HDMI_D2-/ DP1_LANE0-	HDMI_TX_DATA2_N	HDMI_TX_M_LN_2/N1	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver2 Negative.
P95	HDMI_D1+/ DP1_LANE1+	HDMI_TX_DATA1_P	HDMI_TX_P_LN_1/U2	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver1 Positive.
P96	HDMI_D1-/ DP1_LANE1-	HDMI_TX_DATA1_N	HDMI_TX_M_LN_1/U1	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver1 Negative.
P98	HDMI_D0+/ DP1_LANE2+	HDMI_TX_DATA0_P	HDMI_TX_P_LN_0/T1	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver0 Positive.
P99	HDMI_D0-/ DP1_LANE2-	HDMI_TX_DATA0_N	HDMI_TX_M_LN_0/T2	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver0 Negative.
P101	HDMI_CK+/ DP1_LANE3+	HDMI_CLK_P	HDMI_TX_P_LN_3/M1	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver Clock Positive.
P102	HDMI_CK-/ DP1_LANE3-	HDMI_CLK_N	HDMI_TX_M_LN_3/M2	O, TMDS / 0.1uf AC Coupled	HDMI Transceiver Clock Negative.
P104	HDMI_HPD/ DP1_HPD	HDMI_HPD	HDMI_HPD/ W2	I, 1.8V CMOS	HDMI Hot Plug Detect.
P105	HDMI_CTRL_CK/DP1_AUX+	HDMI_CTRL_SCL	HDMI_DDC_SCL/R3	O, 1.8V OD/ 2.2K PU	HDMI DDC Clock.
P106	HDMI_CTRL_DAT/DP1_AUX-	HDMI_CTRL_SDA	HDMI_DDC_SDA/P3	IO, 1.8V OD/ 2.2K PU	HDMI DDC DATA.

i.MX8M SMARC SOM optionally supports DP interface on DP0 port of SMARC PCB Edge connector. The same HDMI output pins from i.MX8M CPU is connected to DP0 port of SMARC PCB Edge connector through resistors and default not populated. Also it supports AUX master interface. To add DP0 interface support on SMARC PCB Edge connector, contact iWave.

For more details on DP pinouts on SMARC PCB edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S93	DP0_LANE0+	NC	HDMI_TX_P_LN_0/T1	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane0 Positive through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P98th pin through resistor and default populated.*
S94	DP0_LANE0-	NC	HDMI_TX_M_LN_0/T2	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane0 Negative through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P99th pin through resistor and default populated.*
S95	DP0_AUX_SEL	NC	NA	NA	NC.
S96	DP0_LANE1+	NC	HDMI_TX_P_LN_1/U2	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane1 Positive through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P95th pin through resistor and default populated.*
S97	DP0_LANE1-	NC	HDMI_TX_M_LN_1/U1	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane1 Negative through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P96th pin through resistor and default populated.*
S98	DP0_HPD	NC	HDMI_HPD/ W2	I, 1.8V CMOS	Default NC. *Note: This pin is optionally connected to DP Hot plug through resistor and default not populated.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Same signal is also connected to SMARC Edge P104th pin through resistor and default populated.
S99	DP0_LANE2+	NC	HDMI_TX_P_LN_2/N2	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane2 Positive through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P92nd pin through resistor and default populated.*
S100	DP0_LANE2-	NC	HDMI_TX_M_LN_2/N1	O, DP	Default NC. *Note: This pin is optionally connected to DP Lane2 Negative through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P93rd pin through resistor and default populated.*
S102	DP0_LANE3+	NC	HDMI_TX_P_LN_3/M1	O, DP	Default NC. *Note: This pin is optionally connected to HDMI Clock Positive through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P101st pin through resistor and default populated.*
S103	DP0_LANE3-	NC	HDMI_TX_M_LN_3/M2	O, DP	Default NC. *Note: This pin is optionally connected to DP Clock Negative through resistor and default not populated.* *Note: Same signal is also connected to SMARC Edge P102nd pin through resistor and default populated.*
S105	DP0_AUX+	NC	HDMI_AUX_P/V1	IO, 1.8 CMOS/0.1Uf AC Coupled	Default NC. *Note: This pin is optionally connected to DP Aux Positive through resistor and default not populated.*
S106	DP0_AUX-	NC	HDMI_AUX_N/V2	IO, 1.8 CMOS/0.1Uf AC Coupled	Default NC. *Note: This pin is optionally connected to DP Aux Negative through resistor and default not populated.*

Note: In default configuration HDMI is supported, contact iWave support team if eDP or DP supported SOM is required.

2.8.3 MIPI CSI Camera Interface

The i.MX8M SMARC SOM supports one two lane and one four lane MIPI CSI 2.0 serial camera interfaces on SMARC PCB Edge connector. i.MX8M CPU's MIPI CSI1 camera interface supports up to four lanes, in that, first two lane is connected to CSI0 interface of SMARC PCB Edge connector and 2nd two lane is connected to Expansion connector. i.MX8M CPU's MIPI CSI2 camera interface supports up to four lanes and directly connected from CSI1 interface of SMARC PCB Edge connector. Also it supports two I2C interfaces (I2C1 & I2C3) on SMARC PCB Edge connector for camera configuration.

The i.MX8M CPU supports the CSI-2 Rx Controller Core implements all three layers defined by the CSI-2 Specification: Pixel to Byte Packing, Low Level Protocol, and Lane Management. The D-PHY interface of the CSI-2 Rx Controller Core supports PHY Protocol Interface (PPI) compatible MIPI D-PHYs. The CSI-2 Rx Controller Core takes care of all packet formatting details and transmission over the MIPI bus.

For more details on MIPI CSI1 pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S5	CSI0_TX-/ I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/ G8	O, 1.8V OD/ 4.7K PU	I2C3 Clock for Camera0.
S6	CAM_MCK	MCLK	SAI1_MCLK/ A3	O, 1.8V CMOS	Master Clock for Camera.
S7	CSI0_TX+/ I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/ E9	IO, 1.8V OD/ 4.7K PU	I2C3 Data for Camera0.
S8	CSI0_CK+	MIPI_CSI1_CLK_P	MIPI_CSI1_CLK_P/B22	I, MIPI	MIPI CSI1 differential Clock Positive.
S9	CSI0_CK-	MIPI_CSI1_CLK_N	MIPI_CSI1_CLK_N/A22	I, MIPI	MIPI CSI1 differential Clock Negative.
S11	CSI0_RX0+	MIPI_CSI1_DATA0_P	MIPI_CSI1_D0_P/B23	I, MIPI	MIPI CSI1 differential data lane 0 positive.
S12	CSI0_RX0-	MIPI_CSI1_DATA0_N	MIPI_CSI1_D0_N/A23	I, MIPI	MIPI CSI1 differential data lane0 negative.
S14	CSI0_RX1+	MIPI_CSI1_DATA1_P	MIPI_CSI1_D1_P/D22	I, MIPI	MIPI CSI1 differential data lane1 positive.
S15	CSI0_RX1-	MIPI_CSI1_DATA1_N	MIPI_CSI1_D1_N/C22	I, MIPI	MIPI CSI1 differential data lane1 negative.

For more details on MIPI CSI2 pinouts on SMARC PCB edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P3	CSI1_CK+	MIPI_CSI2_CLK_P	MIPI_CSI2_CLK_P/B19	I, MIPI	MIPI CSI2 differential Clock Positive.
P4	CSI1_CK-	MIPI_CSI2_CLK_N	MIPI_CSI2_CLK_N/A19	I, MIPI	MIPI CSI2 differential Clock Negative.
P7	CSI1_RX0+	MIPI_CSI2_DATA0_P	MIPI_CSI2_D0_P/D20	I, MIPI	MIPI CSI2 differential data lane0 positive.
P8	CSI1_RX0-	MIPI_CSI2_DATA0_N	MIPI_CSI2_D0_N/C20	I, MIPI	MIPI CSI2 differential data lane0 negative.
P10	CSI1_RX1+	MIPI_CSI2_DATA1_P	MIPI_CSI2_D1_P/B20	I, MIPI	MIPI CSI2 differential data lane1 positive.
P11	CSI1_RX1-	MIPI_CSI2_DATA1_N	MIPI_CSI2_D1_N/A20	I, MIPI	MIPI CSI2 differential data lane1 negative.
P13	CSI1_RX2+	MIPI_CSI2_DATA2_P	MIPI_CSI2_D2_P/B21	I, MIPI	MIPI CSI2 differential data lane positive.
P14	CSI1_RX2-	MIPI_CSI2_DATA2_N	MIPI_CSI2_D2_N/A21	I, MIPI	MIPI CSI2 differential data lane2 negative.
P16	CSI1_RX3+	MIPI_CSI2_DATA3_P	MIPI_CSI2_D3_P/D19	I, MIPI	MIPI CSI2 differential data lane3 positive.
P17	CSI1_RX3-	MIPI_CSI2_DATA3_N	MIPI_CSI2_D3_N/C19	I, MIPI	MIPI CSI2 differential data lane3 negative.
S1	CSI1_TX+/ I2C_CAM1_CK	I2C1_SCL	I2C1_SCL/ E7	O, 1.8V OD/ 4.7K PU	I2C1 Clock for Camera1. *Note: This I2C1 is also shared to PMIC & RTC Controller.*
S2	CSI1_TX-/ I2C_CAM1_DAT	I2C1_SDA	I2C1_SDA/ E8	IO, 1.8V OD/ 4.7K PU	I2C1 Data for Camera1. *Note: This I2C1 is also shared to PMIC & RTC Controller.*

2.8.4 SDIO Interface (Optional)

The i.MX8M SMARC SOM supports one 4bit SDIO interface on SMARC PCB Edge connector. i.MX8M CPU's uSDHC2 controller is used for this interface and can be used for Mass storage or as optional boot device. It supports 1-bit or 4-bit transfer mode for SD/SDIO and works upto UHS-I mode @ up to 208 MHz. Also i.MX8M SMARC SOM supports SDIO card detect function, power enable function through CPU GPIOs GPIO2_12 & GPIO2_19 respectively and connected to SMARC PCB Edge connector.

The i.MX8M SMARC SOM supports configurable IO voltage levels for uSDHC2 lines which can be controlled through CPU GPIO GPIO4_2. If GPIO4_2 is set to low, then 3.3V IO level is selected for uSDHC2 lines and if GPIO4_2 is set to high, then 1.8V IO level is selected for uSDHC2 lines.

For more details on SDIO pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P33	SDIO_WP	NC	SD2_WP/ M21	I, 3.3V CMOS 10K PU	Default NC. *Note: SD2_WP is by default connected to On -SOM Wi-Fi module as a GPIO3_00 through resistor and default populated.*
P34	SDIO_CMD	NC	SD2_CMD/ M22	IO, 3.3V/1.8V CMOS	Default NC. *Note: SD2_CMD is by default connected to On -SOM Wi-Fi through resistor and default populated.*
P35	SDIO_CD#	NC	SD2_CD_B/ L21	I, 3.3V CMOS 10K PU	Default NC. *Note: SD2_CD_B is by default connected to On -SOM Wi-Fi module as a GPIO3_06 through resistor and default populated.*
P36	SDIO_CK	NC	SD2_CLK/ L22	O, 3.3V/1.8V CMOS	Default NC. *Note: SD2_CLK is by default connected to On -SOM Wi-Fi module through resistor and default populated.* *Note: 10K pullup option is provided.*
P37	SDIO_PWR_EN	NC	SD2_RESET_B/ R22	O, 3.3V MOS/ 10K PU	Default NC. *Note: SD2_CLK is by default connected to On -SOM Wi-Fi module through resistor and default populated*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P39	SDIO_D0	NC	SD2_DATA0/ N22	IO, 3.3V/1.8V CMOS	Default NC. *Note: SD2_DATA0 is by default connected to On -SOM Wi-Fi through resistor and default populated.* *Note: 10K pullup option is provided.*
P40	SDIO_D1	NC	SD2_DATA1/ N21	IO, 3.3V/1.8V CMOS	Default NC. *Note: SD2_DATA1 is by default connected to On -SOM Wi-Fi module through resistor and default populated.* *Note: 10K pullup option is provided.*
P41	SDIO_D2	NC	SD2_DATA2/ P22	IO, 3.3V/1.8V CMOS	Default NC. *Note: SD2_DATA2 is by default connected to On -SOM Wi-Fi module through resistor and default populated.* *Note: 10K pullup option is provided.*
P42	SDIO_D3	NC	SD2_DATA3/ P21	IO, 3.3V/1.8V CMOS	Default NC. *Note: SD2_DATA3 is by default connected to On -SOM Wi-Fi module through resistor and default populated.* *Note: 10K pullup option is provided.*

Note: In default configuration, Usdhc2 is used for on board Wi-Fi Module. Contact iWave if SMARC SD feature is required.

2.8.5 SPI Interface

The i.MX8M SMARC SOM supports QSPI interface on SMARC PCB Edge connector. i.MX8M CPU's QSPIB is directly connected to eSPI/SPI1 port of SMARC PCB Edge connector. QSPIB is mainly used for Flash interface and Single, dual, quad mode of operation.

Optionally, i.MX8M SMARC SOM can support one SPI interface on SMARC Edge connector when On-SOM Wi-Fi is not used or Wi-Fi is used with SD interface. i.MX8M CPU's eCSPI1 can be connected to SPI0 port of SMARC PCB Edge connector. The i.MX8M CPU's Enhanced Configurable Serial Peripheral Interface (ECSPI) module is a full-duplex, synchronous, four-wire serial communication block and Master/Slave configurable.

For more details on QSPI1B pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P54	ESPI_CS0#	QSPIB_SS0_B (NAND_CE2_B)	NAND_CE2_B/ F21	O, 1.8V CMOS	QSPIB Chip Select 0.
P55	ESPI_CS1#	QSPIB_SS1_B (NAND_CE3_B)	NAND_CE3_B/ H20	O, 1.8V CMOS	QSPIB Chip Select 1.
P56	ESPI_CK	QSPI_B_SCLK (NAND_CLE)	NAND_CLE/ H21	O, 1.8V CMOS	QSPIB Clock.
P57	ESPI_IO_0	QSPI_B_DATA0(NAND_DATA04)	NAND_DATA04/ L20	IO, 1.8V CMOS	QSPIB DATA 0 Lane.
P58	ESPI_IO_1	QSPI_B_DATA1(NAND_DATA05)	NAND_DATA05/ J22	IO, 1.8V CMOS	QSPIB DATA 1 Lane.
S43	ESPI_ALERT0#	NC	NA	NA	NC.
S44	ESPI_ALERT1#	NC	NA	NA	NC.
S56	ESPI_IO_2	QSPI_B_DATA2(NAND_DATA06)	NAND_DATA06/ L19	IO, 1.8V CMOS	QSPIB Data 3 Lane.
S57	ESPI_IO_3	QSPI_B_DATA3(NAND_DATA07)	NAND_DATA07/ M19	IO, 1.8V CMOS	QSPIB Data 2 Lane.
S58	ESPI_RESET#	QSPI_B_DQS(NAND_RE_B)	NAND_RE_B/ K19	O, 1.8V CMOS	QSPI RESET.

For more details on SPI0 pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P43	SPI0_CS0#	ECSPI1_SS0	ECSPI1_SS0/ D4	O, 1.8V CMOS	ECSPI1 Chip Select 0.
P44	SPI0_CK	ECSPI1_SCLK	ECSPI1_SCLK/ D5	O, 1.8V CMOS	ECSPI1 Chip Select clock.
P45	SPI0_DIN	ECSPI1_MISO	ECSPI1_MISO/ B4	I, 1.8V CMOS	ECSPI1 Chip Select Master in slave out.
P46	SPI0_DO	ECSPI1_MOSI	ECSPI1_MOSI/ E5	O, 1.8V CMOS	ECSPI1 Chip Select Master out slave in.

2.8.6 Audio Interface

The i.MX8M SMARC SOM supports two I2S interface on SMARC PCB Edge connector for Audio. i.MX8M CPU's SAI2 and SAI3 channels are directly connected to I2S0 and I2S1 channels of SMARC PCB Edge connector respectively. The Synchronous Audio Interface (SAI) supports full duplex serial interfaces with frame synchronization such as I2S, AC97 and other audio CODEC/DSP interfaces. The SAI general features are including Transmitter section with independent bit clock and frame sync, Maximum frame size of 32 words, Word size from 8-bits to 32-bits and Supports graceful restart after FIFO error. Only Transmitter CK and LRCK is supported as per SMARC specification.

In i.MX8M SMARC SOM the transmitter is configured for asynchronous mode and the receiver is configured for synchronous mode, hence both transmitter and receiver will use the transmitter bit clock and frame sync.

For more details on Audio Interface pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S38	AUDIO_MCK	SAI2_MCLK	SAI2_MCLK/ H5	O, 1.8V CMOS	Master Clock for Audio codec.
S39	I2S0_LRCK	SAI2_TXFS	SAI2_TXFS/ H4	O, 1.8V CMOS	SAI2 Transmit Frame Sync.
S40	I2S0_SDOUT	SAI2_TXD0	SAI2_TXD0/ G5	O, 1.8V CMOS	SAI2 Transmit Data Lane 0.
S41	I2S0_SDIN	SAI2_RXD0	SAI2_RXD0/ H6	I, 1.8V CMOS	SAI2 Receive Data Lane 0.
S42	I2S0_CK	SAI2_TXC	SAI2_TXC/ J5	O, 1.8V CMOS	SAI2 Transmit Clock.
S48	I2C_GP_CK	I2C2_SCL	I2C2_SCL/ G7	O, 1.8V OD/ 4.7K PU	I2C2 Serial Clock for Audio codec.
S49	I2C_GP_DAT	I2C2_SDA	I2C2_SDA/ F7	IO, 1.8V OD/ 4.7K PU	I2C2 Serial Data for Audio codec.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S50	HDA_SYC/ I2S2_LRCK	SAI3_TXFS	SAI3_TXFS/ G3	O, 1.8V CMOS	SAI3 Transmit Frame Sync.
S51	HDA_SDO/ I2S2_SDOUT	SAI3_TXD0	SAI3_TXD/ C3	O, 1.8V CMOS	SAI3 Transmit Data Lane 0.
S52	HDA_SDI/ I2S2_SDIN	SAI3_RXD0	SAI3_RXD/ F3	I, 1.8V CMOS	SAI3 Receive Data Lane 0.
S53	HDA_CK/ I2S2_CLK	SAI3_TXC	SAI3_TXC/ C4	O, 1.8V CMOS	SAI3 Transmit Clock.

2.8.7 I2C Interface

The i.MX8M SMARC SOM supports four I2C interface on SMARC PCB Edge connector. i.MX8M CPU's I2C1, I2C2, I2C3 & I2C4 interfaces are connected to SMARC PCB Edge connector for I2C. In that, i.MX8M CPU's I2C1 interface is connected to On-SOM peripherals (PMIC with slave address 0x08 & RTC Controller with slave address 0x51) and also shared to I2C_CAM1 port of SMARC PCB Edge connector.

For more details on I2C Interface pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S1	CSI1_TX+/ I2C_CAM1_CK	I2C1_SCL	I2C1_SCL/ E7	O, 1.8V OD/ 4.7K PU	I2C1 Clock for Camera1.
S2	CSI1_TX-/ I2C_CAM1_DAT	I2C1_SDA	I2C1_SDA/ E8	IO, 1.8V OD/ 4.7K PU	I2C1 Data for Camera1.
S5	CSI0_TX-/ I2C_CAM0_CK	I2C3_SCL	I2C3_SCL/ G8	O, 1.8V OD/ 4.7K PU	I2C3 Clock for Camera0.
S7	CSI0_TX+/ I2C_CAM0_DAT	I2C3_SDA	I2C3_SDA/ E9	IO, 1.8V OD/ 4.7K PU	I2C3 Data for Camera0.
S48	I2C_GP_CK	I2C2_SCL	I2C2_SCL/ G7	O, 1.8V OD/ 4.7K PU	I2C2 Serial Clock for General Purpose.
S49	I2C_GP_DAT	I2C2_SDA	I2C2_SDA/ F7	IO, 1.8V OD/ 4.7K PU	I2C2 Serial Data for General Purpose.
P121	I2C_PM_CK	NC	I2C1_SCL/ E7	IO, 1.8V OD/ 4.7K PU	Default NC. *Note: This pin is optionally connected from I2C1_SCL through resistor and default not populated.*
P122	I2C_PM_DAT	NC	I2C1_SCD/ E8	O, 1.8V OD/ 4.7K PU	Default NC. *Note: This pin is optionally connected from I2C1_SDA through resistor and default not populated.*
S139	I2C_LCD_CK	I2C4_SCL	I2C4_SCL/ F8	O, 1.8V OD/ 4.7K PU	I2C4 Clock for Display.
S140	I2C_LCD_DAT	I2C4_SDA	I2C4_SDA/ F9	IO, 1.8V OD/ 4.7K PU	I2C4 Data for Display.

2.8.8 UART Interface

The i.MX8M SMARC SOM supports three UART interface on SMARC PCB Edge connector in default configuration. The i.MX8M CPU's UART2, UART3 & UART1 interfaces are directly connected to SER0, SER1 & SER3 port of SMARC PCB Edge connector respectively. In this, UART1 which is connected to SER3 is used as Debug UART. The i.MX8M CPU's UART supports NRZ encoding format, RS485 compatible 9 bit data format and IrDA compatible infrared slow data rate (SIR) format.

Optionally, i.MX8M SMARC SOM can support one more UART interface on SMARC Edge connector when On-SOM Bluetooth is not used. i.MX8M CPU's UART4 can be connected to SER2 port of SMARC PCB Edge connector.

For more details on UART pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P129	SER0_TX	UART2_TXD	UART2_TXD/ D6	O, 1.8V CMOS	UART2 Transmitter.
P130	SER0_RX	UART2_RXD	UART2_RXD/ B6	I, 1.8V CMOS	UART2 Receiver.
P131	SER0_RTS#	UART2_CTS_B(UART4_TXD)	UART4_TXD/ D7	I, 1.8V CMOS	UART2 Clear to Send.
P132	SER0_CTS#	UART2_RTS_B(UART4_RXD)	UART4_RXD/ C6	O, 1.8V CMOS	UART2 Request to Send.
P134	SER1_TX	UART3_TXD	UART3_TXD/ B7	O, 1.8V CMOS	UART3 Transmitter.
P135	SER1_RX	UART3_RXD	UART3_RXD/ A6	I, 1.8V CMOS	UART3 Receiver.
P136	SER2_TX	UART4_TX	ECSPI2_MOSI /E5	O, 1.8V CMOS	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's UART4_TX(ECSPI2_MOSI) through resistor and default not populated.* *Note: UART4_TX(ECSPI2_MOSI) is by default connected to On -SOM Bluetooth through resistor and default populated.*
P137	SER2_RX	UART4_RX	ECSPI2_SCLK /C5	I, 1.8V CMOS	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's UART4_RX(ECSPI2_SCLK) through resistor and default not populated.* *Note: UART4_RX(ECSPI2_SCLK) is by default connected to On -SOM*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					Bluetooth through resistor and default populated.
P138	SER2_RTS#	UART4_CTS_B	ECSPI2_MISO /B5	I, 1.8V CMOS	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's UART4_CTS_B through resistor and default not populated.* *Note: UART4_CTS_B(ECSPI2_MISO) is by default connected to On -SOM Bluetooth through resistor and default populated.*
P139	SER2_CTS#	UART4_RTS_B	ECSPI2_SS0/ A5	O, 1.8V CMOS	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's UART4_RTS_B through resistor and default not populated.* *Note: UART4_RTS_B(ECSPI2_SS0) is by default connected to On -SOM Bluetooth through resistor and default populated.*
P140	SER3_TX	UART1_TXD	UART1_TXD/ A7	O, 1.8V CMOS	UART1 Transmitter.
P141	SER3_RX	UART1_RXD	UART1_RXD/ C7	I, 1.8V CMOS	UART1 Receiver.

2.8.9 Watchdog Interface

The i.MX8M SMARC SOM supports one Watchdog output on SMARC PCB Edge connector. i.MX8M CPU's Watchdog Timer (WDOG) module out is directly connected to Watchdog output of SMARC PCB Edge connector. i.MX8M WDOG has configurable timeout counter with timeout periods from 0.5 to 128 seconds and time resolution of 0.5 seconds. Once the WDOG is activated, it must be serviced by the software on a periodic basis. If servicing does not take place, the timer times out. Upon timeout, WDOG signal is asserted. Configurable timeout counter with timeout periods from 0.5 to 128 seconds with Time resolution of 0.5 seconds.

For more details on Watchdog output pinout on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S145	WDT_TIME_ OUT#	WDT_OUT(GPIO 1_02)	GPIO1_IO02/ R4	O, 1.8V CMOS	Active Low Watchdog Timer Out.

2.8.10 USB 3.0 OTG Interface

The i.MX8M SMARC SOM supports one USB 3.0 OTG interface and one USB3.0 Host port on SMARC PCB Edge connector. Also it supports four USB2.0 Host interface on SMARC PCB Edge connector through On-SOM USB 2.0 four port hub.

i.MX8M CPU's USB OTG1 controller with integrated PHY is used for USB 3.0 OTG interface and directly connected to USB3 port of SMARC PCB Edge connector. This USB3.0 OTG is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports USB dual-role operation and can be configured as host or device. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

For more details on USB 3.0 OTG pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S37	USB3_VBUS_DET	VBUS_OTG	NA	I, Power	USB 3.0 OTG VBUS power for detection. *Note: Same power is also connected to P63rd pin through resistor and default not populated.*
S62	USB3_SSTX+	USB1_TX_P	USB1_TX_P/ A13	O, USB SS/ 0.1uf AC coupled	USB 3.0 OTG Super Speed Transmit Positive.
S63	USB3_SSTX-	USB1_TX_N	USB1_TX_N/ B13	O, USB SS/ 0.1uf AC coupled	USB 3.0 OTG Super Speed Transmit Negative.
S65	USB3_SSRX+	USB1_RX_P	USB1_RX_P/ A12	I, USB SS	USB 3.0 OTG Super Speed Receive Positive.
S66	USB3_SSRX-	USB1_RX_N	USB1_RX_N/ B12	I, USB SS	USB 3.0 OTG Super Speed Receive Negative.
S68	USB3+	USB_OTG1_DP	USB1_DP/ A14	IO, USB	USB 2.0 OTG High Speed Data Positive.
S69	USB3-	USB_OTG1_DM	USB1_DN/ B14	IO, USB	USB 2.0 OTG High Speed Data Negative.
P74	USB3_EN_OC#	GPIO_USB3_EN_OC(GPIO3_19)	SAI5_RXFS/ N4	I, 3.3V CMOS	USB OTG Power Enable/ Over Current Indicator.
S104	USB3_OTG_ID	USB_OTG1_ID	USB1_ID/ C14	I, 3.3V CMOS	USB OTG ID.

2.8.11 USB 3.0 Host Interface

The i.MX8M SMARC SOM supports one USB 3.0 Host interface on SMARC PCB Edge connector. i.MX8M CPU's USB OTG2 controller with integrated USB3.0 MAC & PHY is used for USB3.0 Host interface and directly connected to USB2 port of SMARC PCB Edge connector. This USB3.0 OTG controller is compliant with the Universal Serial Bus (USB) 3.0 Specifications which supports USB dual-role operation but configured as host only to match the SMARC specification of USB2 port. It supports Super Speed (5 Gbps), High Speed (480 Mbps), Full Speed (12 Mbps) and Low Speed (1.5 Mbps).

To support USB 2.0 Host interface on this USB3.0 Host Interface port, i.MX8M CPU's USB OTG2 controller with integrated USB 2.0 MAC & PHY is used. This USB2.0 PHY output is connected to USB2 port of SMARC PCB Edge connector through four-port USB hub "USB2514" from Microchip. The Hub is used to support more USB2.0 Host Ports on SMARC PCB Edge connector.

For more details on USB 3.0 Host pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P69	USB2+	USB_HUB2OUT_DP	NA	IO, USB	USB 2.0 Port2 Data Positive. *Note: This pin is connected from 4port USB Hub Out2.*
P70	USB2-	USB_HUB2OUT_DM	NA	IO, USB	USB 2.0 Port2 Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
P71	USB2_EN_OC#	USB_HUB2_OC	NA	I, 3.3V CMOS/ 10K PU	USB Port2 Power Enable/ Over Current Indicator. *Note: This pin is connected to USB Hub.*
S71	USB2_SSTX+	USB2_TX_P	USB2_TX_P/ A9	O, USB SS/ 0.1uf AC coupled	USB 3.0 Port2 Transmit Positive.
S72	USB2_SSTX-	USB2_TX_N	USB2_TX_N/ B9	O, USB SS/ 0.1uf AC coupled	USB 3.0 Port2 Transmit Negative.
S74	USB2_SSRX+	USB2_RX_P	USB2_RX_P/ A8	I, USB SS	USB 3.0 Port2 Receive Positive.
S75	USB2_SSRX-	USB2_RX_N	USB2_RX_N/ B8	I, USB SS	USB 3.0 Port2 Receive Negative.

2.8.12 USB 2.0 Host Interface

The i.MX8M SMARC SOM supports four USB2.0 Host interface on SMARC PCB Edge connector. To support four USB2.0 Host interfaces, SOM includes four-port USB hub "USB2514" from Microchip. This Hub is interfaced with i.MX8M CPU using USB OTG2 controller (with integrated PHY) which supports USB2.0 High-Speed (480 Mbps), Full-Speed (12 Mbps) and Low-Speed (1.5 Mbps) transfer. This Hub output is directly connected to USB1, USB2, USB4 & USB5 port of SMARC PCB Edge connector.

For more details on USB 2.0 Host pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P60	USB0+	USB_OTG1_ DP	USB1_DP/A14	IO, USB	Default NC. *Note: This pin is optionally connected from i.MX8M CPU USB1 Data Positive for USB 2.0 OTG through resistor and default not populated.* *Note: USB1 Data Positive is by default connected to S68th pin through resistor and default populated.*
P61	USB0-	USB_OTG1_ DM	USB1_DM/B14	IO, USB	Default NC. *Note: This pin is optionally connected from i.MX8M CPU USB1 Data Negative for USB 2.0 OTG through resistor and default not populated.* *Note: USB1 Data Negative is by default connected to S69th pin through resistor and default populated.*
P62	USB0_EN_OC#	USB3_EN_OC (GPIO3_19)	SAI5_RXFS/N4	IO, 3.3V CMOS	Default NC. *Note: This pin is optionally connected to GPIO3_19 through resistor and default not populated.*
P63	USB0_VBUS_DE T	VBUS_OTG	USB1_VBUS/D1 4	5V, Power	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's USB1_VBUS for VBUS detection through resistor and default not populated.*

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
					Note: Same power is also connected to SMARC Edge S37th pin through resistor and default populated.
P64	USB0_OTG_ID	USB_OTG1_ID	NA	I, 3.3V CMOS	Default NC. *Note: This pin is optionally connected to i.MX8M CPU's USB1_ID pin through resistor and default not populated.*
P65	USB1+	USB_HUB1OUT_DP	NA	IO, USB	USB 2.0 Port1 Data Positive. *Note: This pin is connected from 4port USB Hub Out1.*
P66	USB1-	USB_HUB1OUT_DM	NA	IO, USB	USB 2.0 Port1 Data Negative. *Note: This pin is connected from 4port USB Hub Out1.*
P67	USB1_EN_OC#	USB_HUB1_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port1 Over Current Indicator. *Note: This pin is connected to USB Hub OCS1 pin.*
P76	USB4_EN_OC#	USB_HUB3_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port3 Over Current Indicator. *Note: This pin is connected to USB Hub OCS3 pin.*
S35	USB4+	USB_HUB3OUT_DP	NA	IO, USB	USB 2.0 Port3 Data Positive. *Note: This pin is connected from 4port USB Hub Out3.*
S36	USB4-	USB_HUB3OUT_DM	NA	IO, USB	USB 2.0 Port3 Data Negative. *Note: This pin is connected from 4port USB Hub Out2.*
S55	USB5_EN_OC#	USB_HUB4_OC	NA	I, 3.3V CMOS/ 10K PU	USB 2.0 Port4 Over Current Indicator. *Note: This pin is connected to USB Hub OCS4 pin.*
S59	USB5+	USB_HUB4OUT_DP	NA	IO, USB	USB 2.0 Port4 Data Positive. *Note: This pin is connected from 4port USB Hub Out4.*
S60	USB5-	USB_HUB4OUT_DM	NA	IO, USB	USB 2.0 Port4 Data Negative. *Note: This pin is connected from 4port USB Hub Out4.*

2.8.13 PCIe Interface

The i.MX8M SMARC SOM supports one PCI Express Gen2.0 lane on SMARC PCB Edge connector. i.MX8M CPU's PCIe1 lane with integrated PHY is directly connected to PCIe Link A port of SMARC PCB Edge connector. 100MHz external clock oscillator output is connected to CPU & SMARC PCB Edge for PCIe reference clock. Also PCIe reset and PCIe wake are supported on SMARC PCB Edge connector from i.MX8M CPU IOs GPIO5_4 & GPIO5_5 respectively.

The i.MX8M CPU supports two PCI Express -2.0 Lanes. In that, PCIe1 lane is directly connected to PCIe Link A port of SMARC Edge connector in i.MX8M SMARC SOM. PCIe2 lane is connected to On-SOM PCIe to Ethernet controller by default, but option is provided to connect to PCIe Link B port of SMARC PCB edge connector.

Note: PCIe differential transmitter lines are ac coupled on SOM itself. Also PCIe differential clock lines from external clock oscillator are having On-SOM termination resistors and so no external termination is required.

For more details on PCIe1 pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P75	PCIE_A_RST#	GPIO_PCIE_RST(GPIO5_4)	SPDIF_RX/ G6	O, 3.3V CMOS	PCIe1 Reset Out.
P83	PCIE_A_REFCK+	PCIE1_REFCLK_P	NA	O, HCSL	PCIe1 Clock Positive.
P84	PCIE_A_REFCK+	PCIE1_REFCLK_N	NA	O, HCSL	PCIe1 Clock Negative.
P86	PCIE_A_RX+	PCIE1_RXP	PCIE1_RXN_P/ H25	I, PCIe	PCIe1 Receive Positive.
P87	PCIE_A_RX-	PCIE1_RXN	PCIE1_RXN_N/ H24	I, PCIe	PCIe1 Receive Negative.
P89	PCIE_A_TX+	PCIE1_TXP	PCIE1_TX0_P/ J25	O, PCIe/ 0.1uF AC Coupled	PCIe1 Transmit Positive.
P90	PCIE_A_TX+	PCIE1_TXN	PCIE1_TX0_N/ J24	O, PCIe/ 0.1uF AC Coupled	PCIe1 Transmit Negative.

For more details on PCIe2 pinouts on SMARC PCB edge connector, refer below table:

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S76	PCIE_B_RST#	NC	SPDIF_TX/ F6	O, 3.3V CMOS	Default NC. *Note: GPIO5_3 is optionally connected to this pin through resistor for PCIe2 reset and default not populated.*
S84	PCIE_B_REFCK+	NC	NA	O, HCSL	Default NC. *Note: 100MHz Clock Oscillator output for PCIe2 Clock Positive is optionally connected to this pin through resistor and default not populated.*
S85	PCIE_B_REFCK-	NC	NA	O, HCSL	Default NC. *Note: 100MHz Clock Oscillator output for PCIe2 Clock Negative is optionally connected to this pin through resistor and default not populated.*
S87	PCIE_B_RX+	NC	PCIE2_RXN_P/ D25	I, PCIe	Default NC. *Note: PCIe2 Receiver Positive is optionally connected to this pin through resistor and default not populated.*
S88	PCIE_B_RX-	NC	PCIE2_RXN_N/ D24	I, PCIe	Default NC. *Note: PCIe2 Receiver Negative is optionally connected to this pin through resistor and default not populated.*
S90	PCIE_B_TX+	NC	PCIE2_TX0_P/ E25	O, PCIe/ 0.1uF AC Coupled	Default NC. *Note: PCIe2 Transmitter Positive is optionally connected to this pin through capacitor and default not populated.*
S91	PCIE_B_TX-	NC	PCIE2_TX0_N/ E24	O, PCIe/ 0.1uF AC Coupled	Default NC. *Note: PCIe2 Transmitter Negative is optionally connected to this pin through capacitor and default not populated.*

2.8.14 Dual Gigabit Ethernet

The i.MX8M SMARC SOM supports two Gigabit Ethernet capable ports on SMARC PCB Edge connector. In that, First Ethernet Gigabit Ethernet0 (GBE0) port of SMARC PCB Edge connector is supported through i.MX8M CPU's ENET controller. The MAC is integrated in the i.MX8M CPU ENET and connected to the external Gigabit Ethernet PHY ""AR8031" from Atheros/Qualcomm on SOM through RGMII interface. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. i.MX8M SMARC SOM also supports Link and Activity indication LED control signals for GBE0 port to SMARC PCB Edge connector.

For more details on GBE0 pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P19	GBE0_MDI3-	GBE0_MDI3-	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 3 negative.
P20	GBE0_MDI3+	GBE0_MDI3+	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 3 positive.
P21	GBE0_LINK100#	GBE0_LINK100#	NA	O, 3.3V CMOS	100Mbps Ethernet link status LED.
P22	GBE0_LINK1000#	GBE0_LINK1000#	NA	O, 3.3V CMOS	Gigabit Ethernet link status LED.
P23	GBE0_MDI2-	GBE0_MDI2-	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 2 negative.
P24	GBE0_MDI2+	GBE0_MDI2+	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 2 positive.
P25	GBE0_LINK_ACT#	GBE0_LINK_ACT#	NA	O, 3.3V CMOS	Gigabit Ethernet activity status LED.
P26	GBE0_MDI1-	GBE0_MDI1-	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 1 negative.
P27	GBE0_MDI1+	GBE0_MDI1+	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 1 positive.
P28	GBE0_CTREF	VPHY0_DVDDL	NA	O, Power	Power for Centre Tap. *Note: It is not recommended to connect this power to centre tap of Magnetics.*
P29	GBE0_MDI0-	GBE0_MDI0-	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 0 negative.
P30	GBE0_MDI0+	GBE0_MDI0+	NA	IO, GBE MDI	Gigabit Ethernet MDI differential pair 0 positive.

Second Ethernet Gigabit Ethernet1 (GBE1) port of SMARC PCB Edge connector is supported through PCIe to Ethernet controller "RTL8119" from Realtek on SOM. This Ethernet controller is interfaced with i.MX8M CPU using PCIe2 Lane. This controller combines IEEE 802.3 compliant MAC and Ethernet transceiver. Since MAC and PHY are supported on SOM itself, only Magnetics are required on the carrier board. It also supports Link and Activity indication LED control signals to SMARC PCB Edge connector.

Note: In i.MX8M SMARC SOM, PCIe2 lane signals are having option to connect to PCIe to Ethernet controller and SMARC PCB Edge Connector. By default, PCIe2 is connected to PCIe to Ethernet controller.

For more details on GBE1 pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
S17	GBE1_MDI0+	GBE1_MDI0+	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 0 positive.
S18	GBE1_MDI0-	GBE1_MDI0-	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 0 negative.
S19	GBE1_LINK100#	GBE1_LINK100#	NA	O, 3.3V CMOS	100Mbps Link status LED.
S20	GBE1_MDI1+	GBE1_MDI1+	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 1 positive.
S21	GBE1_MDI1-	GBE1_MDI1-	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 1 negative.
S22	GBE1_LINK1000#	GBE1_LINK1000#	NA	O, 3.3V CMOS	1000Mbps Link status LED.
S23	GBE1_MDI2+	GBE1_MDI2+	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 2 positive.
S24	GBE1_MDI2-	GBE1_MDI2-	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair2 negative.
S26	GBE1_MDI3+	GBE1_MDI3+	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 3 positive.
S27	GBE1_MDI3-	GBE1_MDI3-	NA	IO, GBE MDI	Second Gigabit Ethernet MDI differential pair 3 negative.
S28	GBE1_CTREF	NC	NA	NC	NC.
S31	GBE1_LINK_ACT#	GBE1_LINK_ACT#	NA	O, 3.3V CMOS	Ethernet Activity status LED.

2.8.15 GPIO Interface

The i.MX8M SMARC SOM supports 12 GPIOs on SMARC PCB Edge connector as per SMARC V2.0 specification. i.MX8M CPU's The GPIO general-purpose input/output peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs.

When configured as an output, it is possible to write to an internal register to control the state driven on the output pin. When configured as an input, it is possible to detect the state of the input by reading the state of an internal register. In addition, the GPIO peripheral can produce CORE interrupts.

For more details on GPIO Interface pinouts on SMARC PCB edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P108	GPIO0/ CAM0_PWR#	SMARC_GPIO_0 (GPIO3_16)	NAND_READY_ B/K20	IO, 1.8V CMOS	General Purpose Input/Output 0.
P109	GPIO1/ CAM1_PWR#	SMARC_GPIO_1 (GPIO1_12)	GPIO1_IO12/ L7	IO, 1.8V CMOS	General Purpose Input/Output 1.
P110	GPIO2/ CAM0_RST#	SMARC_GPIO_2 (GPIO1_15)	GPIO1_IO15/ J6	IO, 1.8V CMOS	General Purpose Input/Output 2.
P111	GPIO3/ CAM1_RST#	SMARC_GPIO_3 (GPIO1_11)	GPIO1_IO11/ L6	IO, 1.8V CMOS	General Purpose Input/Output 3.
P112	GPIO4/ HDA_RST#	SMARC_GPIO_4 (GPIO1_10)	GPIO1_IO10/ M7	IO, 1.8V CMOS	General Purpose Input/Output 4.
P113	GPIO5/ PWM_OUT	SMARC_GPIO_5 (GPIO1_01)	GPIO1_IO01/ T7	IO, 1.8V CMOS	General Purpose Input/Output 5.
P114	GPIO6/ TACHIN	SMARC_GPIO_6 (GPIO1_09)	GPIO1_IO09/ M6	IO, 1.8V CMOS	General Purpose Input/Output 6.
P115	GPIO7	SMARC_GPIO_7 (GPIO1_06)	GPIO1_IO06/ N5	IO, 1.8V CMOS	General Purpose Input/Output 7.
P116	GPIO8	SMARC_GPIO_8 (GPIO1_08)	GPIO1_IO08/ N7	IO, 1.8V CMOS	General Purpose Input/Output 8.
P117	GPIO9	SMARC_GPIO_9 (GPIO1_03)	GPIO1_IO03/ P4	IO, 1.8V CMOS	General Purpose Input/Output 9.
P118	GPIO10	SMARC_GPIO_1 0(GPIO1_07)	GPIO1_IO07/ N6	IO, 1.8V CMOS	General Purpose Input/Output 10.
P119	GPIO11	SMARC_GPIO_1 1(GPIO1_04)	GPIO1_IO04/ P5	IO, 1.8V CMOS	General Purpose Input/Output 11.

2.8.16 Management Pins

The i.MX8M SMARC SOM supports Management pins as per SMARC V2.0 specification. For more details on supported Management Signals pinouts on SMARC PCB Edge connector and corresponding pin description, refer the below table.

Also i.MX8M SMARC SOM supports POWER_BTN# input from SMARC PCB Edge connector which is the active low signal and connected to i.MX8M CPU's ONOFF pin. This pin can be used to On/Off the i.MX8M CPU by connecting push button in the carrier board. When the board power is On, a button press between 750ms to 5s will send an interrupt to core to request software to bring down the i.MX8M safely (if software supports). Otherwise, button press greater than 5s results in a direct hardware power down which is applicable when software is unable to power Off the device. When the i.MX8M CPU power supply is Off, a button presses greater in duration than 750ms asserts an output signal to request power from a power IC to power up the i.MX8M CPU.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P126	RESET_OUT#	GPIO_RESET_OUT(GPIO3_25)	SAI5_MCLK/ K4	O, 1.8V CMOS	Reset OUT from CPU to carrier board. *Note: GPIO3_25 is connected to this pin as GPIO for implementing Reset Out.*
P127	RESET_IN#	RESET_IN#	NA	I, 1.8V CMOS 10K PU	RESET Input to SOM. *Note: This will restart the power cycle of SOM.*
P128	POWER_BTN#	POWER_BUTTON	ONOFF/ W21	I, 1.8V CMOS 100K PU	Power ON/OFF Input to SOM.
S150	VIN_PWR_BAD#	VIN_PWR_BAD#	NA	I, 5V CMOS	Power bad indication from Carrier board. Module and Carrier board power supplies shall not be enabled while this signal is held low by the Carrier board.
S153	CARRIER_STBY#	CARRIER_STBY#	NA	O, 1.8V CMOS/ 10K PU	Not supported. *Note: Only pullup is provided in the SOM.*
S154	CARRIER_PWR_ON	CARRIER_PWR_ON	NA	O, 1.8V CMOS/ 10K PU	Carrier board power should be enabled only after this pin goes High.
S157	TEST#	TEST#	NA	I, 1.8V CMOS	Not supported. *Note: This pin is connected to GND in SOM.*

2.8.17 Boot Select

The i.MX8M SMARC SOM supports three Boot Select pins as per SMARC V2.0 specification. i.MX8M SOM supports botting from On-SOM eMMC/MicroSD and SMARC SD (from carrier board). Any of these boot media can selected by properly setting the Boot Select Pins status from the carrier board as mentioned below.

Boot Select Pins			SOM Boot Media
BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0	
Float	Float	GND	eMMC Flash/Micro SD (uSDHC1) [1]
GND	GND	Float	SMARC SD (uSDHC2)

[1] *In i.MX8M SMARC SOM, uSDHC1interface signals are connected to both eMMC Flash and MicroSD connector. So either one feature only can be supported at a time in the SOM.*

Also i.MX8M SMARC SOM supports active low FORCE_RECOV# functionality as per SMARC V2.0 specification. By pulling low on this pin puts i.MX8M CPU in serial download mode where the CPU boot media can be programmed through i.MX8M CPU's USB1 controller USB 2.0 interface which is connected to USB3 port of SMARC PCB Edge connector.

For more details on Boot Select pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P123	BOOT_SEL0#	BOOT_SEL0#	NA	I, 1.8V CMOS 1K PU	Boot Media Select bit 0
P124	BOOT_SEL1#	BOOT_SEL1#	NA	I, 1.8V CMOS 1K PU	Boot Media Select bit 1
P125	BOOT_SEL2#	BOOT_SEL2#	NA	I, 1.8V CMOS 1K PU	Boot Media Select bit 2
S155	FORCE_RECOV#	FORCE_RECOV#	NA	I, 1.8V CMOS 10K PU	Active low Force Recovery Input.

2.8.18 Power and GND

The i.MX8M SMARC SOM works with 5V power input (VCC) from SMARC PCB Edge Connector and generates all other required powers internally On-SOM itself. i.MX8M SMARC SOM also supports coin cell power input (VDD_RTC) from SMARC PCB Edge Connector to On-SOM RTC controller for real time clock.

For more details on Power & GND Signals pinouts on SMARC PCB Edge connector, refer the below table.

SMARC Pin No.	SMARC Edge Pin Name	SMARC Edge Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
P147,P148,P149,P150, P151,P152,P153,P154, P155,P156	VDD_IN	VDD_IN	NA	I, 5V Power	Supply Voltage.
P2,P9,P12,P15,P18,P32, P38,P47,P50,P53,P59, P68,P79,P82,P85,P88, P91,P94,P97,P100, P103,P120,P133,P142, S3,S10,S13,S16,S25,S34, S47,S61,S64,S67,S70, S73,S80,S83,S86,S89, S92,S101,S110,S119, S124,S130,S136,S143, S158	GND	GND	NA	Power	Ground.
S147	VDD_RTC	VDD_RTC	NA	I, 3V Power	3V coin cell input for RTC.

2.9 Expansion Connector (Optional)

The i.MX8M SMARC SOM optionally supports one 100pin Expansion connector to utilise extra interfaces which is not covered under SMARC specification V2.0 PCB edge connector. The interfaces which are available at this connector is explained in the following sections. This connector is placed on bottom side of the SOM as shown below. This is the optional feature and not populated by default.

Number of Pins - : 100

Connector Part - : FX8C-100S-SV(68) from Hirose

Mating Connector - : FX8C-100P-SV(91) from Hirose

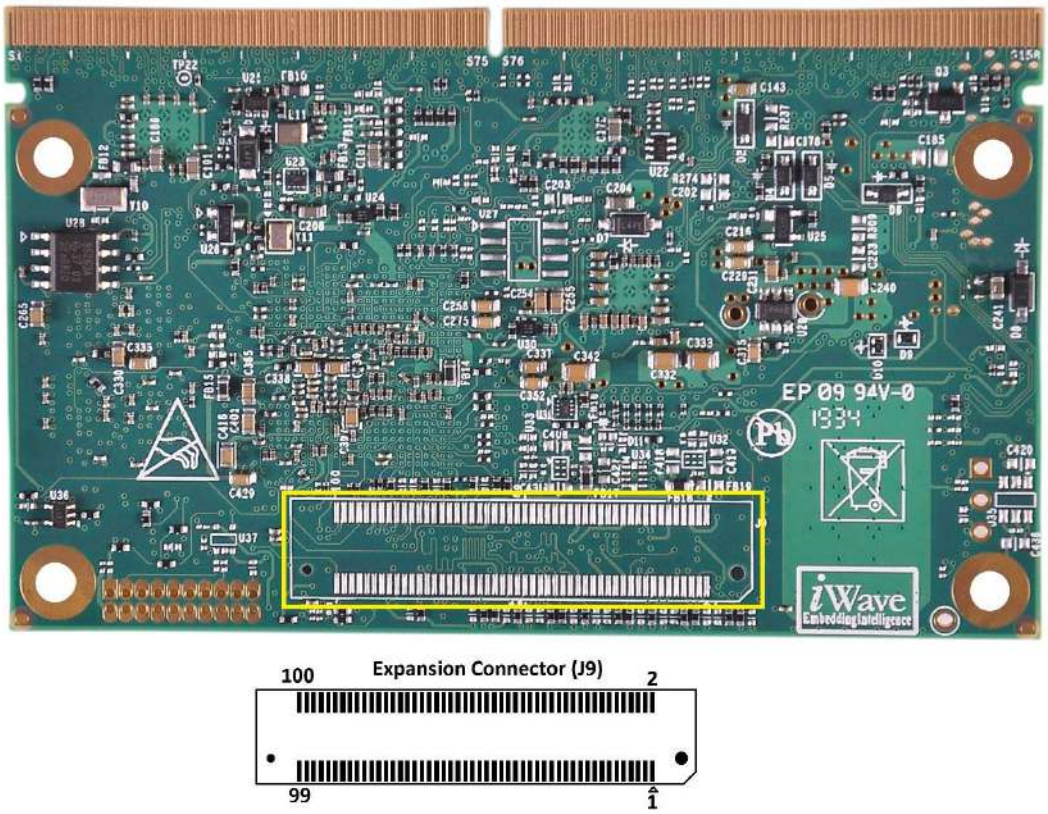

Figure 5: Expansion Connector

Table 4: Expansion Connector Pinouts

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
SAI1_TXD0[1]	1	2	NC
SAI1_TXD6[1]	3	4	NC
SAI1_TXD2[1]	5	6	GND
SAI1_TXD3[1]	7	8	NC
SAI1_TXD4[1]	9	10	NC
SAI1_TXD5[1]	11	12	GND
SAI1_TXD7[1]	13	14	NC
SAI1_TXD1[1]	15	16	NC
GND	17	18	GND
SAI1_TXFS	19	20	NC
SAI1_TXC	21	22	NC
GND	23	24	GND
NC	25	26	NC
NC	27	28	NC
GND	29	30	GND
NC	31	32	GPIO_BCONFIG_0(GPIO3_2)[3]
NC	33	34	NC
SAI1_RXD0[1,2]	35	36	GND
SAI1_RXD1[1,2]	37	38	NC
SAI1_RXD2[1]	39	40	NC
SAI1_RXD5[1]	41	42	NC
SAI1_RXD4[1]	43	44	NC
SAI1_RXD7[1]	45	46	NC
SAI1_RXD3[1]	47	48	NC
SAI1_RXFS	49	50	NC
GND	51	52	NC
SAI1_RXD6[1]	53	54	GND
SAI1_RXC	55	56	NC
GND	57	58	NC
NC	59	60	GND
NC	61	62	NC
NC	63	64	GPIO_BCONFIG_3(GPIO5_2)[3]
GND	65	66	GND
NC	67	68	GPIO_BCONFIG_2(GPIO4_29)[3]
NC	69	70	NC
NC	71	72	GND
NC	73	74	NC
GND	75	76	GPIO_BCONFIG_1(GPIO4_28)[3]
GPIO_BCONFIG_4(GPIO4_22)[3]	77	78	GND
NC	79	80	MIPI_CSI1_DATA2_P

Signal	Expansion Connector Pin	Expansion Connector Pin	Signal
NC	81	82	MIPI_CSI1_DATA2_N
GND	83	84	GND
NC	85	86	MIPI_CSI1_DATA3_P
NC	87	88	MIPI_CSI1_DATA3_N
NC	89	90	GND
NC	91	92	GPIO_BCONFIG_5(GPIO4_21)[3]
NC	93	94	HDMI_CEC[2]
NC	95	96	NC
NC	97	98	CLK1_P
GPIO_BCONFIG_6(GPIO3_14)[3]	99	100	CLK1_N

[1] These signals are also used for i.MX8M CPU boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration.

[2] Optional feature, by default not supported.

[3] These signals are also used for SOM Board configuration number setting and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the configuration number read. If SOM configuration number read is not required, then above restriction need not be considered.

2.9.1 SAI Interface

The i.MX8M SMARC SOM supports Synchronous Audio Interface (SAI) interface on Expansion Connector. i.MX8M CPU's SAI1 module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces. If any of these pins are not used as SAI1 interface, the same pins can be used as GPIO with interrupt capability if required.

For more details on SAI1 pinouts on Expansion connector, refer the below table.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
1	SAI1_TXD0[1]	SAI1_TXD0/ F2	O, 1.8V CMOS/ 10K PD	SAI1 Transmit Data 0.
15	SAI1_TXD1[1]	SAI1_TXD1/ E2	O, 1.8V CMOS/ 10K PD	SAI1 Transmit Data 1.
5	SAI1_TXD2[1]	SAI1_TXD2/ B2	O, 1.8V CMOS/ 10K PD/1K PU	SAI1 Transmit Data 2. *Note: Termination will differ based on boot media selection.*
7	SAI1_TXD3[1]	SAI1_TXD3/ D1	O, 1.8V CMOS/ 10K PD	SAI1 Transmit Data 3.
9	SAI1_TXD4[1]	SAI1_TXD4/ D2	O, 1.8V CMOS/ 10K PD/1K PU	SAI1 Transmit Data 4. *Note: Termination will differ based on boot media selection.*
11	SAI1_TXD5[1]	SAI1_TXD5/ C2	O, 1.8V CMOS/ 10K PD/1K PU	SAI1 Transmit Data 5. *Note: Termination will differ based on boot media selection.*
3	SAI1_TXD6[1]	SAI1_TXD6/ B3	O, 1.8V CMOS/ 10K PD/1K PU	SAI1 Transmit Data 6. *Note: Termination will differ based on boot media selection.*
13	SAI1_TXD7[1]	SAI1_TXD7/ C1	O, 1.8V CMOS/ 10K PD	SAI1 Transmit Data 7.
19	SAI1_TXFS	SAI1_TXFS/ H1	O, 1.8V CMOS	SAI1 Transmit Frame Sync Output.
21	SAI1_TXC	SAI1_TXC/ E1	O, 1.8V CMOS	SAI1 Transmit Clock Input.
35	NC	SAI1_RXD0/ K2	O, 1.8V CMOS/ 10K PD/1K PU	Default NC. *Note: SAI1_RXD0 is optionally connected to this pin through resistor and default not populated.*
37	NC	SAI1_RXD1/ L2	O, 1.8V CMOS/ 10K PD/1K PU	Default NC. *Note: SAI1_RXD1 is optionally connected to this pin through resistor and default not populated.*

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
39	SAI1_RXD2[1]	SAI1_RXD2/ H2	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 2.
47	SAI1_RXD3[1]	SAI1_RXD3/ J2	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 3.
43	SAI1_RXD4[1]	SAI1_RXD4/ J1	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 4.
41	SAI1_RXD5[1]	SAI1_RXD5/ F1	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 5.
53	SAI1_RXD6[1]	SAI1_RXD6/ G2	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 6.
45	SAI1_RXD7[1]	SAI1_RXD7/ G1	I, 1.8V CMOS/ 10K PD	SAI1 Receiver Data 7.
49	SAI1_RXFS	SAI1_RXFS/ L1	I, 1.8V CMOS	SAI1 Receiver Frame Sync Output.
55	SAI1_RXC	SAI1_RXC/ K1	I, 1.8V CMOS	SAI1 Receiver Clock Input.

[1] Important Note: These signals are also used for i.MX8M CPU boot media setting on SOM and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the boot configuration.

2.9.2 MIPI CSI Camera Interface

The i.MX8M CPU supports two four lane MIPI CSI camera interface whereas SMARC PCB Edge connector supports one two lane and one four lane MIPI CSI. Hence 2nd and 3rd Data lane of MIPI CSI0 is connected to SOM Expansion connector.

For more details on MIPI CSI0 pinouts on Expansion connector, refer the below table.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
80	MIPI_CSI1_DATA2_P	MIPI_CSI1_D2_P/ C23	I, MIPI	MIPI CSI1 differential data lane 2 positive.
82	MIPI_CSI1_DATA2_N	MIPI_CSI1_D2_N/ B24	I, MIPI	MIPI CSI1 differential data lane 2 negative.
86	MIPI_CSI1_DATA3_P	MIPI_CSI1_D3_P/ D21	I, MIPI	MIPI CS1 differential data lane 3 positive.
88	MIPI_CSI1_DATA3_N	MIPI_CSI1_D3_N/ C21	I, MIPI	MIPI CSI1 differential data lane 3 negative.

2.9.3 Miscellaneous Signals

The i.MX8M SMARC SOM Expansion Connector includes the remaining signals from i.MX8M CPU which is not used in any other place in the SOM. For more details on these signals' pinout on Expansion connector, refer the below table.

Exp. Pin No	Signal Name	CPU Ball Name/ Pin Number	Signal Type/ Termination	Description
32	GPIO_BCONFIG_0(GPIO3_2)*	NAND_CE1_B/ G21	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
64	GPIO_BCONFIG_3(GPIO5_2)*	SAI3_MCLK/ D3	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
68	GPIO_BCONFIG_2(GPIO4_29)*	SAI3_RXC/ F4	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
76	GPIO_BCONFIG_1(GPIO4_28)*	SAI3_RXFS/ G4	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
77	GPIO_BCONFIG_4(GPIO4_22)*	SAI2_RXC/ H3	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
92	GPIO_BCONFIG_5(GPIO4_21)*	SAI2_RXFS/ J4	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
99	GPIO_BCONFIG_6(GPIO3_14)*	NAND_DQS/ M20	IO, 1.8V CMOS/ 10K PD/10K PU	General Purpose Input/Output. *Note: Termination will differ based on SOM configuration number setting.*
94	HDMI_CEC	HDMI_CEC/ W3	IO, 1.8V CMOS	HDMI CEC *Note: By default not populated.*
98	CLK1_P	CLK1_P/ R23	I, 1.8V LVDS/ 100 ohm Differential termination	Reference Clock Input to PLL.
100	CLK1_N	CLK1_N/ T23	I, 1.8V LVDS/ 100 ohm Differential termination	Reference Clock Input to PLL.

** These signals are also used for SOM configuration number setting and so no external loads or pull-up/pull-down resistors to be connected to these pins which will change the SOM configuration number read. If SOM configuration number read is not required, then above restriction need not be considered.*

2.10 Fan Header

The i.MX8M SMARC SOM supports a Fan Header to connect cooling Fan if required. This Fan Header (J2) is physically located at the top of the board as shown below.

Number of Pins - 2

Connector Part - 0530480210 from Molex

Mating Connector - 51021-0200 from Molex

Figure 6: FAN Header

Table 5: FAN Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_5V	O, Power	+5V Power output to FAN.
2	GND	Power	Ground.

2.11 Optional Features

2.11.1 JTAG Header

The i.MX8M SMARC SOM optionally supports JTAG interface for CPU debug purpose. A customized 20-pin ARM JTAG connector (J5) is available in SOM for JTAG interface. The i.MX8M CPU's JTAG pins are 1.8V tolerant and so 1.8V reference power is provided to pin1 of the connector to allow JTAG tool to automatically configure the logic signals for the right voltage. JTAG connector (J5) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Number of Pins - 20

Connector Part - GRPB102MWCN-RC from Sullins Connector Solutions

Mating Connector - LPPB102CFFN-RC from Sullins Connector Solutions

Table 6: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VDD_1V8	O, 1.8V Power	VTREF Voltage Reference.
2	VDD_1V8	O, 1.8V Power	Supply Voltage.
3	JTAG_TRST_B	I, 1.8V CMOS/ 10K PU	JTAG test reset signal.
4	GND	Power	Ground.
5	JTAG_TDI	I, 1.8V CMOS/ 10K PU	JTAG test data input.
6	GND	Power	Ground.
7	JTAG_TMS	I, 1.8V CMOS/ 10K PD	JTAG test mode select.
8	GND	Power	Ground.
9	JTAG_TCK	I, 1.8V CMOS/ 10K PD	JTAG test Clock. *Note: optionally 10K pull up is provided.*
10	GND	Power	Ground.
11	-	-	Only pull down is provided.
12	GND	Power	Ground.
13	JTAG_TDO	O, 1.8V CMOS/ 10K PU	JTAG test data output.
14	GND	Power	Ground.
15	RESET_IN#	O, 1.8V CMOS/ 10K PU	Reset output.
16	GND	Power	Ground.
17	-	-	Only pull up is provided.
18	GND	Power	Ground.

19	JTAG_MOD	O, 1.8V CMOS/ 10K PD	JTAG Mode select out.
20	GND	Power	Ground.

2.11.2 Debug UART Header

The i.MX8M SMARC SOM optionally supports 3pin UART header for i.MX8M CPU's debug purpose. The i.MX8M CPU's UART1 can be connected to this header via 1.8 to 3.3 voltage level translator. FTDI's UART to USB smart cable (*TTL-232R-RPI)* can be directly connected between this header and Host PC for debugging. This UART header (J3) is physically located on topside of the SOM. This is the optional feature and not populated by default.

Table 7: Debug UART Header Pin Out

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	UART1_TXD	UART1_TXD / A7	O, 1.8V CMOS	Debug UART Transmitter
2	UART1_RXD	UART1_RXD/ C7	I, 1.8V CMOS	Debug UART Receiver.
3	GND	GND	Power	Ground

2.11.3 Power IN Connector

The i.MX8M SMARC SOM works with +5V power input from SMARC PCB Edge connector. Optionally SOM can be powered up using Power IN Connector (P1) for standalone purpose. This is the optional feature and not populated by default.

Figure 7: Power IN Connector

2.12 i.MX8M PinMultiplexing on SMARC Edge

The i.MX8M CPU IO pins have many alternate functions and can be configured to any one of the alternate functions based on the requirement. Also most of the i.MX8M CPU's IO pins can be configured as GPIO if required. The below table provides the details of i.MX8M CPU pin connections to the SMARC edge connector and with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX8M Hardware User's Manual.

Important Note: It is strongly recommended to use the pin function same as selected in the SMARC SOM Edge connector for iWave's BSP reusability and to have compatible SMARC modules in future for upgradability.

Table 8: i.MX8M CPU IOMUX for SMARC Edge Connector interfaces

Interface/ Function	SMARC Edge Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
MIPI CSI0	S9	A22	MIPI_CSI1_CLK_N							MIPI_CSI1_CLK_N
	S8	B22	MIPI_CSI1_CLK_P							MIPI_CSI1_CLK_P
	S12	A23	MIPI_CSI1_D0_N							MIPI_CSI1_D0_N
	S11	B23	MIPI_CSI1_D0_P							MIPI_CSI1_D0_P
	S15	C22	MIPI_CSI1_D1_N							MIPI_CSI1_D1_N
	S14	D22	MIPI_CSI1_D1_P							MIPI_CSI1_D1_P
	S6	A3	SAI1_MCLK	SAI5_MCLK	SAI1_TX_BCLK			GPIO4_IO20		GPIO4.IO[20]
	S5	G8	I2C3_SCL	PWM4_OUT	GPT2_CLK			GPIO5_IO18		GPIO5.IO[18]
	S7	E9	I2C3_SDA	PWM3_OUT	GPT3_CLK			GPIO5_IO19		GPIO5.IO[19]
MIPI CSI1	P4	A19	MIPI_CSI2_CLK_N							MIPI_CSI2_CLK_N
	P3	B19	MIPI_CSI2_CLK_P							MIPI_CSI2_CLK_P
	P8	C20	MIPI_CSI2_D0_N							MIPI_CSI2_D0_N
	P7	D20	MIPI_CSI2_D0_P							MIPI_CSI2_D0_P
	P11	A20	MIPI_CSI2_D1_N							MIPI_CSI2_D1_N
	P10	B20	MIPI_CSI2_D1_P							MIPI_CSI2_D1_P
	P14	A21	MIPI_CSI2_D2_N							MIPI_CSI2_D2_N
	P13	B21	MIPI_CSI2_D2_P							MIPI_CSI2_D2_P
	P17	C19	MIPI_CSI2_D3_N							MIPI_CSI2_D3_N

Interface/ Function	SMARC Edge Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	P16	D19	MIPI_CSI2_D3_P							MIPI_CSI2_D3_P
	S1	E7	I2C1_SCL	ENET1_MDC				GPIO5_IO14		GPIO5.IO[14]
	S2	E8	I2C1_SDA	ENET1_MDIO				GPIO5_IO15		GPIO5.IO[15]
MIPI DSI0	S135	C16	MIPI_DSI_CLK_N							MIPI_DSI_CLK_N
	S134	D16	MIPI_DSI_CLK_P							MIPI_DSI_CLK_P
	S126	A17	MIPI_DSI_D0_N							MIPI_DSI_D0_N
	S125	B17	MIPI_DSI_D0_P							MIPI_DSI_D0_P
	S129	A16	MIPI_DSI_D1_N							MIPI_DSI_D1_N
	S128	B16	MIPI_DSI_D1_P							MIPI_DSI_D1_P
	S132	A18	MIPI_DSI_D2_N							MIPI_DSI_D2_N
	S131	B18	MIPI_DSI_D2_P							MIPI_DSI_D2_P
	S138	A15	MIPI_DSI_D3_N							MIPI_DSI_D3_N
	S137	B15	MIPI_DSI_D3_P							MIPI_DSI_D3_P
	S139	F8	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B			GPIO5_IO20		GPIO5.IO[20]
	S140	F9	I2C4_SDA	PWM1_OUT	PCIE2_CLKREQ_B			GPIO5_IO21		GPIO5.IO[21]
	S141	K7	GPIO1_IO14	USB2_OTG_PWR				PWM3_OUT	CCM_CLKO1	GPIO1.IO[14]
HDMI	P102	M2	HDMI_TX_M_LN_3							HDMI_TX_M_LN_3
	P101	M1	HDMI_TX_P_LN_3							HDMI_TX_P_LN_3
	P99	T2	HDMI_TX_M_LN_0							HDMI_TX_M_LN_0
	P98	T1	HDMI_TX_P_LN_0							HDMI_TX_P_LN_0
	P96	U1	HDMI_TX_M_LN_1							HDMI_TX_M_LN_1
	P95	U2	HDMI_TX_P_LN_1							HDMI_TX_P_LN_1
	P93	N1	HDMI_TX_M_LN_2							HDMI_TX_M_LN_2
	P92	N2	HDMI_TX_P_LN_2							HDMI_TX_P_LN_2
	P104	W2	HDMI_HPD							HDMI_HPD
	P105	R3	HDMI_DDC_SCL							HDMI_DDC_SCL
	P106	P3	HDMI_DDC_SDA							HDMI_DDC_SDA
SD Interface (Optional)	P36	L22	USDHC2_CLK					GPIO2_IO13		GPIO2.IO[13]
	P34	M22	USDHC2_CMD					GPIO2_IO14		GPIO2.IO[14]
	P39	N22	USDHC2_DATA0					GPIO2_IO15		GPIO2.IO[15]

Interface/ Function	SMARC Edge Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	P40	N21	USDHC2_DATA1					GPIO2_IO16		GPIO2.IO[16]
	P41	P22	USDHC2_DATA2					GPIO2_IO17		GPIO2.IO[17]
	P42	P21	USDHC2_DATA3					GPIO2_IO18		GPIO2.IO[18]
	P37	R22	USDHC2_RESET_B					GPIO2_IO19		GPIO2.IO[19]
	P35	L21	USDHC2_CD_B					GPIO2_IO12		GPIO2.IO[12]
QSPI	P54	F21	RAWNAND_CE2_B	QSPI_B_SS0_B				GPIO3_IO03		GPIO3.IO[3]
	P55	H20	RAWNAND_CE3_B	QSPI_B_SS1_B				GPIO3_IO04		GPIO3.IO[4]
	P56	H21	RAWNAND_CLE	QSPI_B_SCLK				GPIO3_IO05		GPIO3.IO[5]
	S58	K19	RAWNAND_RE_B	QSPI_B_DQS				GPIO3_IO15		GPIO3.IO[15]
	S56	L19	RAWNAND_DATA06	QSPI_B_DATA2				GPIO3_IO12		GPIO3.IO[12]
	S57	M19	RAWNAND_DATA07	QSPI_B_DATA3				GPIO3_IO13		GPIO3.IO[13]
	P58	J22	RAWNAND_DATA05	QSPI_B_DATA1				GPIO3_IO11		GPIO3.IO[11]
	P57	L20	RAWNAND_DATA04	QSPI_B_DATA0				GPIO3_IO10		GPIO3.IO[10]
SPI	P44	D5	ECSPI1_SCLK	UART3_RX				GPIO5_IO06		GPIO5.IO[6]
	P45	B4	ECSPI1_MISO	UART3_CTS_B				GPIO5_IO08		GPIO5.IO[8]
	P46	A4	ECSPI1_MOSI	UART3_TX				GPIO5_IO07		GPIO5.IO[7]
	P43	D4	ECSPI1_SS0	UART3_RTS_B				GPIO5_IO09		GPIO5.IO[9]
USB3	P74	N4	SAI5_RX_SYNC	SAI1_TX_DATA0				GPIO3_IO19		GPIO3.IO[19]
	S104	C14	USB1_ID							USB1_ID
	S68	A14	USB1_DP							USB1_DP
	S69	B14	USB1_DN							USB1_DN
	S62	A13	USB1_TX_P							USB1_TX_P
	S63	B13	USB1_TX_N							USB1_TX_N
	S65	A12	USB1_RX_P							USB1_RX_P
	S66	B12	USB1_RX_N							USB1_RX_N
PCIe1	P89	J25	PCIE1_TXN_P							PCIE1_TXN_P
	P90	J24	PCIE1_TXN_N							PCIE1_TXN_N
	P86	H25	PCIE1_RXN_P							PCIE1_RXN_P
	P87	H24	PCIE1_RXN_N							PCIE1_RXN_N
	P75	G6	SPDIF1_IN	PWM2_OUT				GPIO5_IO04		GPIO5.IO[4]
	S146	E6	SPDIF1_EXT_CLK	PWM1_OUT				GPIO5_IO05		GPIO5.IO[5]
	S90	E25	PCIE2_TXN_P							PCIE2_TXN_P

Interface/ Function	SMARC Edge Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
PCIe2 (Optional)	S91	E24	PCIE2_TXN_N							PCIE2_TXN_N
	S87	D25	PCIE2_RXN_P							PCIE2_RXN_P
	S88	D24	PCIE2_RXN_N							PCIE2_RXN_N
UART SER0	P130	B6	UART2_RX	ECSPI3_MISO				GPIO5_IO24		GPIO5.IO[24]
	P129	D6	UART2_TX	ECSPI3_SS0				GPIO5_IO25		GPIO5.IO[25]
	P131	C6	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B			GPIO5_IO28		GPIO5.IO[28]
	P132	D7	UART4_TX	UART2_RTS_B	PCIE2_CLKREQ_B			GPIO5_IO29		GPIO5.IO[29]
UART SER1	P134	B7	UART3_TX	UART1_RTS_B				GPIO5_IO27		GPIO5.IO[27]
	P135	A6	UART3_RX	UART1_CTS_B				GPIO5_IO26		GPIO5.IO[26]
UART SER2 (Optional)	P136	E5	ECSPI2_MOSI	UART4_TX				GPIO5_IO11		GPIO5.IO[11]
	P137	C5	ECSPI2_SCLK	UART4_RX				GPIO5_IO10		GPIO5.IO[10]
	P138	B5	ECSPI2_MISO	UART4_CTS_B				GPIO5_IO12		GPIO5.IO[12]
	P139	A5	ECSPI2_SS0	UART4_RTS_B				GPIO5_IO13		GPIO5.IO[13]
UART SER3	P141	C7	UART1_RX	ECSPI3_SCLK				GPIO5_IO22		GPIO5.IO[22]
	P140	A7	UART1_TX	ECSPI3_MOSI				GPIO5_IO23		GPIO5.IO[23]
Audio SAI0	S52	F3	SAI3_RX_DATA0	GPT1_COMPARE1	SAI5_RX_DATA0			GPIO4_IO30		GPIO4.IO[30]
	S53	C4	SAI3_TX_BCLK	GPT1_COMPARE2	SAI5_RX_DATA2			GPIO5_IO00		GPIO5.IO[0]
	S50	G3	SAI3_TX_SYNC	GPT1_CLK	SAI5_RX_DATA1			GPIO4_IO31		GPIO4.IO[31]
	S51	C3	SAI3_TX_DATA0	GPT1_COMPARE3	SAI5_RX_DATA3			GPIO5_IO01		GPIO5.IO[1]
Audio SAI1	S41	H6	SAI2_RX_DATA0	SAI5_TX_DATA0				GPIO4_IO23		GPIO4.IO[23]
	S42	J5	SAI2_TX_BCLK	SAI5_TX_DATA2				GPIO4_IO25		GPIO4.IO[25]
	S40	G5	SAI2_TX_DATA0	SAI5_TX_DATA3				GPIO4_IO26		GPIO4.IO[26]
	S39	H4	SAI2_TX_SYNC	SAI5_TX_DATA1				GPIO4_IO24		GPIO4.IO[24]
	S38	H5	SAI2_MCLK	SAI5_MCLK				GPIO4_IO27		GPIO4.IO[27]
GPIO	P108	K20	RAWNAND_READY_B					GPIO3_IO16		GPIO3.IO[16]
	P109	L7	GPIO1_IO12	USB1_OTG_PWR				SDMA2_EXT_EVENT1		GPIO1.IO[12]
	P110	J6	GPIO1_IO15	USB2_OTG_OC				PWM4_OUT	CCM_CLKO2	GPIO1.IO[15]
	P111	L6	GPIO1_IO11	USB2_OTG_ID				CCM_PMIC_READY		GPIO1.IO[11]
	P112	M7	GPIO1_IO10	USB1_OTG_ID						GPIO1.IO[10]

Interface/ Function	SMARC Edge Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	P113	T7	GPIO1_IO01	PWM1_OUT				ANAMIX_REF_CLK_24M	CCM_EXT_CLK2	GPIO1.IO[1]
	P114	M6	GPIO1_IO09	ENET1_1588_EVENT0_OUT				SDMA2_EXT_EVENT0		GPIO1.IO[9]
	P115	N5	GPIO1_IO06	ENET1_MDC				USDHC1_CD_B	CCM_EXT_CLK3	GPIO1.IO[6]
	P116	N7	GPIO1_IO08	ENET1_1588_EVENT0_IN				USDHC2_RESET_B		GPIO1.IO[8]
	P117	P4	GPIO1_IO03	USDHC1_VSELECT				SDMA1_EXT_EVENT0		GPIO1.IO[3]
	P118	N6	GPIO1_IO07	ENET1_MDIO				USDHC1_WP	CCM_EXT_CLK4	GPIO1.IO[7]
	P119	P5	GPIO1_IO04	USDHC2_VSELECT				SDMA1_EXT_EVENT1		GPIO1.IO[4]
I2C	S48	G7	I2C2_SCL	ENET1_1588_EVENT1_IN				GPIO5_IO16		GPIO5.IO[16]
	S49	F7	I2C2_SDA	ENET1_1588_EVENT1_OUT				GPIO5_IO17		GPIO5.IO[17]
Watchdog	S145	R4	GPIO1_IO02	WDOG1_WDOG_B				WDOG1_WDOG_ANY		GPIO1.IO[2]
Management Signals	P126	K4	SAI5_MCLK	SAI1_TX_BCLK	SAI4_MCLK			GPIO3_IO25		GPIO3.IO[25]
	P128	W21	ONOFF							ONOFF

2.13 i.MX8M Pin Multiplexing on Expansion Connector

The below table provides the details of i.MX8M Processor pin connections to the Expansion connector with selected pin function highlighted and available alternate functions. This table has been prepared by referring NXP's i.MX8M Hardware User's Manual.

Table 9: i.MX8M Pin Multiplexing on Expansion Connector interfaces

Interface/ Function	Expan. Conn. Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
SAI1	49	L1	SAI1_RX_SYNC	SAI5_RX_SYNC			CORESIGHT_TRACE_CLK	GPIO4_IO00		GPIO4.IO[0]
	55	K1	SAI1_RX_BCLK	SAI5_RX_BCLK			CORESIGHT_TRACE_CTL	GPIO4_IO01		GPIO4.IO[1]
	35	K2	SAI1_RX_DATA0	SAI5_RX_DATA0			CORESIGHT_TRACE0	GPIO4_IO02	SRC_BOOT_CFG 0	GPIO4.IO[2]
	37	L2	SAI1_RX_DATA1	SAI5_RX_DATA1			CORESIGHT_TRACE1	GPIO4_IO03	SRC_BOOT_CFG 1	GPIO4.IO[3]
	39	H2	SAI1_RX_DATA2	SAI5_RX_DATA2			CORESIGHT_TRACE2	GPIO4_IO04	SRC_BOOT_CFG 2	GPIO4.IO[4]
	47	J2	SAI1_RX_DATA3	SAI5_RX_DATA3			CORESIGHT_TRACE3	GPIO4_IO05	SRC_BOOT_CFG 3	GPIO4.IO[5]
	43	J1	SAI1_RX_DATA4	SAI6_TX_BCLK	SAI6_RX_BCLK		CORESIGHT_TRACE4	GPIO4_IO06	SRC_BOOT_CFG 4	GPIO4.IO[6]
	41	F1	SAI1_RX_DATA5	SAI6_TX_DATA0	SAI6_RX_DATA0	SAI1_RX_SYNC	CORESIGHT_TRACE5	GPIO4_IO07	SRC_BOOT_CFG 5	GPIO4.IO[7]
	53	G2	SAI1_RX_DATA6	SAI6_TX_SYNC	SAI6_RX_SYNC		CORESIGHT_TRACE6	GPIO4_IO08	SRC_BOOT_CFG 6	GPIO4.IO[8]
	45	G1	SAI1_RX_DATA7	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA4	CORESIGHT_TRACE7	GPIO4_IO09	SRC_BOOT_CFG 7	GPIO4.IO[9]
	19	H1	SAI1_TX_SYNC	SAI5_TX_SYNC			CORESIGHT_EVENTO	GPIO4_IO10		GPIO4.IO[10]
	21	E1	SAI1_TX_BCLK	SAI5_TX_BCLK			CORESIGHT_EVENTI	GPIO4_IO11		GPIO4.IO[11]

Interface/ Function	Expan. Conn. Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
	1	F2	SAI1_TX_DATA0	SAI5_TX_DATA0			CORESIGHT_TRACE8	GPIO4_IO12	SRC_BOOT_CFG8	GPIO4.IO[12]
	15	E2	SAI1_TX_DATA1	SAI5_TX_DATA1			CORESIGHT_TRACE9	GPIO4_IO13	SRC_BOOT_CFG9	GPIO4.IO[13]
	5	B2	SAI1_TX_DATA2	SAI5_TX_DATA2			CORESIGHT_TRACE10	GPIO4_IO14	SRC_BOOT_CFG10	GPIO4.IO[14]
	7	D1	SAI1_TX_DATA3	SAI5_TX_DATA3			CORESIGHT_TRACE11	GPIO4_IO15	SRC_BOOT_CFG11	GPIO4.IO[15]
	9	D2	SAI1_TX_DATA4	SAI6_RX_BCLK	SAI6_TX_BCLK		CORESIGHT_TRACE12	GPIO4_IO16	SRC_BOOT_CFG12	GPIO4.IO[16]
	11	C2	SAI1_TX_DATA5	SAI6_RX_DATA0	SAI6_TX_DATA0		CORESIGHT_TRACE13	GPIO4_IO17	SRC_BOOT_CFG13	GPIO4.IO[17]
	3	B3	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		CORESIGHT_TRACE14	GPIO4_IO18	SRC_BOOT_CFG14	GPIO4.IO[18]
	13	C1	SAI1_TX_DATA7	SAI6_MCLK			CORESIGHT_TRACE15	GPIO4_IO19	SRC_BOOT_CFG15	GPIO4.IO[19]
MIPI CSI0	80	C23	MIPI_CSI1_D2_P							MIPI_CSI1_D2_P
	82	B24	MIPI_CSI1_D2_N							MIPI_CSI1_D2_N
	86	D21	MIPI_CSI1_D3_P							MIPI_CSI1_D3_P
	88	C21	MIPI_CSI1_D3_N							MIPI_CSI1_D3_N
GPIO	32	G21	RAWNAND_CE1_B	QSPI_A_SS1_B				GPIO3_IO02		GPIO3.IO[2]
	64	D3	SAI3_MCLK	PWM4_OUT	SAI5_MCLK			GPIO5_IO02		GPIO5.IO[2]
	68	F4	SAI3_RX_BCLK	GPT1_CAPTURE2	SAI5_RX_BCLK			GPIO4_IO29		GPIO4.IO[29]
	76	G4	SAI3_RX_SYNC	GPT1_CAPTURE1	SAI5_RX_SYNC			GPIO4_IO28		GPIO4.IO[28]
	77	H3	SAI2_RX_BCLK	SAI5_TX_BCLK				GPIO4_IO22		GPIO4.IO[22]
	92	J4	SAI2_RX_SYNC	SAI5_TX_SYNC				GPIO4_IO21		GPIO4.IO[21]
	99	M20	RAWNAND_DQS	QSPI_A_DQS				GPIO3_IO14		GPIO3.IO[14]

Interface/ Function	Expan. Conn. Pin Number	i.MX8M CPU Pin Number	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Default State
Misc.	94	W3	HDMI_CEC							HDMI_CEC
	98	R23	CLK1_P							CLK1_P
	100	T23	CLK1_N							CLK1_N

3. TECHNICAL SPECIFICATION

This section provides detailed information about the i.MX8M SMARC SOM technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Electrical Characteristics

The Module input power voltage is brought in on the ten VDD_IN pins and returned through the numerous GND pins on the connector. A Module will withstand an indefinite exposure to an applied VDD_IN that may vary over the 4.5V to 5.25V range, without damage, and it will operate over the entire VDD_IN range of 4.5V to 5.25V. Ten pins are allocated to VDD_IN. The connector pin current rating is 0.5A per pin. This works out to 5A total for the 10 pins.

3.1.1 Power Input Requirement

The below table provides the Power Input Requirement of i.MX8M SMARC SOM.

Table 10: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VDD_IN [1]	4.75V	5V	5.25V	±50mV
2	VDD_RTC [2]	2.8V	3V	3.3V	±20mV

[1] *i.MX8M SMARC SOM is designed to work with VDD_IN input power rail from SMARC PCB Edge connector. Optionally we can use On-SOM Power In connector to feed VDD_IN which can be used only for SOM standalone power up.*

[2] *i.MX8M SMARC SOM use this voltage as backup power source to RTC controller when VDD_IN is off.*

3.1.2 Power Input Sequencing

The i.MX8M SMARC SOM's Power Input sequence requirement is explained below.

Power up Sequence:

- VDD_RTC must come up at the same time or before VDD_IN comes up.
- VIN_PWR_BAD# signal from SMARC Edge must be active at the same time or after VDD_IN comes up.
- After VDD_IN comes up and all On-SOM power is stable, CARRIER_PWR_ON signal will be pulled high by SOM to enable the carrier board power.

Power down Sequence:

- VIN_PWR_BAD# signal from SMARC Edge must be inactive at the same time or before VDD_IN goes down.
- VDD_IN must go down at the same time or before VDD_RTC goes down.

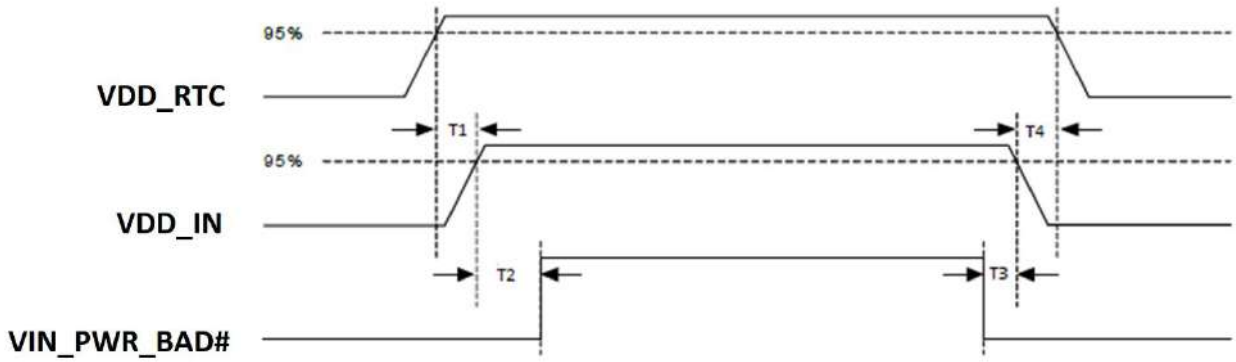

Figure 8: Power Input Sequencing

Table 11: Power Sequence Timing

Item	Description	Value
T1	VDD_RTC rise time to VDD_IN rise time	≥ 0 ms
T2	VDD_IN rise time to VIN_PWR_BAD# rise time	≥ 0 ms
T3	VIN_PWR_BAD# fall time to VDD_IN fall time	≥ 0 ms
T4	VDD_IN fall time to VDD_RTC fall time	≥ 0 ms

Important Note: All carrier board power supplies should be powered ON only after the SOM is powered ON completely. This is to ensure that there is no back voltage (leakage) from any supply on the board towards the i.MX8M CPU IO pins.

3.1.3 Power Consumption

Table 12: Power Consumption

Task/Status	Power Rail	Current Drawn/ Power Consumption
Run Mode Power Consumption[1]		
Play Video run in MIPI display (Gplay)	VDD_IN (5V)	1.19A/5.95W
Play Audio	VDD_IN (5V)	1.13A/5.65W
Ping Bluetooth	VDD_IN (5V)	1.12A/5.6W
Ping Wi-Fi	VDD_IN (5V)	1.11A/5.55W
Ping Ethernet (Eth0 and Eth1)	VDD_IN (5V)	1.26A/6.3W
Bluetooth file transfer	VDD_IN (5V)	1.21A/6.05W
eMMC to USB3.0 file transfer	VDD_IN (5V)	1.18A/5.9W
eMMC to PCIe X 4 file transfer	VDD_IN (5V)	1.32A/6.6W
GPU Processor -Graphics 3D Test	VDD_IN (5V)	1.53A/7.65W
Transfer the 1MB file between USB (USB3.0 and USB2.0), PCIe with 1000 counts	VDD_IN (5V)	1.26A/6.3W
Ethernet Streaming (Video Play)	VDD_IN (5V)	1.33A/6.65W
Dhrystone	VDD_IN (5V)	1.53A/7.65W
Maximum Power Test: • GPU test in background • Run the video on MIPI display using gstreamer • Ethernet - Run the ping (65507 packet size) test on back ground (eth0 & eth1) • WIFI- Run the ping test on back ground • File Transfer - Transfer 1GB file between all storage devices • Run the Dhrystone dry2 application	VDD_IN (5V)	1.81A/9.05W
Low Power Mode Power Consumption		
System Idle Mode.	VDD_IN (5V)	0.84A / 4.2W
Deep Sleep Mode.	VDD_IN (5V)	0.73A / 3.65W
RTC power when no VIN_3V3 supply is provided	VRTC_3V0	0.57uA/1.7uW

[1] *Power consumption measurements have been done in i.MX8M Quad based SMARC SOM (iW-G33M-SCMQ-4L002G-E008G-LIE) with iWave's Linux4.14.98 BSP (iW-PRFSZ-SC-01-R2.0-REL1.0-Linux4.14.98).*

3.2 Environmental Characteristics

3.2.1 Environmental Specification

The below table provides the Environment specification of i.MX8M SMARC SOM.

Table 13: Environmental Specification

Parameters	Min	Max
Operating temperature range (Industrial)[1, 2,3]	-40°C	85°C

[1] iWave guarantees the component selection for the given operating temperature. The operating temperature at the system level will be affected by the various system components like carrier board and its components, system enclosure, air circulation in the system, system power supply etc. Based on the system design, specific heat dissipating approach might be required from system to system. It is recommended to do the necessary system level thermal simulation and find necessary thermal solution in the system before using this board in the end application.

[2] If Expansion connectors are supported in i.MX8M SMARC SOM, operating temperature range is -35°C to 85°C. If Micro SD connector is supported in i.MX8M SMARC SOM, operating temperature range is -25°C to 85°C.

[3] For more information on Thermal solution & Heat sink refer the following section.

3.2.2 RoHS Compliance

iWave's i.MX8M SMARC SOM is designed by using RoHS compliant components and manufactured on lead free production process.

3.2.3 Electrostatic Discharge

iWave's i.MX8M SMARC SOM is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use the SOM except at an electrostatic free workstation.

3.2.4 Heat Sink

For any highly integrated System On Modules, thermal design is very important factor. As IC's size is decreasing and performance of module is increasing by rising processor frequencies, it generates high amount of heat which should be dissipated for the system to work as expected without fault.

To dissipate the heat, appropriate thermal management technique like Heat spreader, Heat sink must be used. Always remember that more effective thermal solution will give more performance out of the CPU.

iWave supports Heat Sink Solution for i.MX8M SMARC SOM. Refer the below figure for Heat Sink dimension details. It also has provision to fix the Fan if required. For Heat Sink ordering information, refer section4 **ORDERING INFORMATION**.

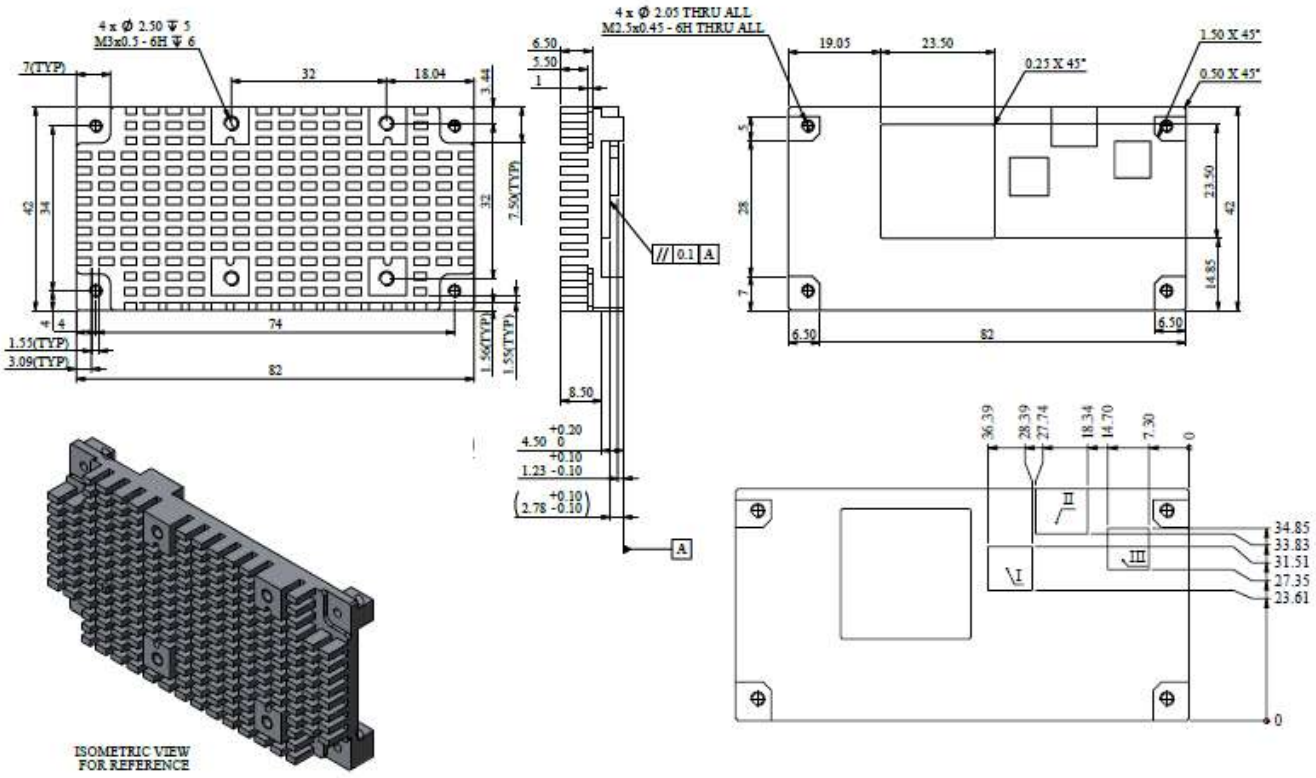

Figure 9: Heat Sink Dimension

3.3 Mechanical Characteristics

3.3.1 i.MX8M SMARC SOM Mechanical Dimensions

i.MX8M SMARC SOM PCB size is 50 mm x 82mm x 1.2mm. SMARC SOM mechanical dimension is shown below. (All dimensions are shown in mm)

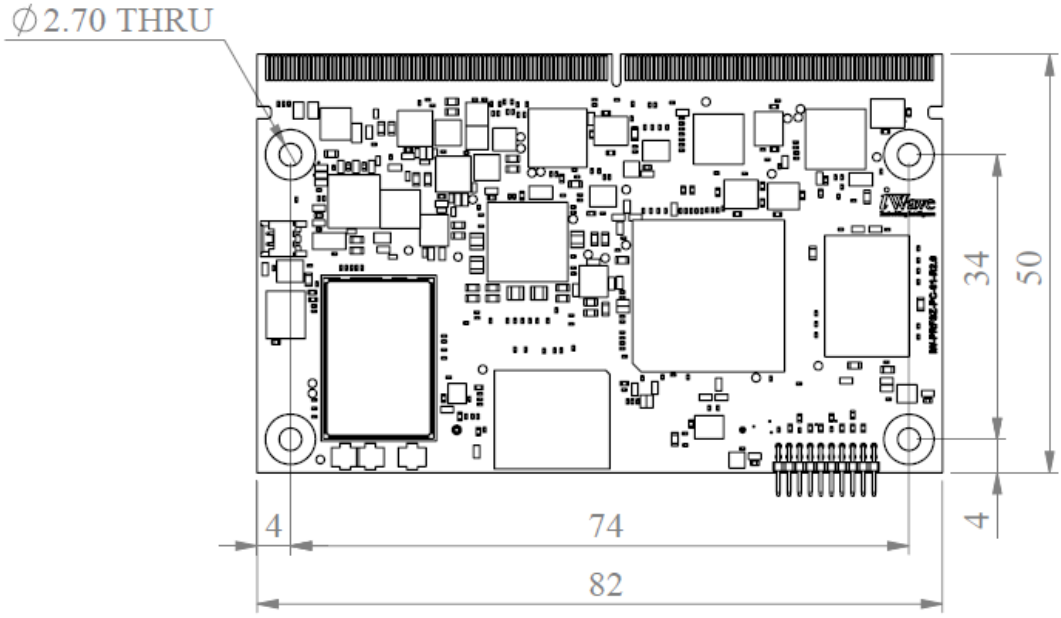

Figure 10: Mechanical dimension of i.MX8M SMARC SOM Top View

The i.MX8M SMARC SOM PCB thickness is 1.2mm±0.15mm, top side maximum height component is 3.5mm (FAN Header) followed by 3.5mm (JTAG Header) which is optional in default configuration then 3.2mm Inductor will be the height components on Top side in default configuration and bottom side maximum height component is expansion connector (3.95mm) followed by RTC Controller (1.75mm). Refer the below figure which gives height details of the i.MX8M SMARC SOM.

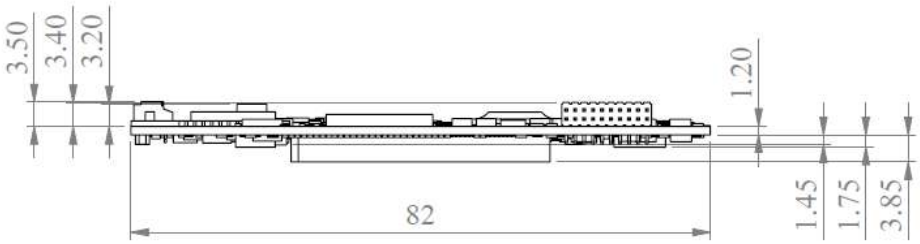

Figure 11: Mechanical dimension of i.MX8M SMARC SOM- Side View

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for different i.MX8M SMARC SOM variations. For orderable part number of higher RAM memory size or Flash memory size SOM configurations, contact iWave. Also, if the desired part number is not listed in below table or if any custom configuration part number is required, contact iWave.

Table 14: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-Rainbow G33M - i.MX8M Quad SMARC SOM (Industrial grade)		
iW-G33M-SCMQ-4L002G-E008G-BIE	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-BIF	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,2x Ethernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-BIG	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 1xEthernet and no Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-BIH	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,1x Ethernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-LIE	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-LIF	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,2x Ethernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-LIG	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 1xEthernet and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-LIH	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,1x Ethernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-AIE	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-AIF	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,2x Ethernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-AIG	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 1xEthernet and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMQ-4L002G-E008G-AIH	With i.MX8M Quad Core CPU, 2GB LPDDR4, 8GB eMMC,1x Ethernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C

iW-Rainbow G33M - i.MX8M QuadLite SMARC SOM (Industrial grade)		
iW-G33M-SCML-4L002G-E008G-BIE	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,2xEthernrt and no Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-BIF	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 2x Ethernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-BIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,1xEthernrt and no Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-BIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-LIE	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,2xEthernrt and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-LIF	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 2xEthernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-LIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,1xEthernrt and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-LIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-AIE	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,2xEthernrt and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-AIF	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 2xEthernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-AIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,1xEthernrt and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCML-4L002G-E008G-AIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C
iW-Rainbow G33M - i.MX8M Dual SMARC SOM (Industrial grade)		
iW-G33M-SCMD-4L001G-E008G-BIE	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-BIF	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, 2xEthernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-BIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT,1xEthernrt and no Expansion Connector - Boot code	-40°C to 85°C

iW-G33M-SCMD-4L001G-E008G-BIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Boot code	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-LIE	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-LIF	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, 2xEthernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-LIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 1xEthernrt and no Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-LIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Linux	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-AIE	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 2xEthernet and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-AIF	With i.MX8M Dual Core CPU, 1GB LPDDR4, 8GB eMMC, 2xEthernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-AIG	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, Wi-Fi, BT, 1xEthernrt and no Expansion Connector - Android	-40°C to 85°C
iW-G33M-SCMD-4L001G-E008G-AIH	With i.MX8M QuadLite Core CPU, 2GB LPDDR4, 8GB eMMC, 1xEthernet and without Wi-Fi, BT & Expansion Connector - Android	-40°C to 85°C

Important Note: Some of the above-mentioned Part Number is subject to MOQ purchase. Contact iWave for further details.

For SOM identification purpose, Product Part Number and SOM Unique Serial Number are pasted as Label with Barcode readable format on SOM.

5. APPENDIX

5.1 i.MX8M SMARC Development Platform

iWave Systems supports iW-RainboW-G33D-i.MX8M SMARC Development Platform which is targeted for quick validation of i.MX8M CPU based SMARC SOM and its features. Being a Nano-ITX form factor with 120mm x 120mm size, the carrier board is highly packed with all necessary interfaces & on-board connectors to validate complete SMARC supported features.

For more details on i.MX8M SMARC Development Platform, visit the below web link.

https://www.iwavesystems.com/product/dev-kits/smarc/imx8m-dev-kit/imx8m-development-board.html

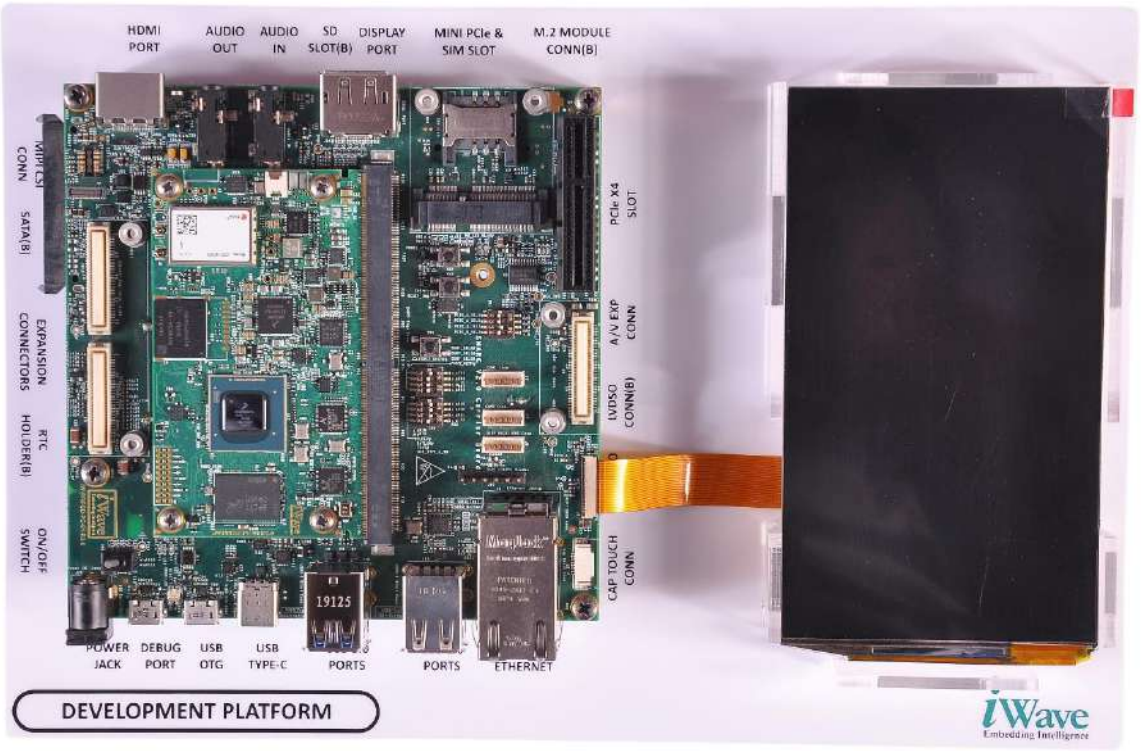

Figure 12: i.MX8M SMARC Development Platform