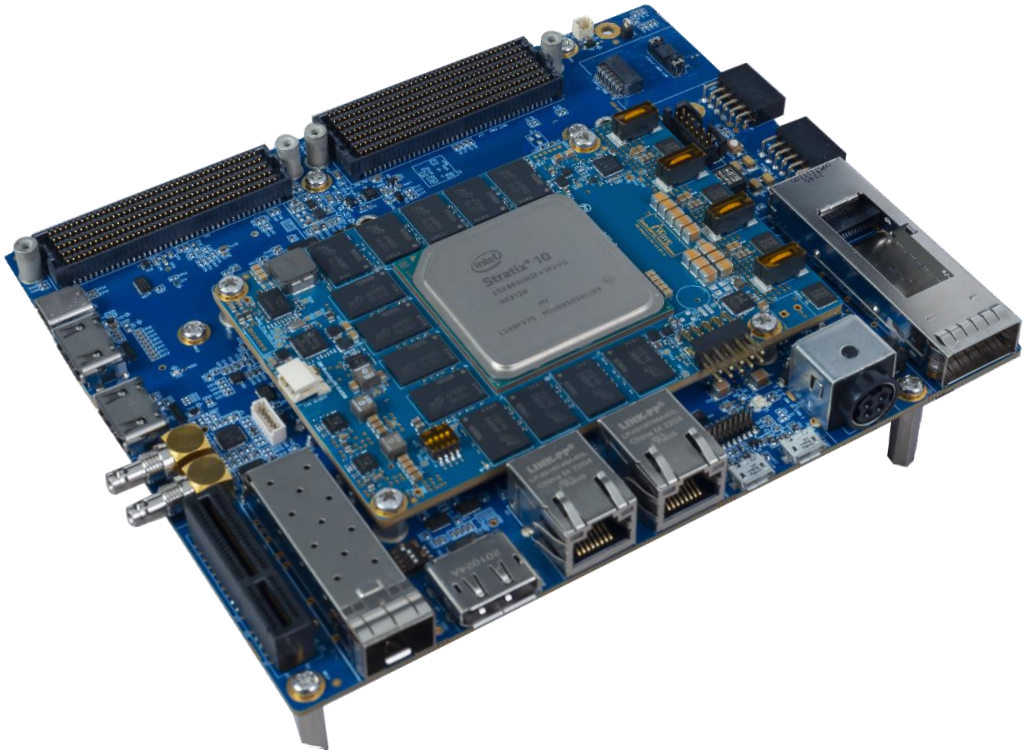
iW-RainboW-G45D
Stratix10 GX/SX SoC FPGA SOM
Development Platform
Hardware User Guide



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1. INTRODUCTION

1.1 Purpose

The iW-RainboW-G45D Intel Stratix10 GX/SX SoC FPGA SOM Development platform incorporates Intel Stratix10 GX/SX SoC FPGA based SOM and Ultra-High-Performance Carrier board for complete validation of Intel Stratix10 GX/SX SoC FPGA functionality. This document is the Hardware User Guide for the iW-RainboW-G45D Intel Stratix10 GX/SX SoC FPGA Development Platform and provides detailed information on the overall design & usage of the Carrier Board from a Hardware Systems perspective. The details about the iW-RainboW-G45M Intel Stratix10 GX/SX SoC FPGA SOM hardware is explained in another document “iW-RainboW-G45M-Stratix10 SoC FPGA-SOM-HardwareUserGuide”.

1.2 Overview

iWave's iW-RainboW-G45D Stratix10 GX/SX SoC FPGA Development platform comes with iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM and the Ultra-High-Performance Carrier Board. The development board can be used for quick prototyping of various applications targeted by the iW-RainboW-G45M Stratix10 GX/SX SoC FPGA. With the 140mmx170mm size, carrier board is packed with all the necessary on-board connectors to validate the features of iW-RainboW-G45M Stratix10 GX/SX SoC FPGA SOM.

1.3 List of Acronyms

The following acronyms will be used throughout this document.

Table 1: Acronyms & Abbreviations

Acronyms	Abbreviations
ARM	Advanced RISC Machine
B2B	Board to Board
CAN	Controller Area Network
CH	Channel
CMOS	Complementary Metal Oxide Semiconductor
DP	Display Port
FPGA	Field Programmable Gate Array
FMC	FPGA Mezzanine Card
FMC+	FPGA Mezzanine Card Plus
Gbps	Gigabits per sec
GEM	Gigabit Ethernet Controller
GPIO	General Purpose Input Output
HDMI	High-Definition Multimedia Interface
HPC	High Pin Count
I2C	Inter-Integrated Circuit
IC	Integrated Circuit
JTAG	Joint Test Action Group

Acronyms	Abbreviations
LVCMOS	Low Voltage Complementary Metal Oxide Semiconductor
LVDS	Low Voltage Differential Signal
Mbps	Megabits per sec
MHz	Mega Hertz
NC	No Connect
NPTH	Non-Plated Through Hole
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PMOD	Peripheral Module
PTH	Plated Through Hole
RGMII	Reduced Gigabit Media Independent Interface
RTC	Real Time Clock
RX	Receiver
SATA	Serial Advanced Technology Attachment
SDI	Serial Digital Interface
SDIO	Secure Digital Input Output
SDHI	SD Card Host Interface
SFP	Small Form-factor Pluggable
SOM	System On Module
TXVR	Transceiver
TX	Transmitter
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
USB OTG	USB On The Go
QSFP+	Quad Small Form-factor Pluggable

Terminology Description

In this document, wherever Signal Type is mentioned, below terminology is used.

Table 2: Terminology

Terminology	Description
I	Input Signal
O	Output Signal
IO	Bidirectional Input/output Signal
CMOS	Complementary Metal Oxide Semiconductor Signal
DIFF	Differential Signal
OD	Open Drain Signal
OC	Open Collector Signal
Analog	Analog Signal
Power	Power Pin
PU	Pull Up
PD	Pull Down
NA	Not Applicable
NC	Not Connected

Note: Signal Type does not include internal pull-ups or pull-downs implemented by the chip vendors and only includes the pull-ups or pull-downs implemented on board.

1.4 References

- Stratix10 GX/SX Datasheet & HPS Technical Reference Manual
- Stratix10 GX/SX SOM Hardware User Guide

2. ARCHITECTURE AND DESIGN

This section provides detailed information about the Carrier Board features of iW-RainboW-G45D Stratix10 GX/SX SoC FPGA Development Platform with high level block diagram and detailed information about each block.

2.1 iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA SOM Carrier Board Block Diagram

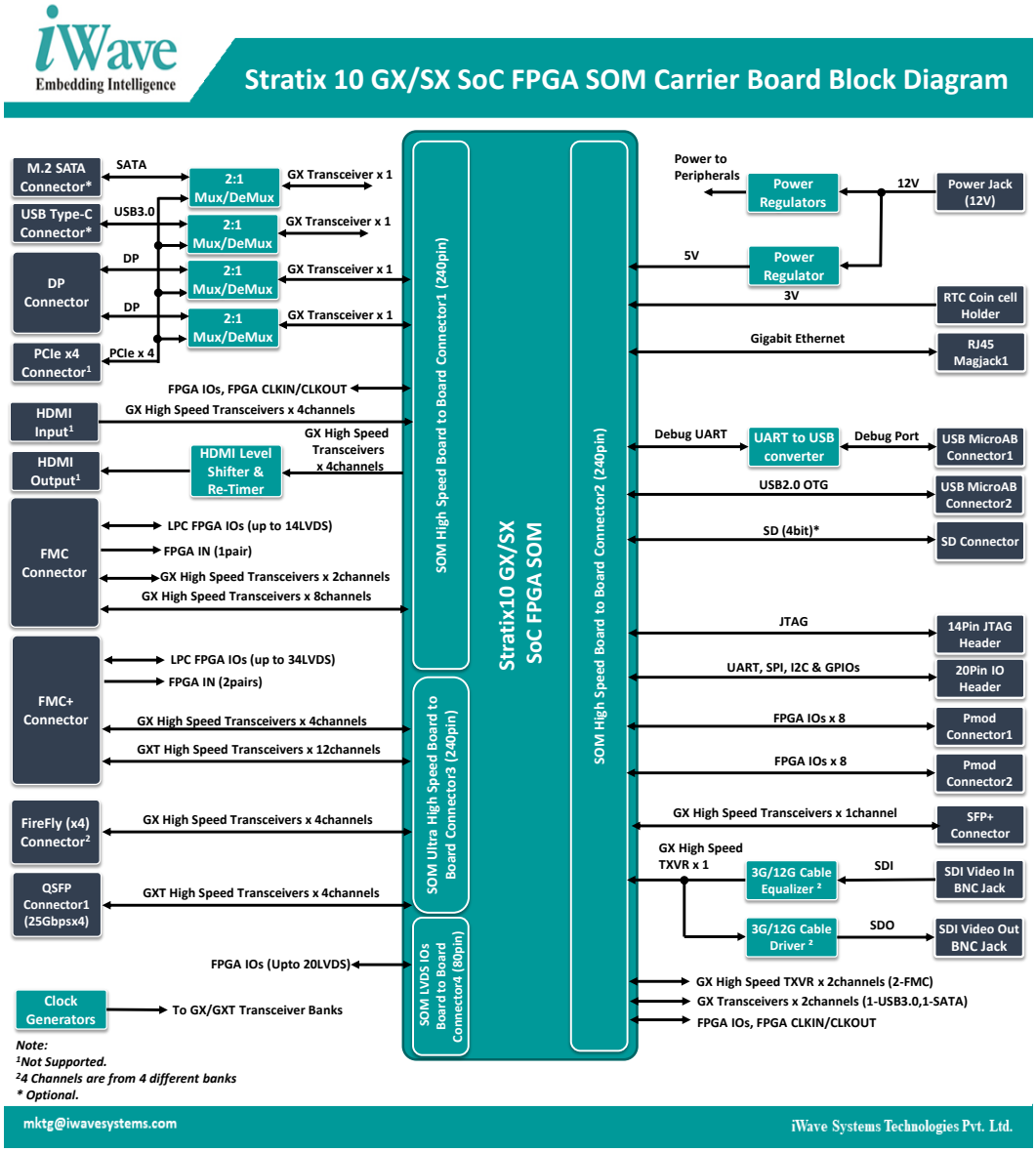

Figure 1: iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA SOM Carrier Board Block Diagram

2.2 iW-RainboW-G45D Stratix10 GX/SX SoC FPGA SOM Carrier Board Features:

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Carrier board supports the following features to validate the iW-RainboW-G45M-Stratix10 SoC FPGA SOM supported interfaces.

HPS Interface Features

- Debug UART through USB Micro AB connector x 1
- Gigabit Ethernet through RJ45MagJack x 1
- USB2.0 OTG through Micro AB connector or Type-C Connector x 1
- UART (with CTS & RTS)/SPI Slave x 1

FPGA Interface Features

- SFP+ Connector x 1
- SDI Video IN through HD BNC Connector x 1
- SDI Video OUT through HD BNC Connector x 1
- QSFP28/QSFP+/QSFP Connector x 1
- FireFly Connector x 1
- Display Port (Single Lane) x 1
- FMC High Pin Count (HPC) Connector
  - 10 High Speed GX Transceivers Channels
  - 2 Transceiver Reference Clock inputs
  - Up to 09 LVDS IOs/18 Single ended (SE) IOs from FPGA IO Banks.
  - 2 Clock Input Capable LVDS/SE pins from FPGA IO Banks
  - 3 Clock Output Capable LVDS/SE pins from FPGA IO Banks
- FMC+ High Pin Count (HPC) Connector
  - Up to 12 High Speed GXT Transceivers Channels
  - Up to 16 High Speed GXT Transceivers Channels (Inclusive of the GXT Channels)
  - 2 Transceiver Reference Clock Inputs
  - Up to 28 LVDS IOs/56 Single ended (SE) IOs from FPGA IO Banks
  - 5 Clock Input Capable LVDS/SE pins from FPGA IO Banks
  - 2 Clock Output Capable LVDS/SE pins from FPGA IO Banks
- PMOD Connector x 2

Additional Features

- Clock Synthesizers/Generators x2
- JTAG Connector x 1
- 16-Bit IO Expanders x 3
- I2C Expander x 1
- 20 Pin GPIO Header x 1
- Power ON/OFF DIP Switch x 1
- Reset Pushbutton Switch x 1
- RTC Coin Cell Holder x 1
- 12V FAN Header x 1

General Specification

- Power Supply : DC 12V, 14A Power Input Jack
- Form Factor : 140mm X 170mm

2.3 Board to Board Connectors

The Carrier Board of iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Devkit supports four Board to Board mating connectors for Stratix10 GX/SX SoC FPGA SOM attachment. This Board to Board connector are capable of handling high-speed serialized signals and can be used for size constrained embedded applications.

2.3.1 Board to Board Connector1

Board to Board Connector1 (J18) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector1 pinout, refer the document "iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM Hardware User Guide".

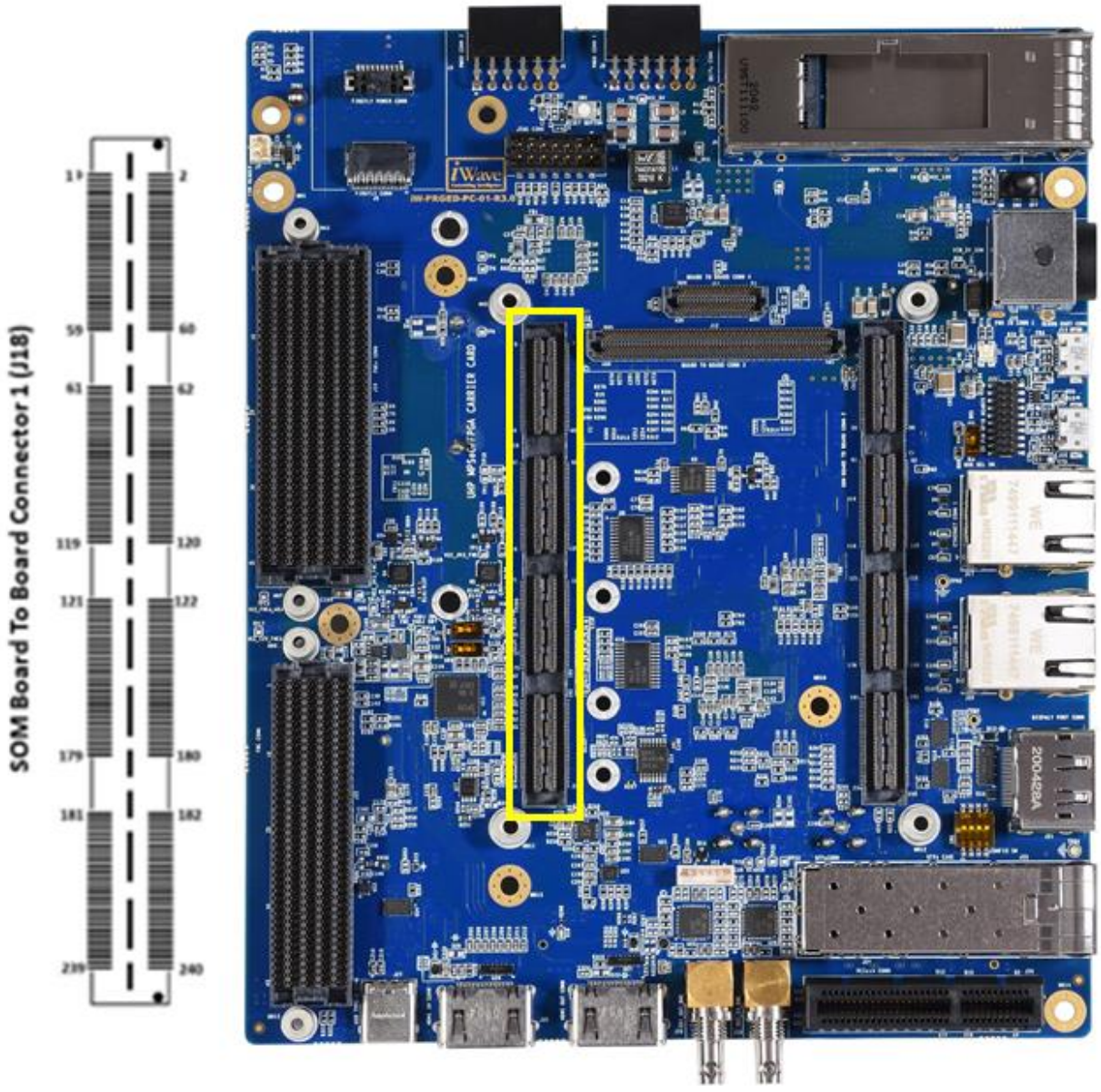

Figure 2: Board to Board Connector1

2.3.2 Board to Board Connector2

Board to Board Connector2 (J19) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector2 pinout, refer the document "iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM Hardware User Guide".

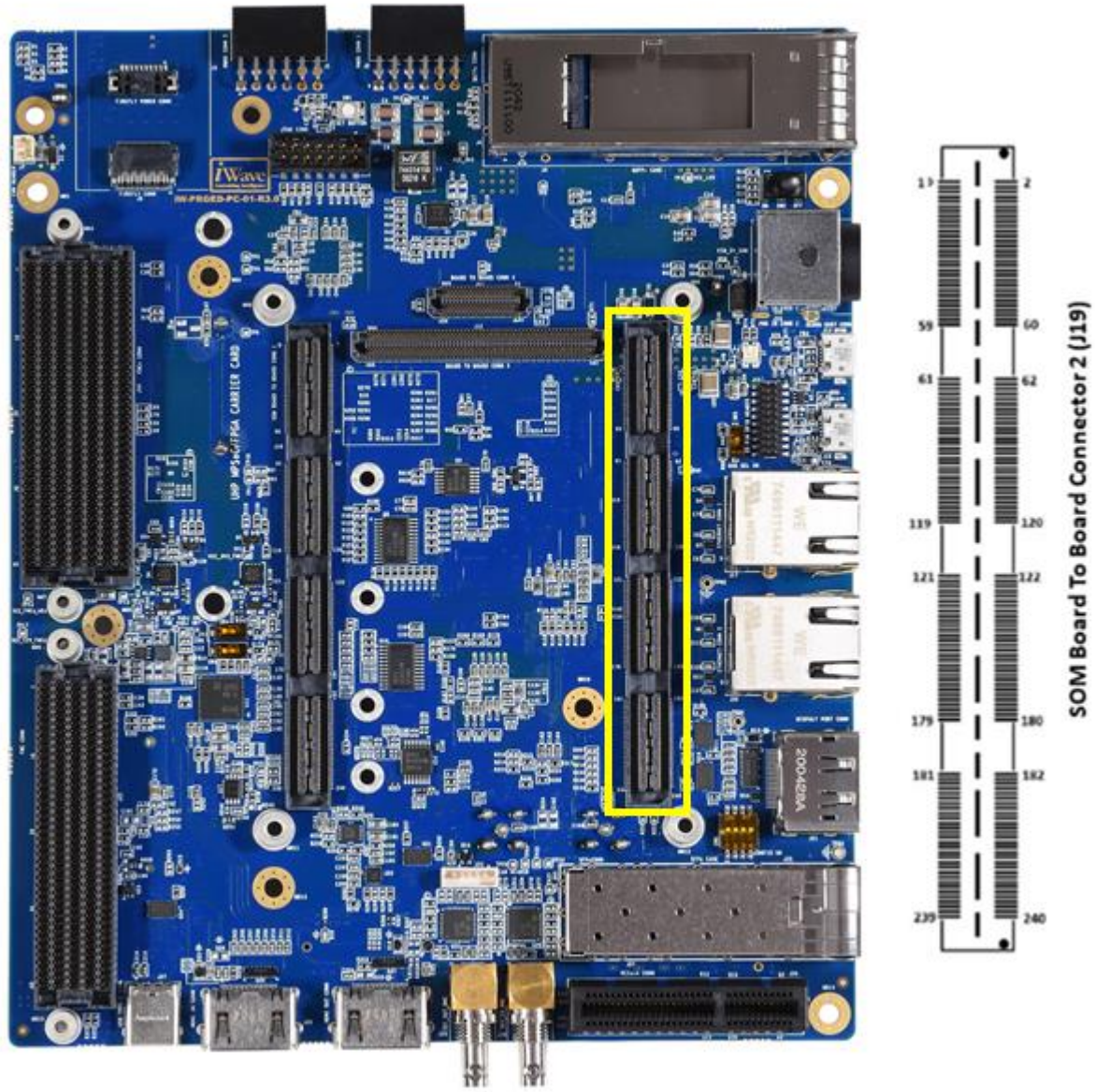

Figure 3: Board to Board Connector2

2.3.3 Board to Board Connector3

Board to Board Connector3 (J12) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector3 pinout, refer the document "iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM Hardware User Guide".

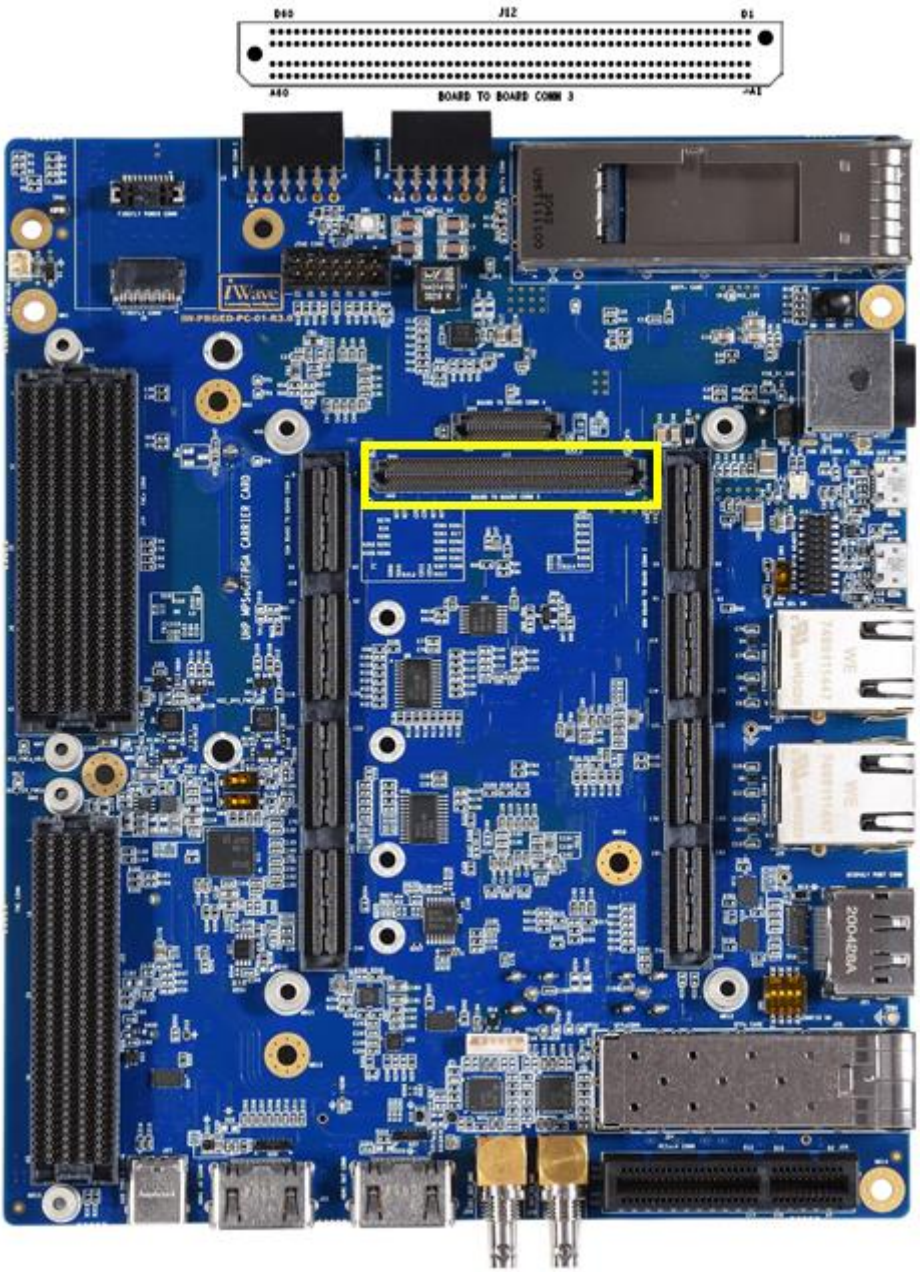

Figure 4 Board to Board Connector3

2.3.4 Board to Board Connector4

Board to Board Connector4 (J11) is physically located at the top of the board as shown below.

Note: For the Board to Board Connector4 pinout, refer the document "iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM Hardware User Guide".

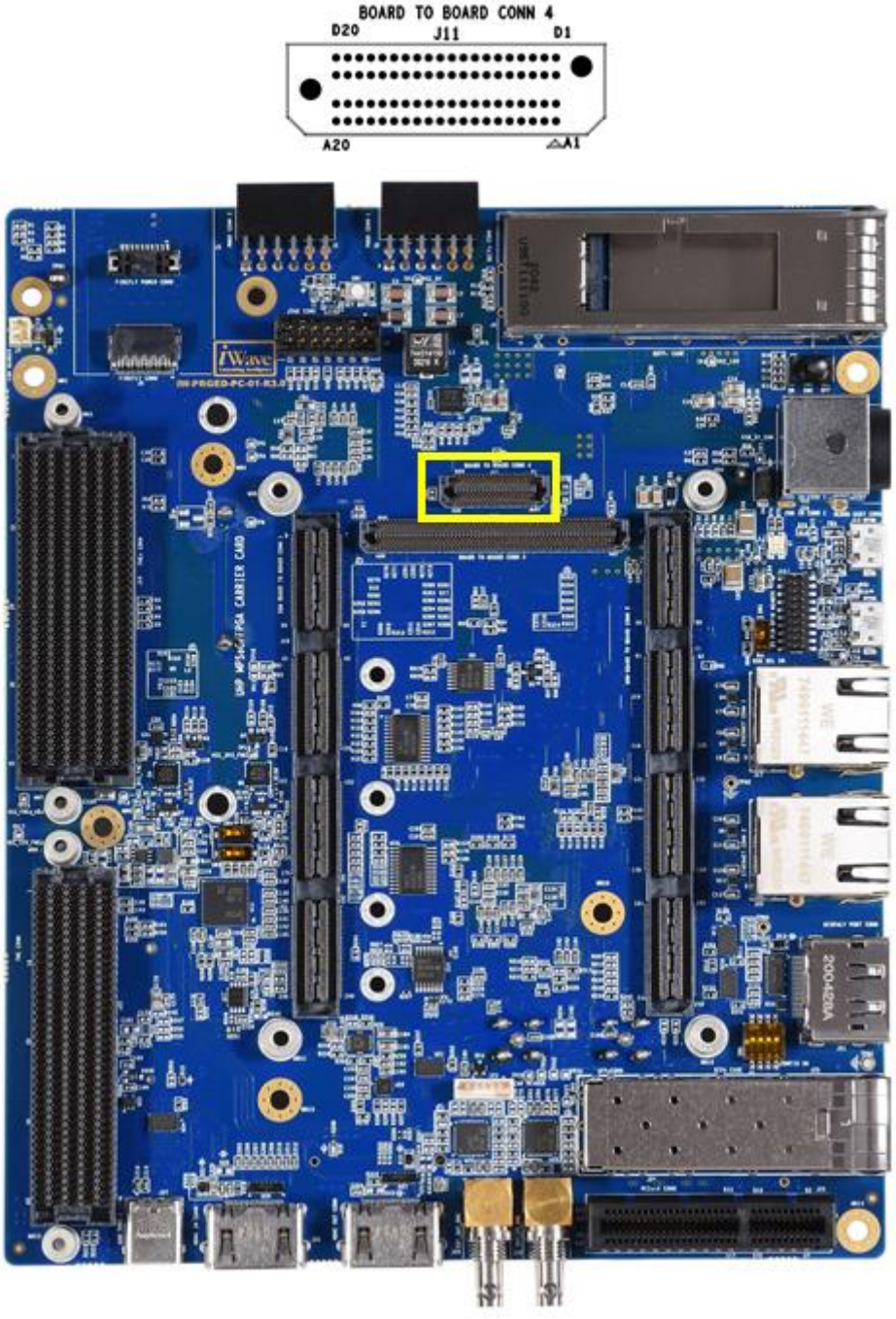

Figure 5 Board to Board Connector4

2.4 HPS Interface Features

The features which are supported from the HPS of iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM through the Carrier Card are explained in the following sections.

2.4.1 Gigabit Ethernet Port1 - HPS

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports two 10/100/1000Mbps Ethernet ports. First Ethernet port is supported through EMAC1 interface of CPU HPS. And the second one is connected to the FPGA Ios. Ethernet PHY output signals from Board to Board connector2 are directly connected to RJ45 Magjack (J17). The Ethernet supports Speed (Yellow) and Link/Activity (Green) LED indications on RJ45 Magjack connector. This RJ45 Magjack connector(J17) is physically located at the top of the board as shown below.

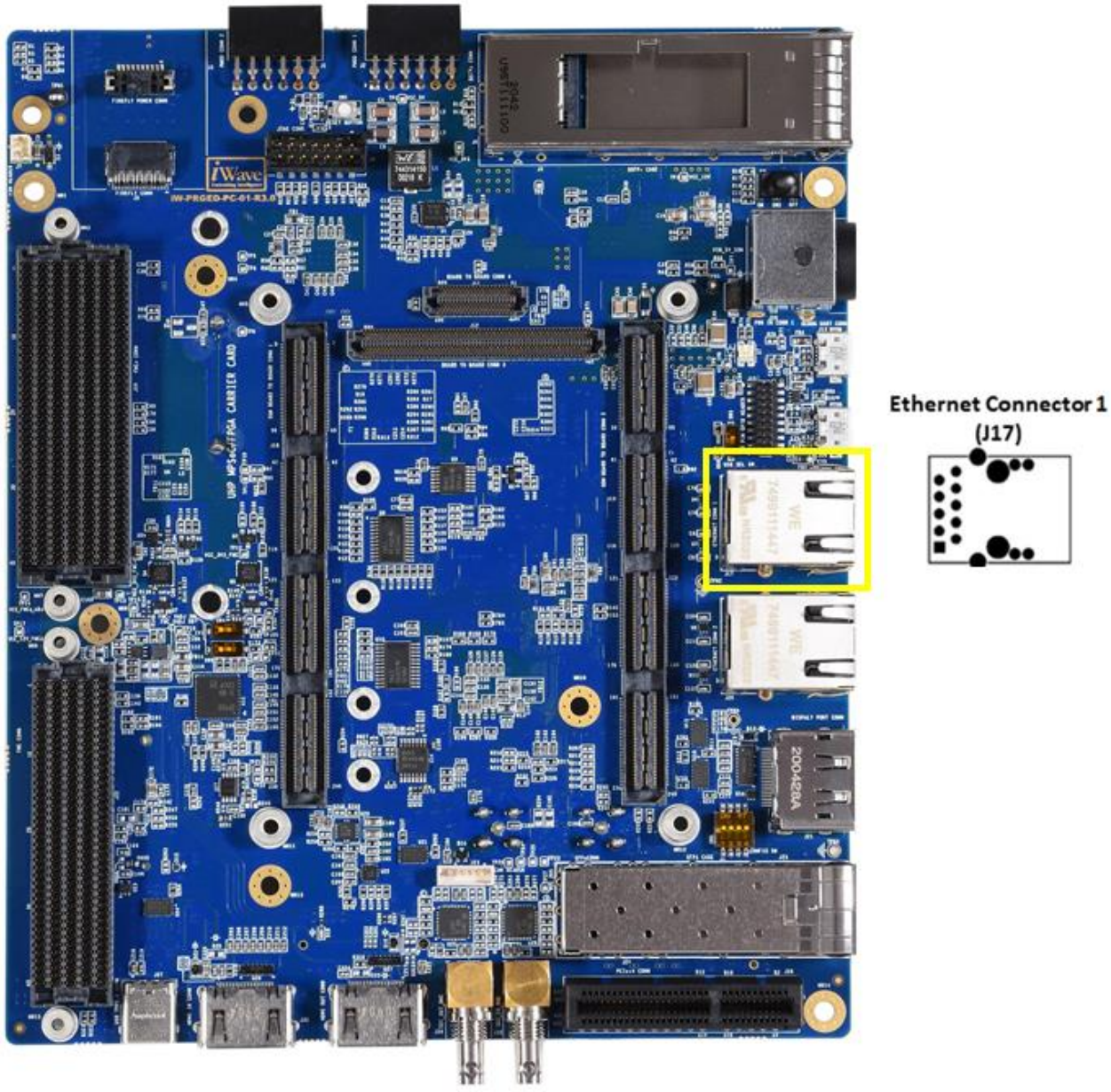

Figure 6: Gigabit Ethernet Connector1

2.4.2 USB2.0 OTG Port

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports USB2.0 High Speed OTG interface through USB0 OTG Controller of Stratix10 GX/SX SoC FPGA HPS. This USB2.0 OTG interface is supported through USB2.0 MicroAB connector (J16). The USB PHY Transceiver output signals from Board to Board connector2 is connected to "FUSB340" USB Switch for selecting the USB2.0 OTG connection between USB2.0 MicroAB connector (J16) and USB3.0 TypeC connector (J27). The selection can be done by setting the Single bit DIP switch (SW3). If the DIP switch (SW3) is set to ON, USB2.0 OTG is connected to MicroAB connector (J16) and if the DIP switch (SW3) is set to OFF, USB2.0 OTG is connected to USB3.0 TypeC connector (J27).

The USB2.0 OTG port can be used as full functional OTG functionality which supports USB2.0 host and USB2.0 device based on USB ID pin status. The VBUS power of this USB2.0 MicroAB connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 900mA in host mode. The USB PHY transceiver in SOM detects the USB functionality through USB ID pin (34^{th} pin of B2B-2) and controls the power using the USB_PWR_EN pin (32^{nd} pin of B2B-2). This USB2.0 OTG connector (J16) is physically located at the top of the board as shown below.

Note: *Connect the USB2.0 pendrive/mouse to the microAB to Host connector first, then connect the connector to the board connector(J16).*

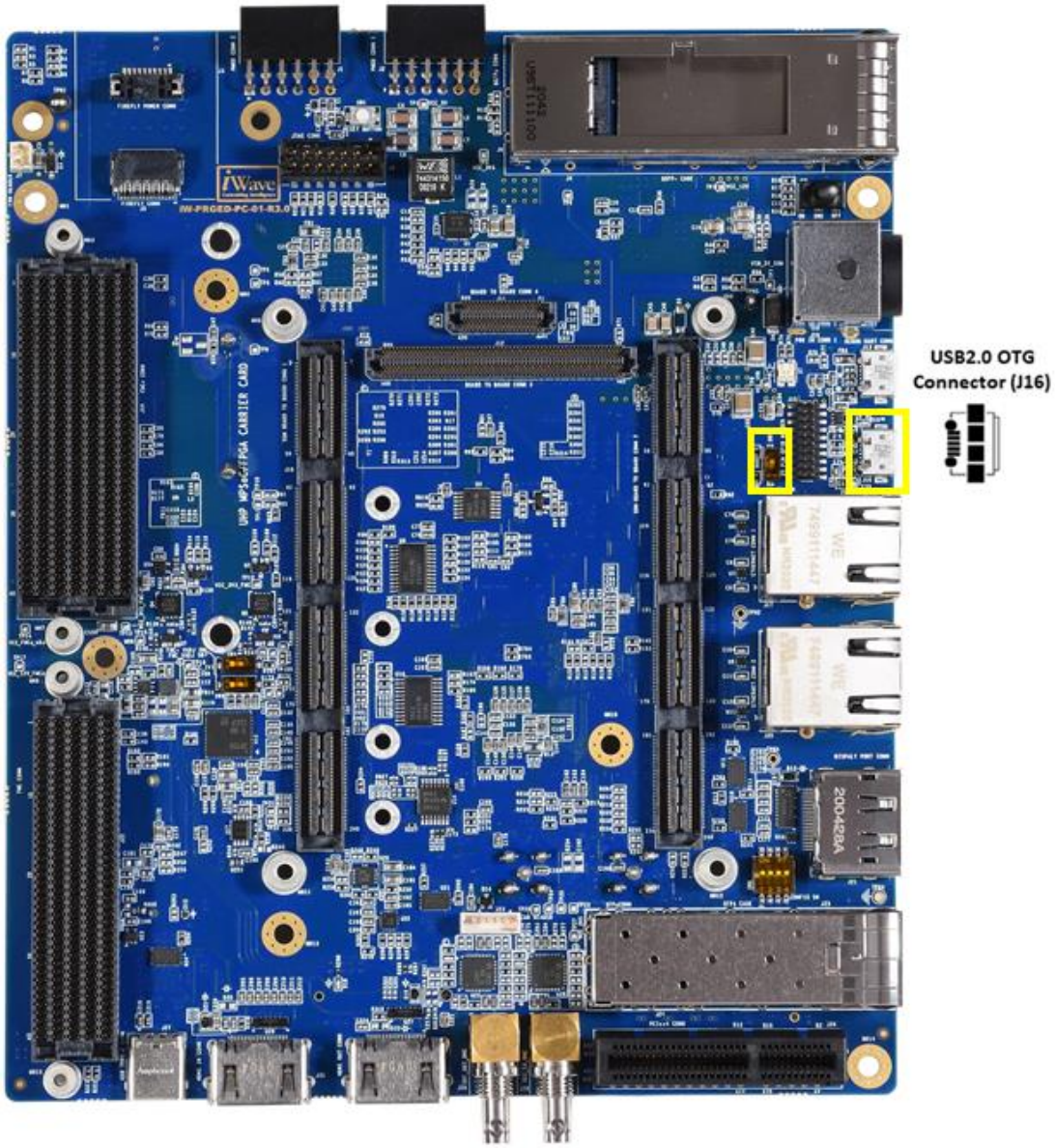

Figure 7: USB OTG Connector

2.4.3 Standard SD Port (Optional)

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform optionally supports one Standard SD interface through HPS SDMMC interface of Stratix10 GX/SX SoC FPGA. These SDMMC signals are muxed with the On-SOM eMMC and so the Standard SD feature in the Development Platform can be made available only when eMMC is unused. These SDMMC signals from Board to Board connector2 is connected to Standard SD connector (J33) through auto-direction control memory card voltage level translator to support both 1.8V and 3.3V supported cards. It supports up to 4-Bit data transfer with card detect and write protect.

The memory card voltage level translator's voltage selection is controlled through HPS_SD_PWR_EN_B2B pin from Board to Board Connector2 pin44. If HPS_SD_PWR_EN_B2B is set to low, then 3.3V IO level is selected for SDMMC signals to SD connector. If HPS_SD_PWR_EN_B2B is set to high, then 1.8V IO level is selected for SDMMC signals to SD connector. For the Card detect and Write Protect functions, HPS GPIOs - GPIO1_IO18 and GPIO1_IO19 are used respectively.The Standard SD connector (J33) is physically located at the bottom of the board as shown below.

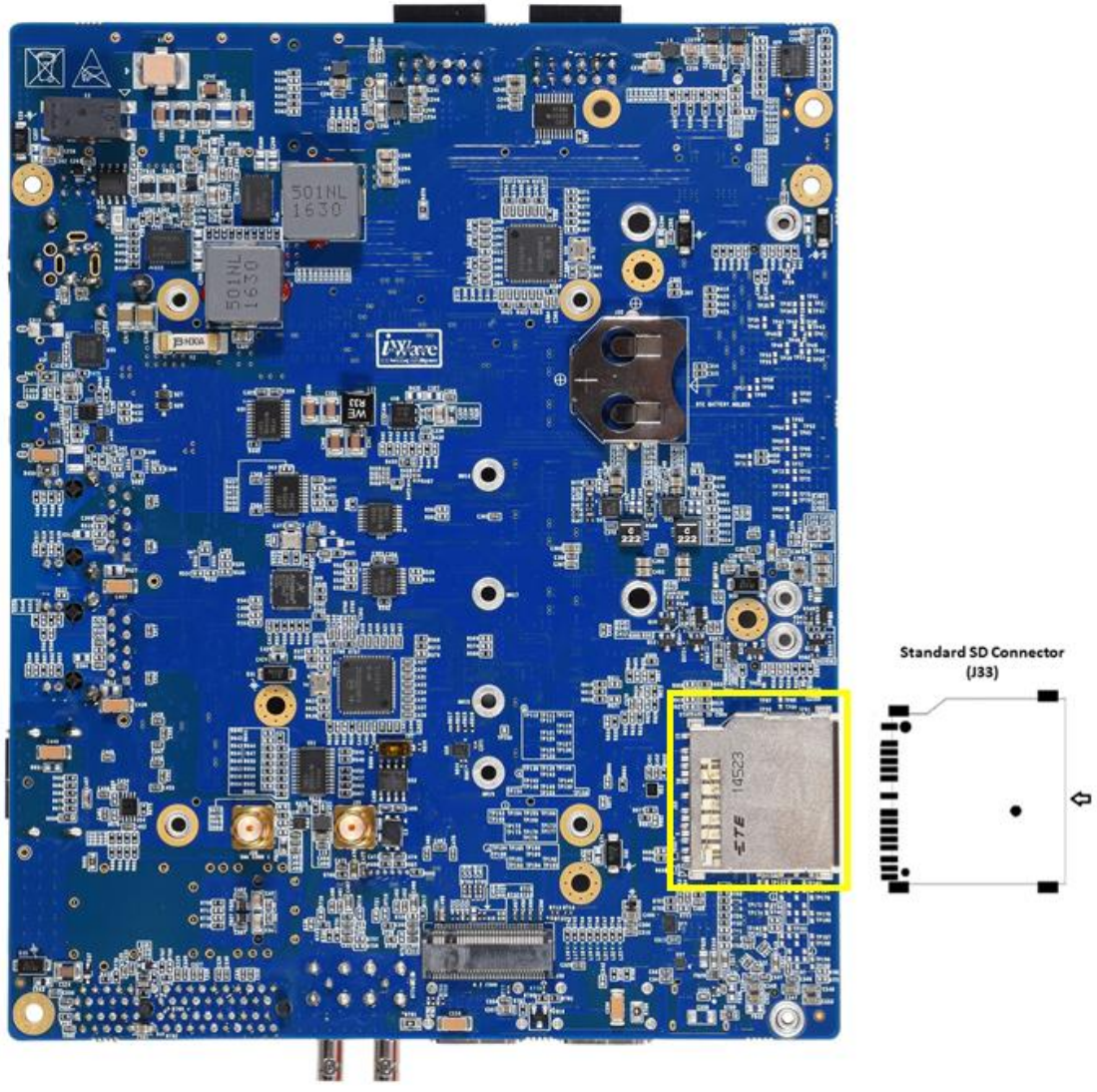

Figure 8: Standard SD Connector

2.4.4 Debug UART

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports debug interface through UART1 interface of the HPS of Stratix10 GX/SX SoC FPGA. This UART1 signals from Board to Board Connector2 are connected to the UART to USB Convertor “FT232RQ”. The output of the USB convetor is connected to USB MicroAB Connector (J13). This USB MicroAB Connector can be used for Debug purpose which is is physically located at the top of the board as shown below.

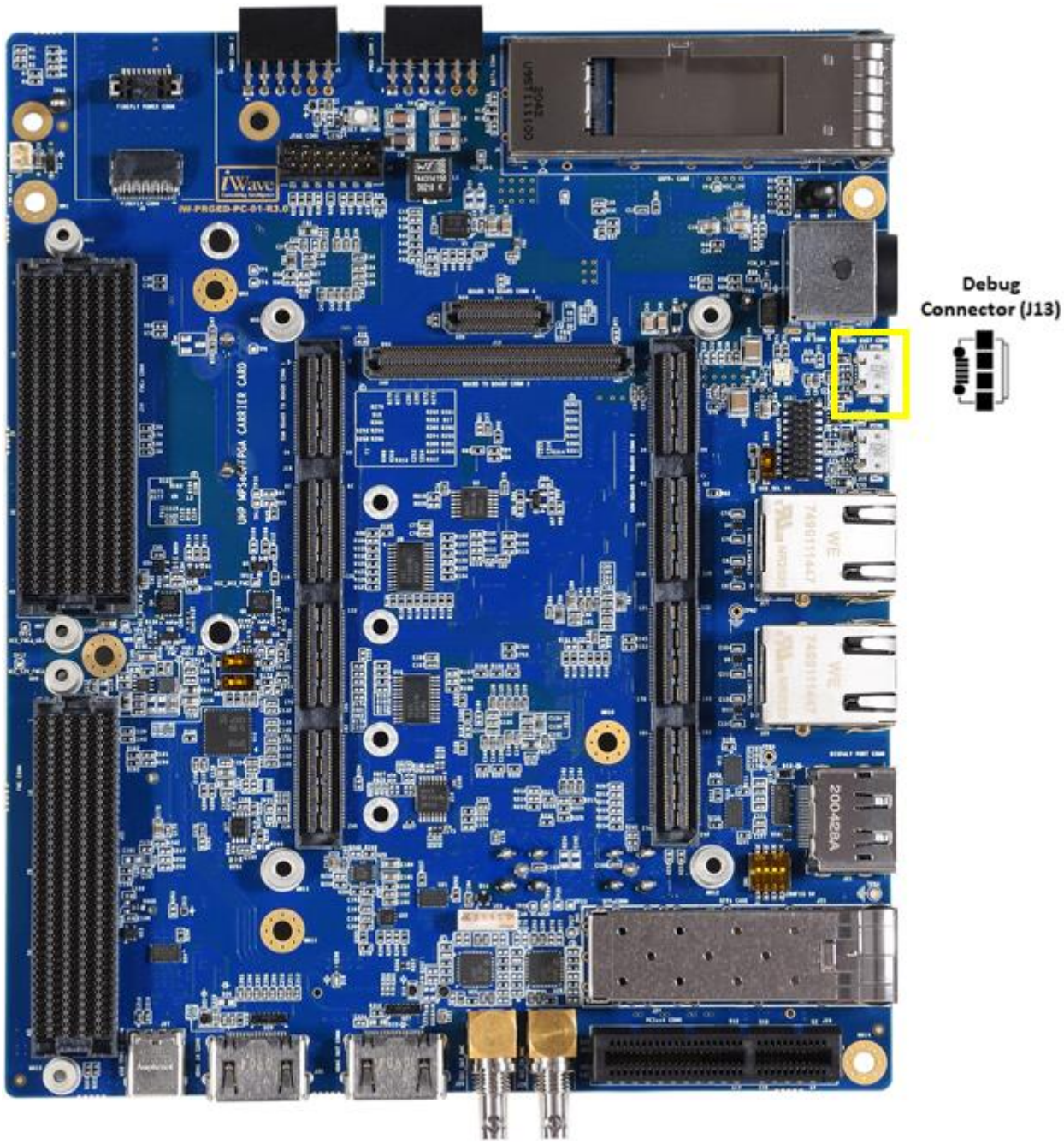

Figure 9: Debug UART Connector

2.5 FPGA Interface Features

The features which are supported from the FPGA of the Stratix10 GX/SX SoC FPGA is explained in the following section.

2.5.1 GX/GXT High Speed Transceivers

The iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM supports supports 48 high speed Transceivers which are conneted to different interfaces in the Carrier Board (8 from B2B-1, 4 from B2B-2, 24 from B2B-3) as mentioned below.

- SFP+ Connector (1 Transceiver Lane)
- 3G/12G SDI Video IN (1 Transmitter Lane)
- 3G/12G SDI Video OUT (1 Receiver lane)
- SMA TX (1 Transmitter Lane)
- DisplayPort (1 Transmitter Lane)
- QSFP28/QSFP+/QSFP Connector (4 Transceivers Lanes)
- FireFly Connector (4 Transceivers Lanes)
- FMC HPC Connector (10 Transceiver lanes)
- FMC+ HPC Connector (16 Transceiver lanes)

Note: All the transceivers coming from the Stratix10 GX/SX SoC FPGA SOM are not supported in the iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform. Also, some of the transceivers are connected to interfaces not supported in the platform.

2.5.2 GX/GXT Transceivers

The iW-RainboW-G45D-Stratix10 GX/SX SoC Development platform supports different high speed interfaces through four Transceiver lanes (two from B2B-1 and two from B2B-2). Each Transceiver lane is connected to High speed MUX/DEMUX IC to support different high speed interfaces as mentioned below.

- x1, x2, or x4 lane of PCIe (Not Supported due to CPU limitation)
- 1 or 2 lanes of DisplayPort (TX only) at 1.62Gb/s, 2.7Gb/s, or 5.4Gb/s
- 1 SATA port at 1.5Gb/s, 3.0Gb/s, or 6.0Gb/s
- 1 USB3.0 port at 5.0Gb/s

The MUX/DEMUX connection and interface selection option is shown below for easy understanding. The selection control of each MUX IC is connected to Transceiver Lanes selection 4bit DIP switch (SW6).

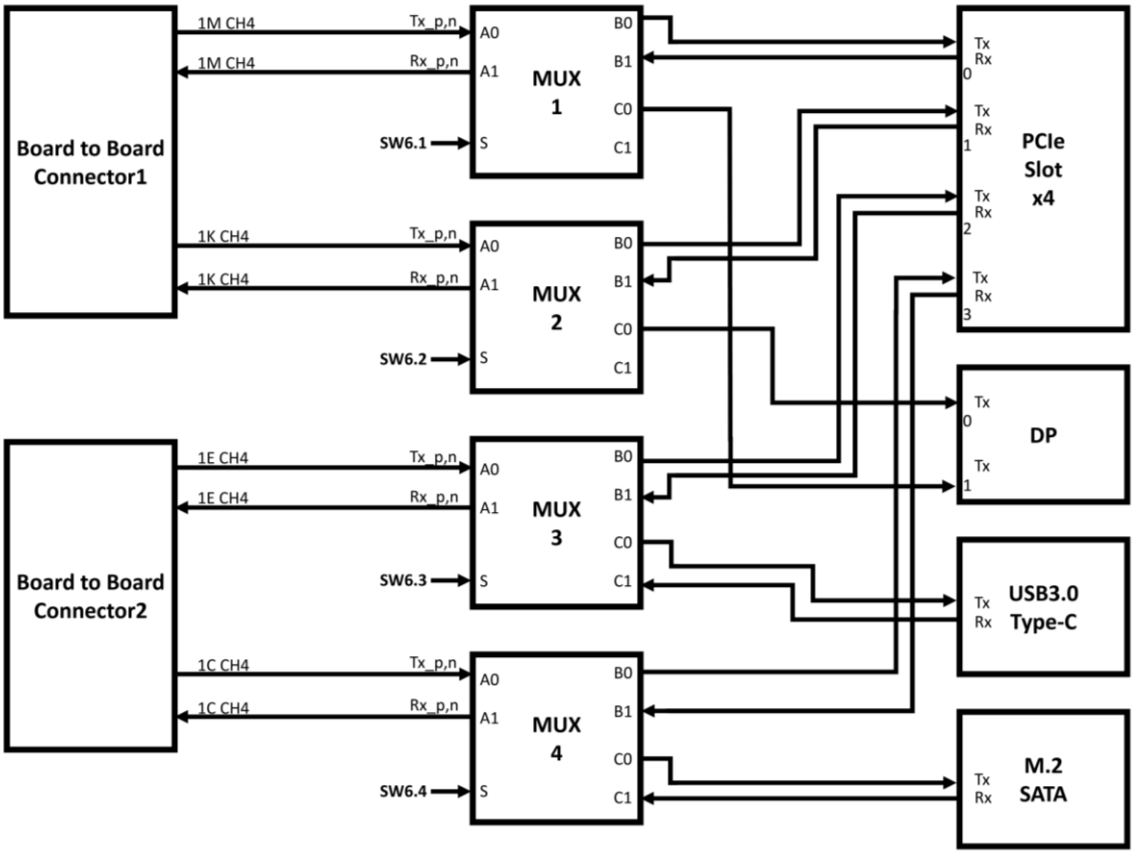

Figure 10: Transceiver Switch Connectivity.

The Transceiver Lane selection switch (SW6) setting and corresponding interface selection option is explained below.

Table 3: Transceiver Lane Selection Switch Setting

Transceiver Lanes	Transceiver Lane Selection Switch (SW6)		
	Switch Bit Number	Switch Bit Position	
		OFF	ON
1M CH4	**Bit1**	1M Bank Lane4 is connected to Lane0 of PCIe x4 connector	1M Bank Lane4 is connected to Lane1 of DP connector
1K CH4	**Bit2**	1K Bank Lane4 is connected to Lane1 of PCIe x4 connector	1K Bank Lane4 is connected to Lane0 of DP connector (default)
1E CH4	**Bit3**	1E Bank Lane4 is connected to Lane2 of PCIe x4 connector	1E Bank Lane4 is connected to Lane1 of USB3.0 Type-C connector (default)
1C CH4	**Bit4**	1C Bank Lane4 is connected to Lane3 of PCIe x4 connector	1C Bank Lane4 is connected to M.2 SATA connector (default)

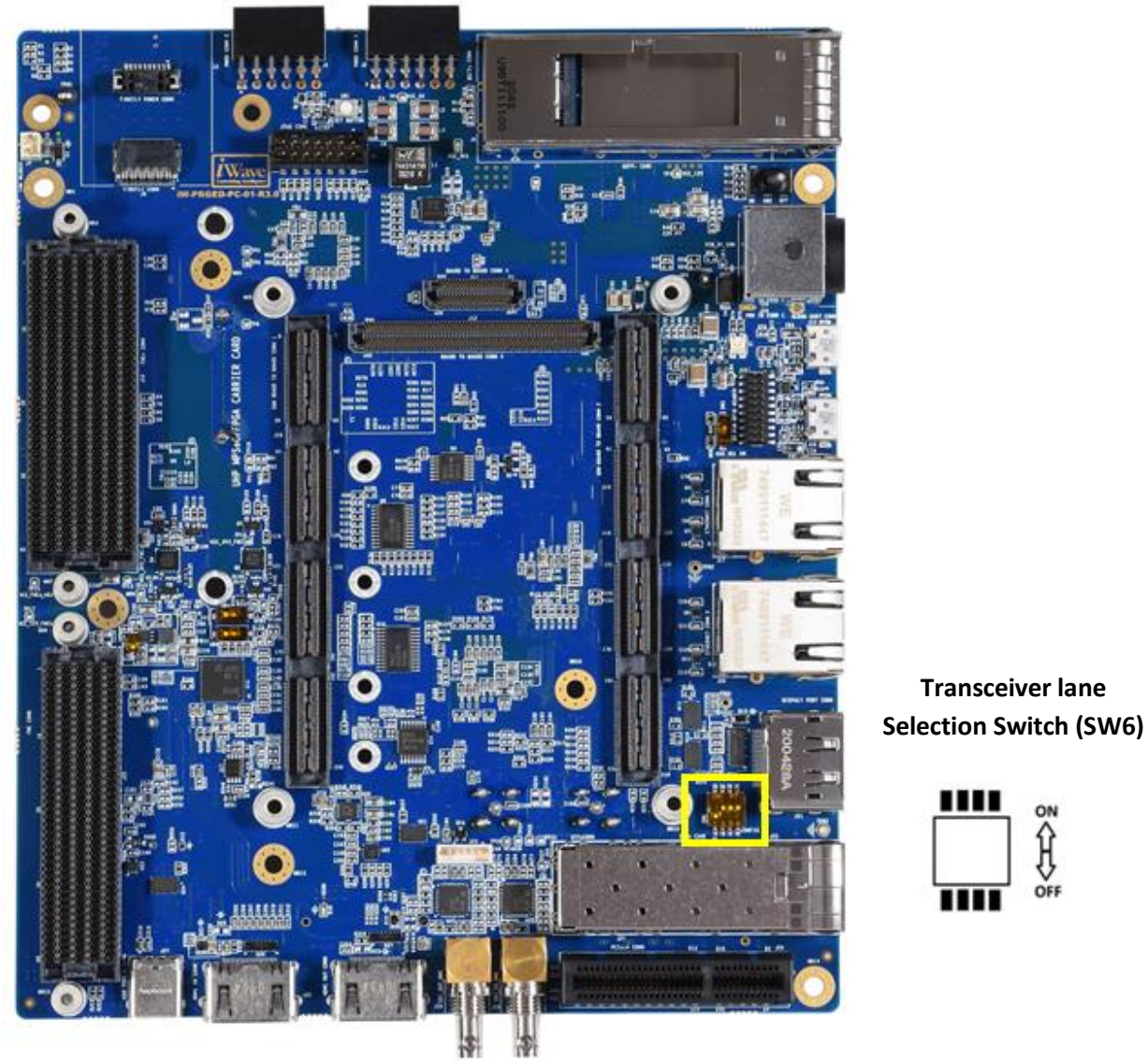

Figure 11: Transceiver Lane Selection Switch

2.5.2.1 PCIe x4 Connector (Not Supported)

In iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform eventhough there is provision available for one PCIe x4 connector, PCIe cannot be supported due to the limitations of CPU and transceivers mapped to the connector.

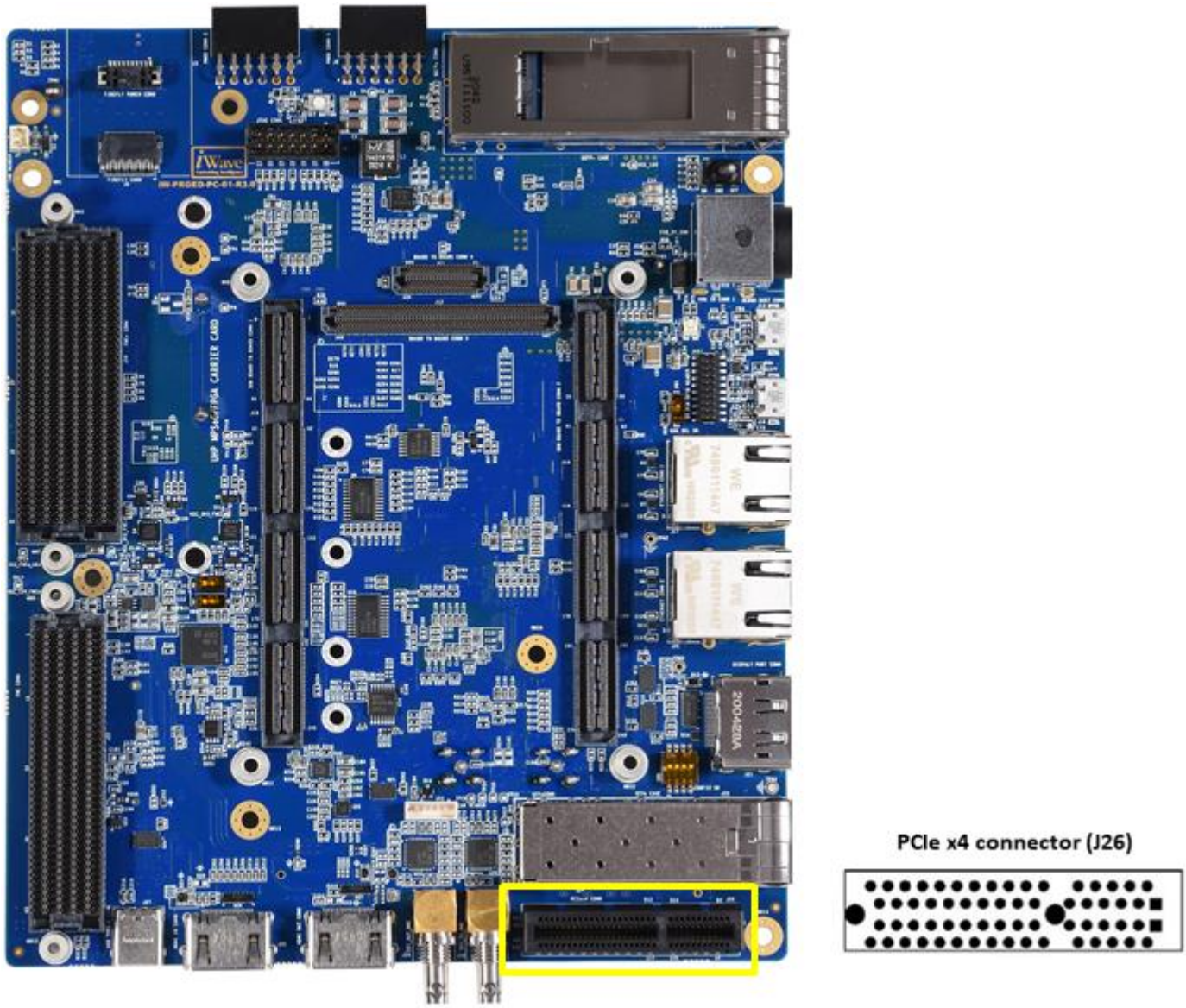

Figure 12: PCIe x4 Connector

Table 4: PCIe x4 Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	PRSNT1#	PRSNT1#	O, 3.3V CMOS	Default Grounded.
A2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A3	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
A4	GND	GND	Power	Ground.
A5	TCK	NA	NA	NC.
A6	TDI	NA	NA	NC.
A7	TDO	NA	NA	NC.
A8	TMS	NA	NA	NC.
A9	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A10	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
A11	PERST#	FPGA_LVDS3D_22p_IO5	O, 3.3V CMOS	PCIe Reset through FPGA Bank IO.
A12	GND	GND	Power	Ground.
A13	REFCLK+	PCIe_REFCLKP	O, DIFF	100MHz PCIe Reference Clock positive from clock synthesizer.
A14	REFCLK-	PCIe_REFCLKn	O, DIFF	100MHz PCIe Reference Clock negative from clock synthesizer.
A15	GND	GND	Power	Ground.
A16	PERp0	GXBL1M_RX_CH4p	I, DIFF	PCIe Lane0 Receive pair positive.
A17	PERn0	GXBL1M_RX_CH4n	I, DIFF	PCIe Lane0 Receive pair negative.
A18	GND	GND	Power	Ground.
A19	RSVD	NA	NA	NC.
A20	GND	GND	Power	Ground.
A21	PERp1	GXBL1K_RX_CH4p	NA	PCIe Lane1 Receive pair positive.
A22	PERn1	GXBL1K_RX_CH4n	NA	PCIe Lane1 Receive pair negative
A23	GND	GND	Power	Ground.
A24	GND	GND	Power	Ground.
A25	PERp2	GXBL1E_RX_CH3p	NA	PCIe Lane2 Receive pair positive.
A26	PERn2	GXBL1E_RX_CH3n	NA	PCIe Lane2 Receive pair negative.
A27	GND	GND	Power	Ground.
A28	GND	GND	Power	Ground.
A29	PERp3	GXBL1C_RX_CH4n	NA	PCIe Lane3 Receive pair positive.
A30	PERn3	GXBL1C_RX_CH4p	NA	PCIe Lane3 Receive pair negative.
A31	GND	GND	Power	Ground.
A32	RSVD	NA	NA	NC.
B1	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B2	+12V	VCC_12V	O, 12V Power	12V Supply Voltage.
B3	RSVD	NA	NA	NC.
B4	GND	GND	Power	Ground.
B5	SMCLK	I2C0_SD1_SCL	O, 3.3V CMOS	SMB Clock from I2C bus switch
B6	SMDAT	I2C0_SD1_SDA	IO, 3.3V CMOS	SMB Data from I2C bus switch
B7	GND	GND	Power	Ground.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
B8	+3V3	VCC_3V3	O, 3.3V Power	3.3V Supply Voltage.
B9	TRST#	NA	NA	NC.
B10	3V3AUX	VCC_3V3_AUX	O, 3.3V Power	3.3V Supply Voltage
B11	WAKE#	FPGA_LVDS3D_22n_IO6	O, 3.3V CMOS	PCIe Wake through FPGA Bank IO.
B12	RSVD	NA	NA	NC.
B13	GND	GND	Power	Ground.
B14	PETp0	GXBL1M_TX_CH4p	O, DIFF	PCIe Lane0 Transmit pair positive.
B15	PETn0	GXBL1M_TX_CH4n	O, DIFF	PCIe Lane0 Transmit pair negative.
B16	GND	GND	Power	Ground.
B17	PRSNT2	NA	NA	NC.
B18	GND	GND	Power	Ground.
B19	PETp1	GXBL1K_TX_CH4p	NA	PCIe Lane1 Transmit pair positive.
B20	PETn1	GXBL1K_TX_CH4n	NA	PCIe Lane1 Transmit pair negative
B21	GND	GND	Power	Ground.
B22	GND	GND	Power	Ground.
B23	PETp2	GXBL1E_TX_CH4p	NA	PCIe Lane2 Transmit pair positive.
B24	PETn2	GXBL1E_TX_CH4n	NA	PCIe Lane2 Transmit pair negative
B25	GND	GND	Power	Ground.
B26	GND	GND	Power	Ground.
B27	PETp3	GXBL1C_TX_CH4p	NA	PCIe Lane3 Transmit pair positive.
B28	PETn3	GXBL1C_TX_CH4n	NA	PCIe Lane3 Transmit pair negative
B29	GND	GND	Power	Ground.
B30	RSVD	NA	NA	NC.
B31	PRSNT#2	NA	NA	NC.
B32	GND	GND	Power	Ground.

2.5.2.2 Display Port Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one single lane Display port connector through 1K Bank Channel 4 of Stratix10 GX/SX SoC FPGA. Eventhough there is proviion available for two lanes, 2 lane DP cannot be supported due to the the lanes being from two different banks. The Transceiver Lane selection to Display port connector is done through the Transceiver Lane Selection Switch (SW6).

The Display port connector supports AUX+ & AUX- signals from the FPGA Bank IOs. Also, it supports Hot plug detect signal and connected to FPGA Bank IO. This Display Port connector (J21) is physically located at the top of the board as shown below.

*Note: For more details on the Transceiver Lane selection options, refer **Table 3**.*

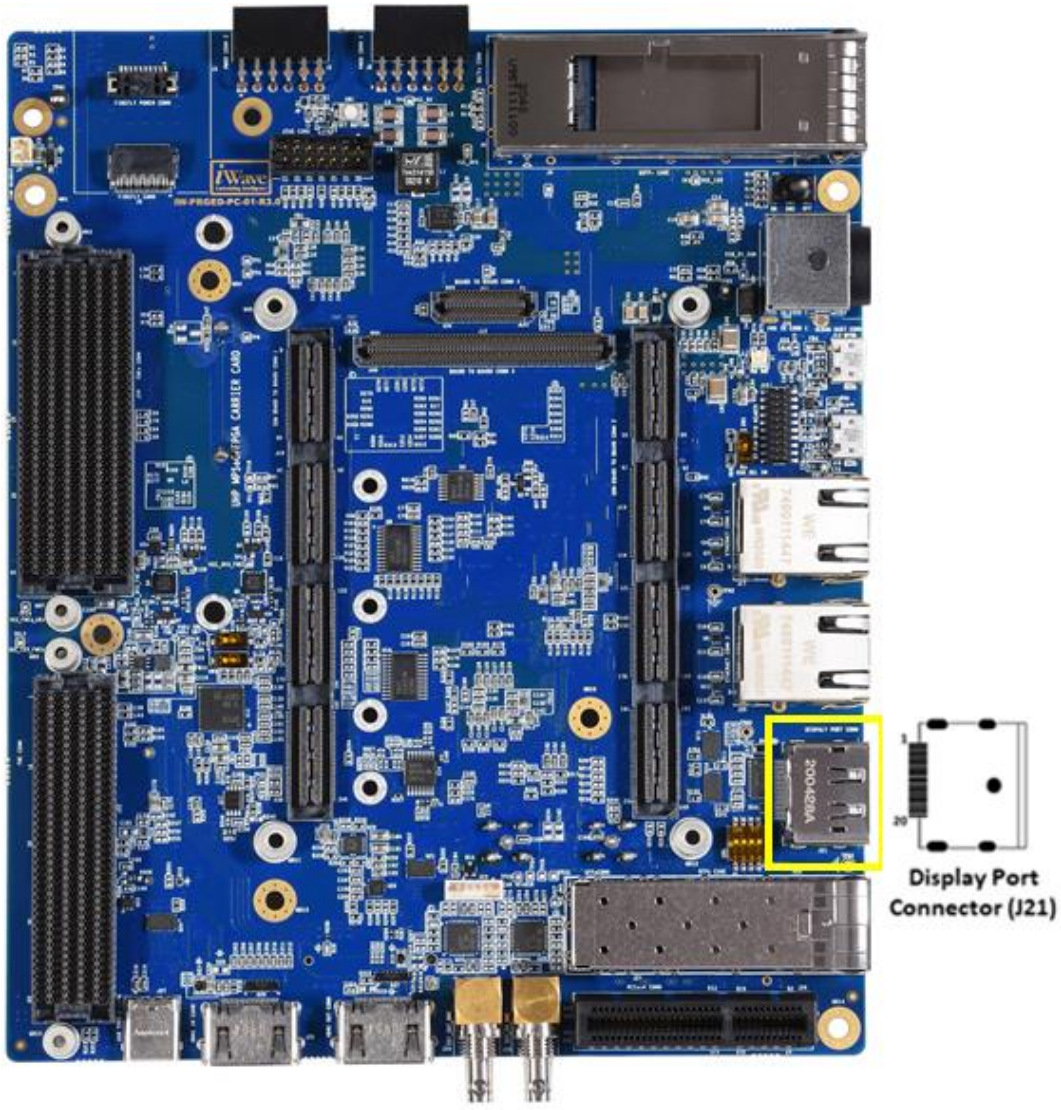

Figure 13: Display Port Connector

2.5.2.3 USB Type-C Connector (Not supported)

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform has hardware support available for one Super Speed USB3.0 OTG through USB Type-C connector. The 1E Bank Channel4 of Stratix10 GX/SX SoC FPGA connected to Board to Board Connector2 of the SOM can be used for USB3.0 OTG interface. The Lane2 selection to USB Type-C connector is done through the Transceiver Lane Selection Switch (SW6). Even though the option is made available, this feature s not implemented as IP is not available from Intel. For more details on Transceiver Lane selection options, refer **Table 3**.

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports “FUSB302” USB Type-C controller for port detection & cable orientation and controlled through I2C0 interface of the HPS. To support double-way plug in on USB Type-C connector, Transceiver Bank 1E Channel4 is connected to “FUSB340” 2:1 data Switch and then connected to USB Type-C connector. The lane selection to Type-C connector (top or bottom port) is controlled through FPGA Bank IO “FPGA_LVDS3D_4p_IO41” from Board to Board Connector1 pin70.

Also, USB2.0 OTG interface of the HPS of Stratix10 GX/SX SoC FPGA is connected to USB Type-C connector for backward compatible USB2.0 support. The USB2.0 PHY Transceiver output signals from Board to Board connector2 is connected to “FUSB340” USB Switch for selecting the USB2.0 OTG connection between USB2.0 MicroAB connector (J16) and USB3.0 Type-C connector (J27). The selection can be done by setting the Single bit DIP switch (SW3). If the DIP switch (SW3) is set to ON, USB2.0 OTG is connected to MicroAB connector (J16) and if the DIP switch (SW3) is set to OFF, USB2.0 OTG is connected to USB3.0 TypeC connector (J27).

The USB3.0 OTG port can be used as full functional OTG functionality which supports USB3.0 host and USB2.0 device based on Type-C . The VBUS power of this USB Type-C connector is connected through current limit power switch which can be used to switch On/Off the power based on the device or Host and also limits the current above 900mA in host mode. Enable pin of the USB Power switch is connected to the HPS GPIO “IO3V3_10” from Board-to-Board connector2 pin38. This USB Type-C connector (J27) is physically located at the top of the board as shown below.

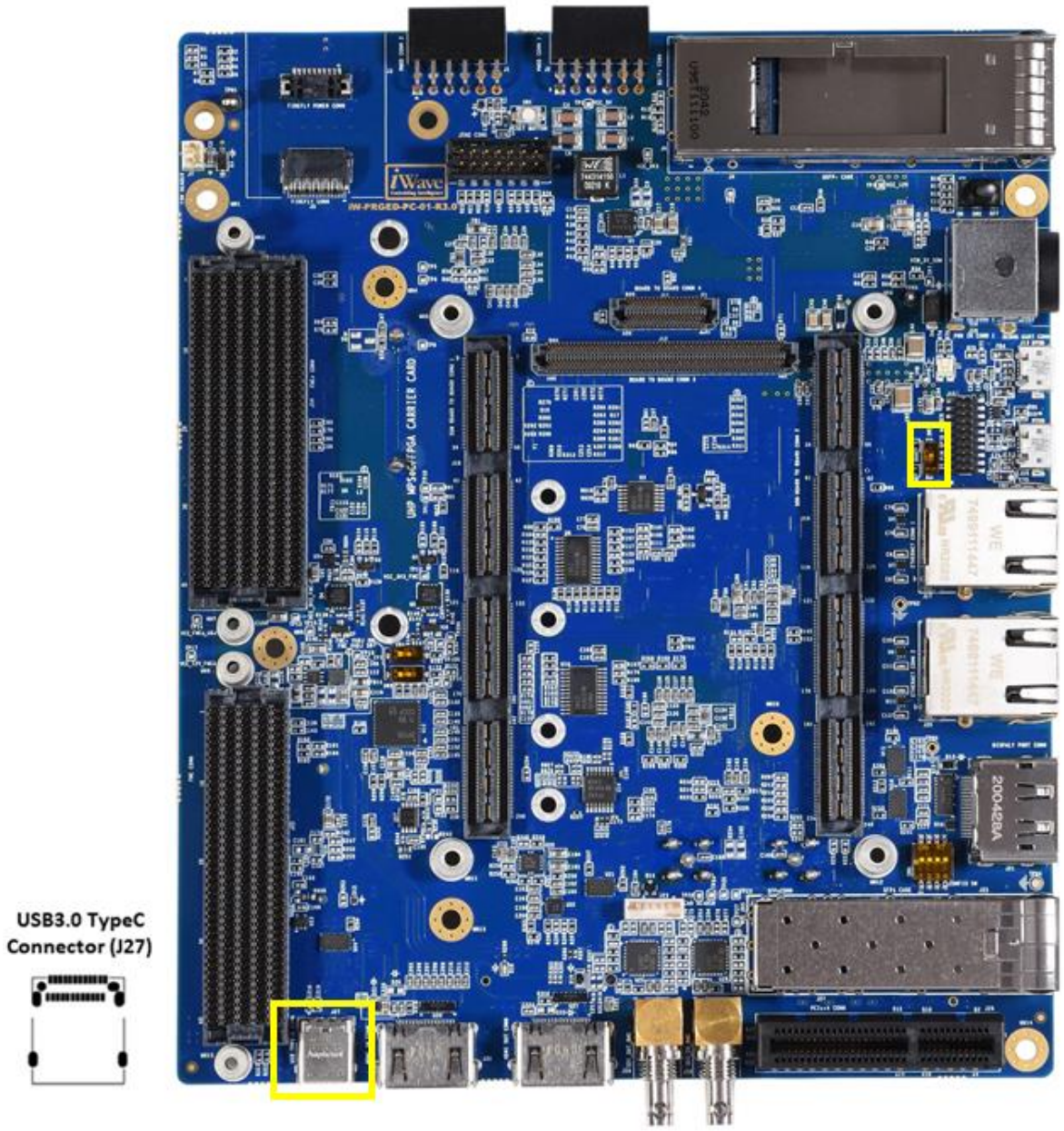

Figure 14: USB Type-C Connector

Table 5: USB TypeC Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
A1	GND	GND	Power	Ground.
A2	SSTXp1	GXBL1E_TX_CH4p	O, DIFF	USB3.0 Super Speed Transmit Data Positive.
A3	SSTXn1	GXBL1E_TX_CH4n	O, DIFF	USB3.0 Super Speed Transmit Data Negative.
A4	VBUS	VBUS_USB	Power	5V Power Supply.
A5	CC1	CC1	O, 5V CMOS	Configuration Channel pin1.
A6	Dp1	USB_OTG_DP	IO, DIFF	USB2.0 Transmit Data Positive.
A7	Dn1	USB_OTG_DM	IO, DIFF	USB2.0 Transmit Data Negative.
A8	SBU1	NC	NC	NC.
A9	VBUS	VBUS_USB	Power	5V Power Supply.
A10	SSRXn2	GXBL1E_RX_CH4n	I, DIFF	USB3.0 Super Speed Receive Data Negative.
A11	SSRXp2	GXBL1E_RX_CH4n	I, DIFF	USB3.0 Super Speed Receive Data Positive.
A12	GND	GND	Power	Ground.
B1	GND	GND	Power	Ground.
B2	SSTXp2	GXBL1E_TX_CH4p	O, DIFF	USB3.0 Super Speed Transmit Data Positive.
B3	SSTXn2	GXBL1E_TX_CH4n	O, DIFF	USB3.0 Super Speed Transmit Data Negative.
B4	VBUS	VBUS_USB	Power	5V Power Supply.
B5	CC2	CC2	O, 5V CMOS	Configuration Channel pin2.
B6	Dp2	USB_OTG_DP	IO, DIFF	USB2.0 Transmit Data Positive.
B7	Dn2	USB_OTG_DM	IO, DIFF	USB2.0 Transmit Data Negative.
B8	SBU2	NC	NC	NC.
B9	VBUS	VBUS_USB	Power	5V Power Supply.
B10	SSRXn1	GXBL1E_RX_CH4n	I, DIFF	USB3.0 Super Speed Receive Data Negative.
B11	SSRXp1	GXBL1E_RX_CH4n	I, DIFF	USB3.0 Super Speed Receive Data Positive.
B12	GND	GND	Power	Mechanical Pin.

2.5.2.4 M.2 SATA Connector (Not Supported)

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform has the hardware providion to support one SATA interface through M.2 (Key M) SATA connector. This support is not made available as IP is not available from Intel. Bank 1C Channel4 of Stratix10 SX/GX SoC FPGA is connected to the SATA interface. The Transceiver Lane selection to M.2 SATA connector is done through Transceiver Lane Selection Switch (SW6). For more details on Transceiver Lane selection options, refer **Table 3**. This M.2 SATA connector (J36) is physically located at the bottom of the board as shown below.

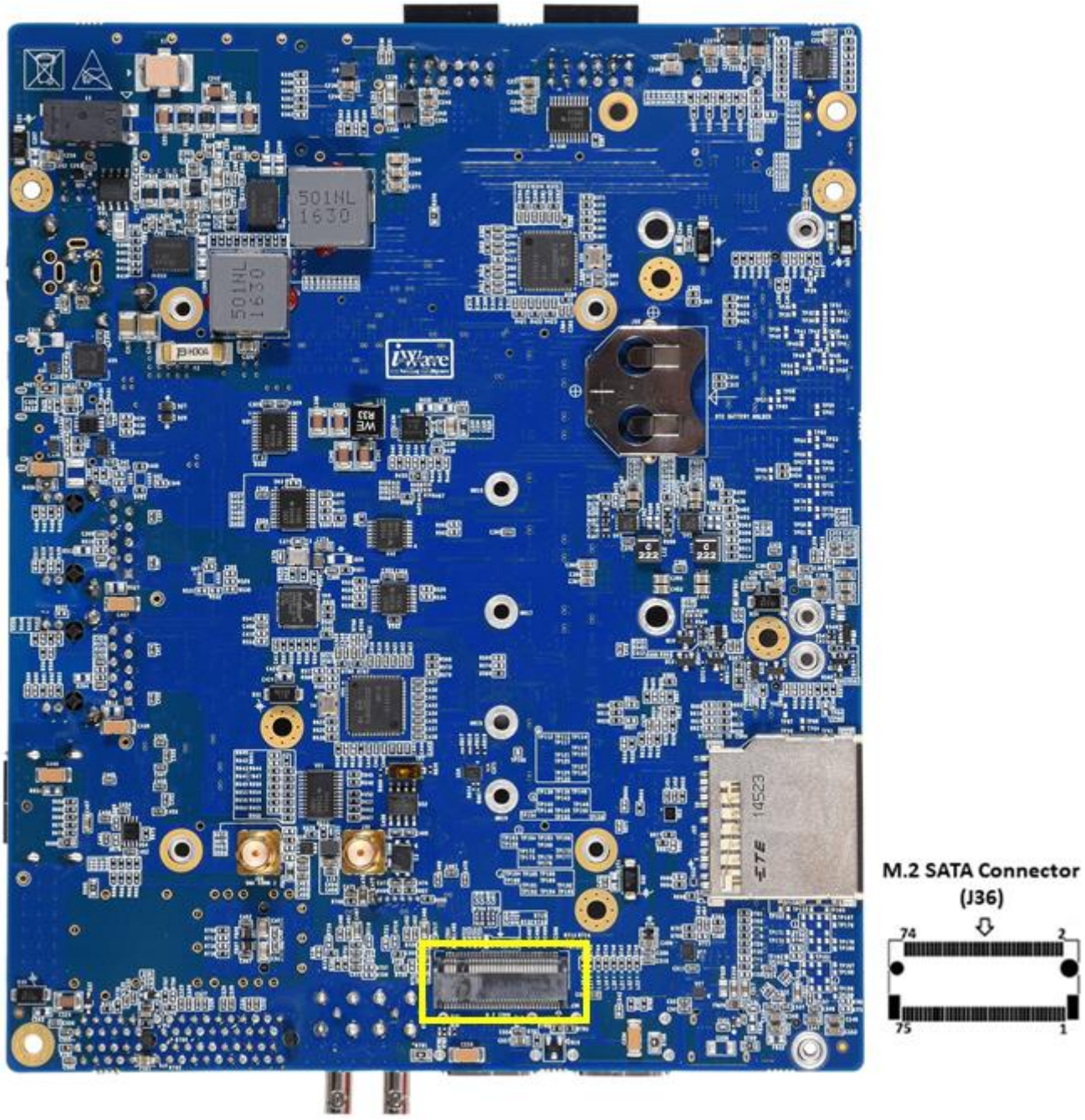

Figure 15: M.2 SATA Connector (Key M)

Table 6: M.2 SATA Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	CONFIG_3	NA	NA	NC
2	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
3	GND	GND	Power	Ground.
4	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
5	PERn3	NA	NA	NC.
6	N/A1	NA	NA	NC.
7	PERp3	NA	NA	NC.
8	N/A2	NA	NA	NC.
9	GND	GND	Power	Ground.
10	DAS/DSS	DAS	IO, 3.3V CMOS	Connected to LED D20 for the activity indication
11	PETn3	NA	NA	NC.
12	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
13	PETp3	NA	NA	NC.
14	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
15	GND	GND	Power	Ground.
16	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
17	PERn2	NA	NA	NC.
18	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
19	PERp2	NA	NA	NC.
20	N/A3	NA	NA	NC.
21	CONFIG_0	NA	NA	NC
22	N/A4	NA	NA	NC.
23	PETn2	NA	NA	NC.
24	N/A5	NA	NA	NC.
25	PETp2	NA	NA	NC.
26	N/A6	NA	NA	NC.
27	GND	GND	Power	Ground.
28	N/A7	NA	NA	NC.
29	PERn1	NA	NA	NC.
30	N/A8	NA	NA	NC.
31	PERp1	NA	NA	NC.
32	N/A9	NA	NA	NC.
33	GND	GND	Power	Ground.
34	N/A10	NA	NA	NC.
35	PETn1	NA	NA	NC.
36	N/A11	NA	NA	NC.
37	PETp1	NA	NA	NC.
38	DEVSLP	NA	NA	NC.
39	GND	GND	Power	Ground.
40	SMB_CLK	NA	NA	NC.

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
41	SATA-B+/PERn0	GXBL1C_RX_CH4p	I, DIFF	SATA Receive pair positive.
42	SMB_DATA	NA	NA	NC.
43	SATA-B-/PERp0	GXBL1C_RX_CH4n	I, DIFF	SATA Receive pair negative.
44	N/A14	NA	NA	NC.
45	GND	GND	Power	Ground.
46	N/A15	NA	NA	NC.
47	SATA-A-/PETn0	GXBL1C_TX_CH4n	O, DIFF	SATA Transmit pair negative.
48	N/A16	NA	NA	NC.
49	SATA-A+/PETp0	GXBL1C_TX_CH4p	O, DIFF	SATA Transmit pair positive.
50	PERST#	B_M2_PCI_RST#	O, 3.3V CMOS	This pin is connected to IO Expander port 14
51	GND	GND	Power	Ground.
52	CLKREQ#	B_PCI_CLKREQ#	I, 3.3V CMOS	This pin is connected to IO Expander port 16
53	REFCLKN	M2_PCIe_REFCLKn	O, DIFF	PCIe reference clock pair negative.
54	PEWAKE#	B_M2_PCI_WAK#	O, 3.3V CMOS	This pin is connected to IO Expander port 15
55	REFCLKP	M2_PCIe_REFCLKP	O, DIFF	PCIe reference clock pair positive.
56	MFG1	NA	NA	NC.
57	GND	GND	Power	Ground.
58	MFG2	NA	NA	NC.
59	M1	NA	NA	NC.
60	M2	NA	NA	NC.
61	M3	NA	NA	NC.
62	M4	NA	NA	NC.
63	M5	NA	NA	NC.
64	M6	NA	NA	NC.
65	M7	NA	NA	NC.
66	M8	NA	NA	NC.
67	N/A17	NA	NA	NC.
68	SUSCLK	NA	NA	NC.
69	CONFIG_1	PCI/SATA_CONFIG	Power, 10K PU	This pin is connected to VCC_3V3
70	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
71	GND	GND	Power	Ground.
72	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
73	GND	GND	Power	Ground.
74	3.3V	VCC_3V3	O, 3.3V Power	Supply Voltage.
75	CONFIG_2	NA	NA	NC

2.5.2.5 SFP+ Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one SFP+ Connector through 1C Bank of Stratix10 GX/SX SoC FPGA. The transceiver Channel2 of FPGA Bank1C connected to the Board to Board Connector2 is connected to SFP+ connector. Also HPS I2C0 is connected to this connector for control and configuration. All other contorl signals of SFP+ connnector is connected from IO Expander. This SFP+ connector with dust case (J25) is physically located at the top of the board as shown below.

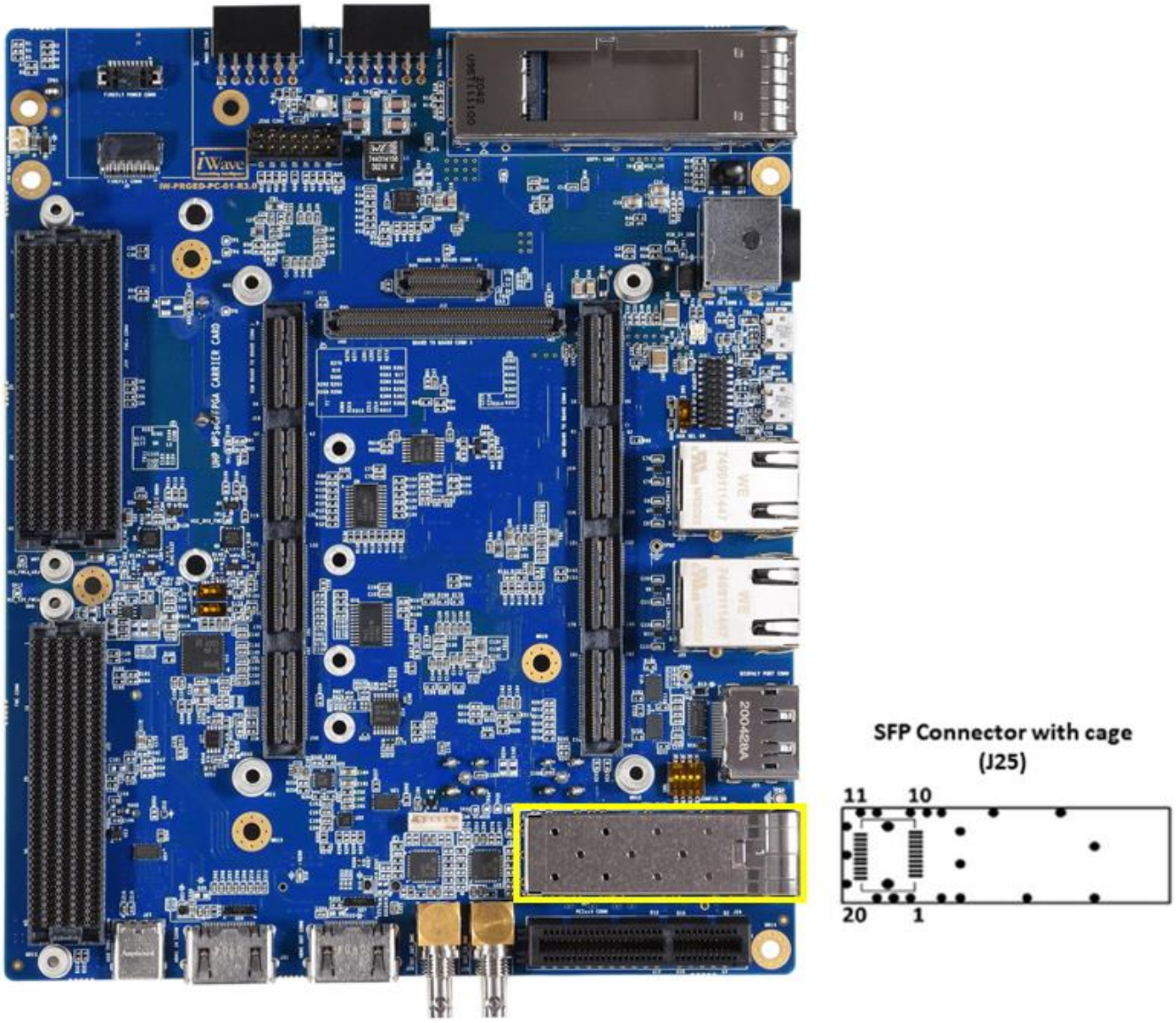

Figure 16: SFP+ Connector with Cage

Table 7: SFP+ Connector Pin Assignment

Pin No	Pin Name	Signal Name	Signal Type/ Termination	Description
1	VEET1	GND	Power	Ground.
2	TFAULT	IOEXP_P00_SFP_TFAULT	I, LVTTL/ 4.7K PU	Module Transmitter Fault. This Pin is connected to IO Expander1 Port 0 for software access if required.
3	TDIS	IOEXP_P05_SFP_TDIS	O, LVTTL/ 4.7K PD	Transmitter Disable. This Pin is connected to IO Expander1 Port 5 for software control if required.
4	SDA	I2C0_SD2_SDA	IO, 3.3V CMOS	I2C Data. This Pin is connected from 9th pin of I2C Bus switch (U29).
5	SCL	I2C0_SD2_SCL	O, 3.3V CMOS	I2C Clock. This Pin is connected from 10th pin of I2C Bus switch (U29).
6	MOD_ABS	IOEXP_P02_SFP_MOD_ABS	I, 3.3V CMOS/ 4.7K PU	Module Definition. This Pin is connected to IO Expander1 Port 2 for software access if required.
7	RS0	IOEXP_P04_SFP_RS0	O, 3.3V CMOS/ 4.7K PU	Rate select 0. This Pin is connected to IO Expander1 Port 4 for software control if required.
8	RX_LOS	IOEXP_P01_SFP_RX_LOS	I, 3.3V CMOS/ 4.7K PU	Receiver loss of signal indication. This Pin is connected to IO Expander1 Port 1 for software access if required.
9	RS1	IOEXP_P03_SFP_RS1	O, 3.3V CMOS/ 4.7K PU	Rate select 1. This Pin is connected to IO Expander1 Port 3 for software control if required.
10	VEER1	GND	Power	Ground.
11	VEER2	GND	Power	Ground.
12	RD-	GXBL1C_RX_CH2n	I, DIFF	SFP+ Receiver Data Negative
13	RD+	GXBL1C_RX_CH2p	I, DIFF	SFP+ Receiver Data Positive
14	VEER3	GND	Power	Ground.
15	VCCR	VCC_3V3	O, 3.3V Power	3.3V Receiver Supply Voltage
16	VCCT	VCC_3V3	O, 3.3V Power	3.3V Transmitter Supply Voltage
17	VEET2	GND	Power	Ground.
18	TD+	GXBL1C_TX_CH2p	O, DIFF	SFP+ Transmit Data Positive
19	TD-	GXBL1C_TX_CH2n	O, DIFF	SFP+ Transmit Data Negative
20	VEET3	GND	Power	Ground.

2.5.2.6 SDI Video IN

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one 3G/12G SDI Video IN interface through HD BNC connector (J29). The Video input signals from HD BNC Connector is directly connected to Adaptive Cable Equalizer chip and then connected to the receiver Channel3 of Transceiver Bank1C of Stratix10 GX/SX SoC FPGA through Board to Board connector2.

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports Video Input Lock status LED (D17) for presence and absence of the Video Input signal on HD BNC connector (J29). This LED will glow when the Video Input signal is detected on HD BNC connector (J29). Also HPS I2C0 is connected to Adaptive Cable Equalizer chip for control and configuration with I2C address 0x2D. SDI Video IN HD BNC connector (J29) is physically located at the top of the board as shown below.

Note: By default, 12G Adaptive Cable Equalizer chip "LMH1297" is supported on the board. To support 3G Adaptive Cable Equalizer chip "LMH0397", contact iWave.

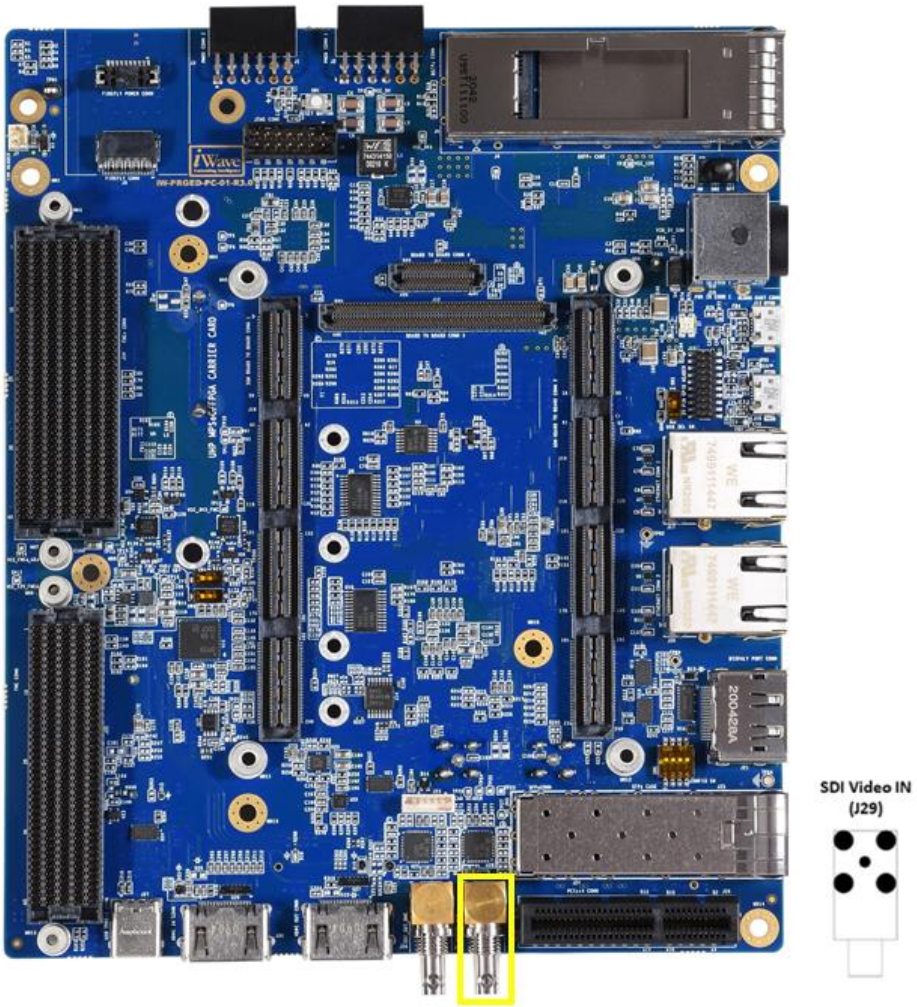

Figure 17: SDI Video IN HD BNC Connector

2.5.2.7 SDI Video Out

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one 3G/12G SDI Video OUT interface through HD BNC connector (J28). Channel3 Transmitter from the Bank1C of Stratix10 GX/SX SoC FPGA connected to Board to Board connector2 is directly connected to Cable Driver chip and then connected to HD BNC Connector (J28) for Video out.

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports Video Output Lock status LED (D16). This LED will glow when the video signal from Stratix10 GX/SX SoC FPGA transmitter is detected on Cable Driver chip. Also HPS I2C0 is connected to Cable Driver chip for control and configuration with I2C address 0x30. SDI Video OUT HD BNC connector (J28) is physically located at the top of the board as shown below.

Note: By default, 12G Adaptive Cable Equalizer chip "LMH1297" is supported on the board. To support 3G Adaptive Cable Equalizer chip "LMH0397", contact iWave.

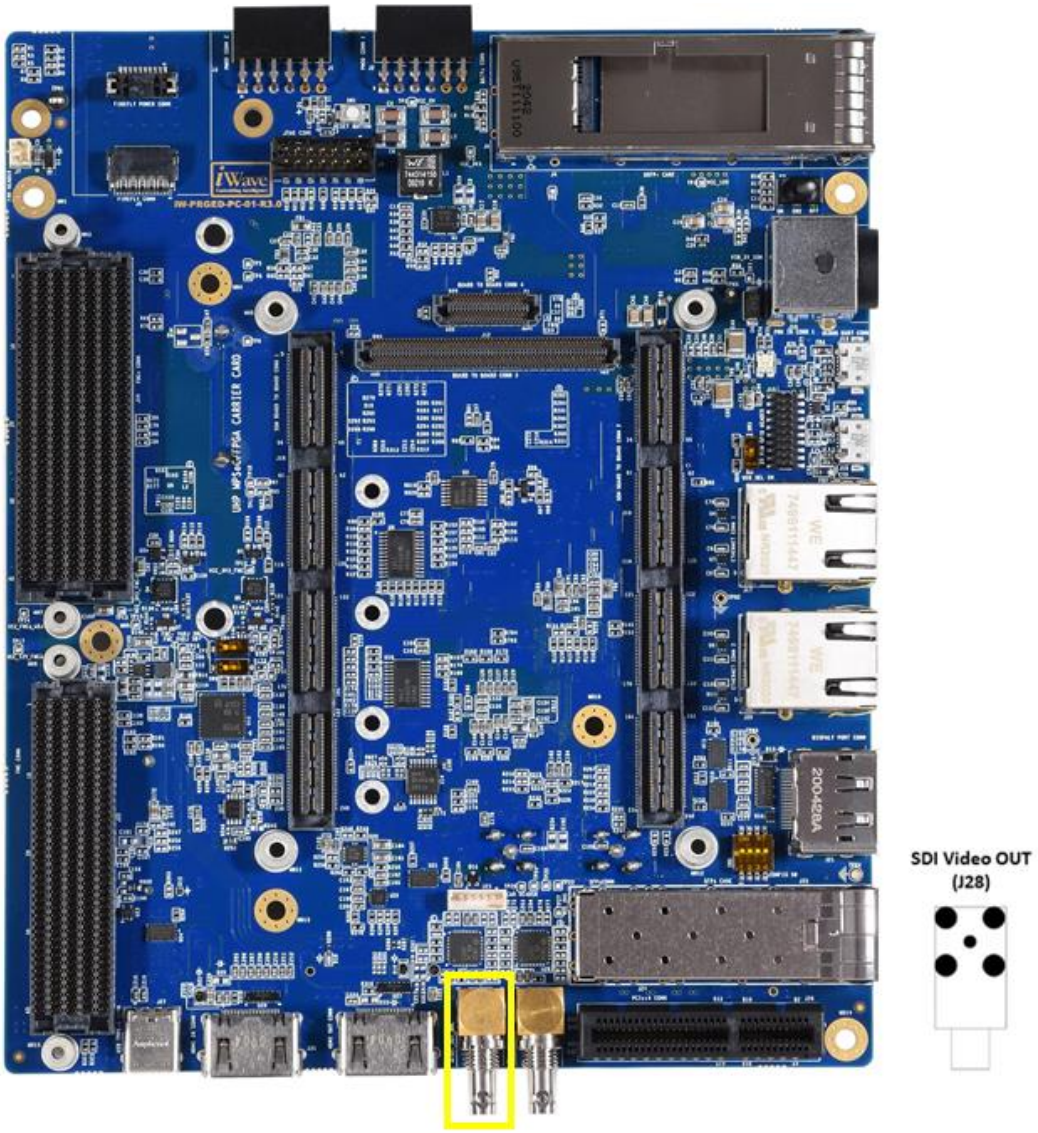

Figure 18: SDI Video OUT HD BNC Connector

2.5.2.8 QSFP28/QSFP+/QSFP Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one QSFP28/QSFP+/QSFP Connector through GX/GXT Transceivers of iW-RainboW-G45M-Stratix10 SoC FPGA SOM. GX/GXT Transceivers of FPGA Bank1D Channel 0, 1, 3 and 4 from Board-to-Board Connector3 is connected to QSFP+ connector. Also HPS I2C0 is connected to this connector for control and configuration. All other control signals of QSFP+ connnector is connected from IO Expander. This QSFP+ connector with dust case (J4) is physically located at the top of the board as shown below.

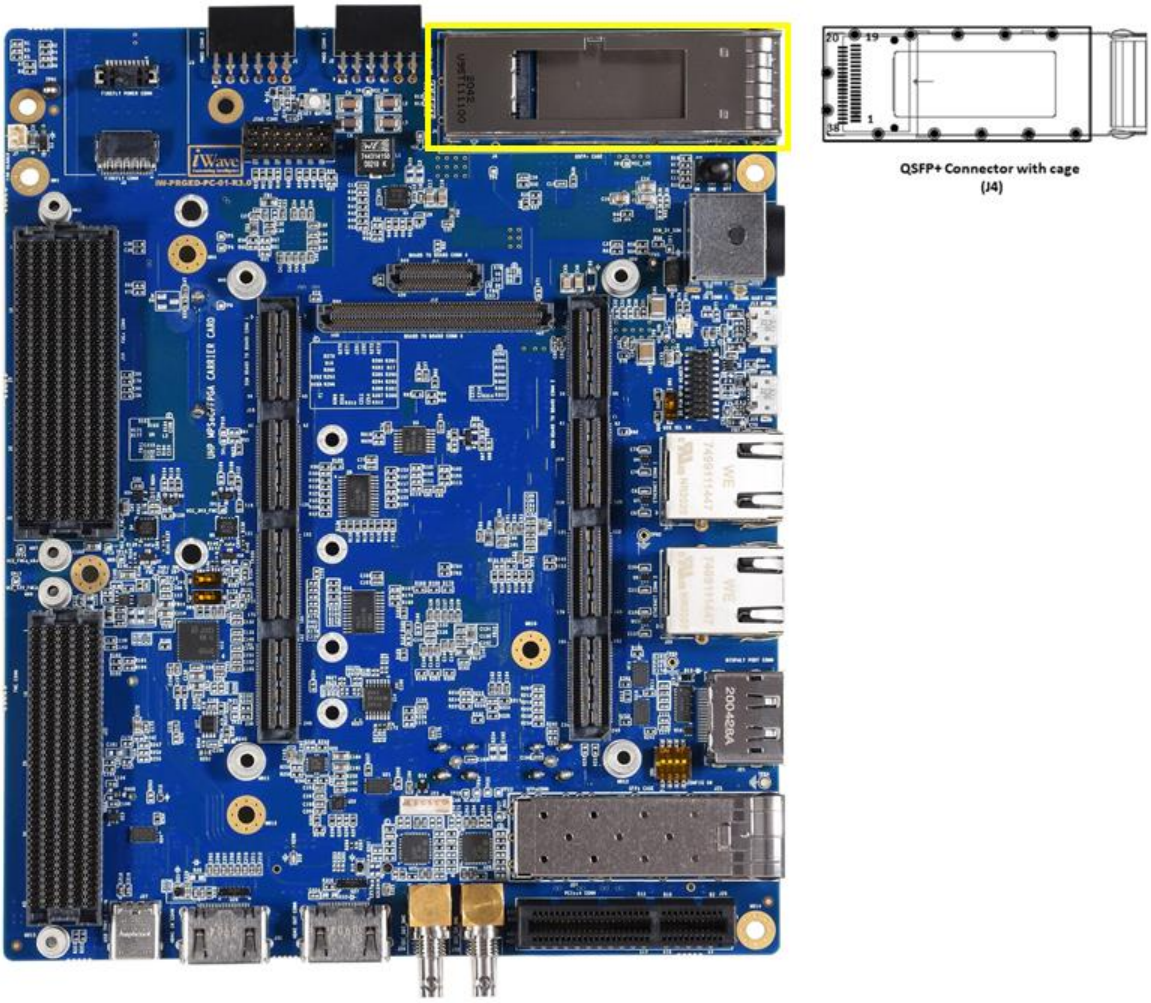

Figure 19 QSFP28/QSFP+/QSFP+ Connector with Cage

Table 8 QSFP28/QSFP+/QSFP Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	GND1	GND	Power	Ground.
2	Tx2n	GXBL1D_TX_CH1n	O, DIFF	QSFP+ Transmit2 Data Negative
3	Tx2p	GXBL1D_TX_CH1p	O, DIFF	QSFP+ Transmit2 Data Positive.
4	GND2	GND	Power	Ground.
5	Tx4n	GXBL1D_TX_CH4n	O, DIFF	QSFP+ Transmit4 Data Negative
6	Tx4p	GXBL1D_TX_CH4p	O, DIFF	QSFP+ Transmit4 Data Positive.
7	GND3	GND	Power	Ground.
8	ModSelL	IOEXP_P00_Q_MODESEL	I, 3.3V CMOS/ 4.7K PD	Module select. This Pin is connected to IO Expander2 Port 0 for software access if required
9	ResetL	IOEXP_P01_Q_RESETL	I, 3.3V CMOS/ 4.7K PU	Module reset. This Pin is connected to IO Expander2 Port 1 for software access if required
10	Vcc Rx	VCCRX_3V3	O, 3.3V Power	3.3V Receiver Supply Voltage
11	SCL	I2C0_SD0_SDA	O, 3.3V CMOS	I2C Clock. This Pin is connected from 4th pin of I2C Bus switch (U29).
12	SDA	I2C0_SD0_SCL	IO, 3.3V CMOS	I2C Data. This Pin is connected from 5th pin of I2C Bus switch (U29).
13	GND4	GND	Power	Ground.
14	Rx3p	GXBL1D_RX_CH3p	I, DIFF	QSFP+ Receiver3 Data Positive
15	Rx3n	GXBL1D_RX_CH3n	I, DIFF	QSFP+ Receiver3 Data Negative
16	GND5	GND	Power	Ground.
17	Rx1p	GXBL1D_RX_CH0p	I, DIFF	QSFP+ Receiver1 Data Positive
18	Rx1n	GXBL1D_RX_CH0n	I, DIFF	QSFP+ Receiver1 Data Negative
19	GND6	GND	Power	Ground.
20	GND7	GND	Power	Ground.
21	Rx2n	GXBL1D_RX_CH1n	I, DIFF	QSFP+ Receiver2 Data Negative
22	Rx2p	GXBL1D_RX_CH1p	I, DIFF	QSFP+ Receiver2 Data Positive
23	GND8	GND	Power	Ground.
24	Rx4n	GXBL1D_RX_CH4n	I, DIFF	QSFP+ Receiver4 Data Negative
25	Rx4p	GXBL1D_RX_CH4p	I, DIFF	QSFP+ Receiver4 Data Positive
26	GND9	GND	Power	Ground.
27	ModPrsL	IOEXP_P04_Q_MODPRSL	I, 3.3V CMOS/ 4.7K PU	Module present. This Pin is connected to IO Expander2 Port 4 for software access if required
28	IntL	IOEXP_P03_Q_INTL	I, 3.3V CMOS/ 4.7K PU	Module Interrupt. This Pin is connected to IO Expander2 Port 3 for software access if required
29	Vcc Tx	VCCTX_3V3	O, 3.3V Power	3.3V Transmit Supply Voltage

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
30	Vcc1	VCC1_3V3	O, 3.3V Power	3.3V Supply Voltage
31	LPMode	IOEXP_P02_Q_LPMODE	I, 3.3V CMOS/ 4.7K PD	Module Low power mode. This Pin is connected to IO Expander2 Port 2 for software access if required
32	GND10	GND	Power	Ground.
33	Tx3p	GXBL1D_TX_CH3p	O, DIFF	QSFP+ Transmit3 Data Positive.
34	Tx3n	GXBL1D_TX_CH3n	O, DIFF	QSFP+ Transmit3 Data Negative.
35	GND11	GND	Power	Ground.
36	Tx1p	GXBL1D_TX_CH0p	O, DIFF	QSFP+ Transmit1 Data Positive
37	Tx1n	GXBL1D_TX_CH0n	O, DIFF	QSFP+ Transmit1 Data Negative.
38	GND12	GND	Power	Ground.

2.5.2.9 FireFly Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one FireFly Connector through Transceiver banks 1D, 1F, 1L, 1N of Stratix10 GX/SX SoC FPGA. Channel 2 of the Transceiver Bank 1D, 1F, 1L and 1N from Board-to-Board Connector3 is connected to FireFly data connector(J5). Also HPS I2C0 is connected to this connector for control and configuration. All other contorl signals of FireFly connnector is connected from IO Expander. And FireFly module power is supplied from FireFly power connector (J3). This FireFly data with power connector (J5) is physically located at the top of the board as shown below.

Note: The applications using the Firefly connector may be limited as the transceiver lanes are from 4 different banks.

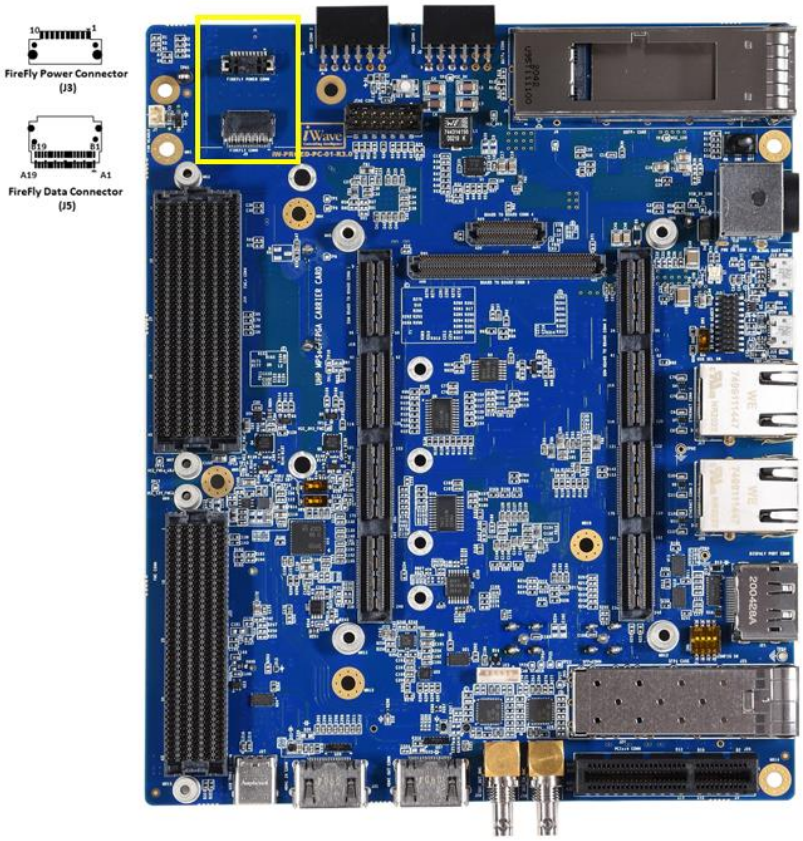

Figure 20 FireFly Connector

Table 9 FireFly Data Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
A1	GND_1	GND	Power	Ground.
A2	TX1N	GXBL1D_TX_CH2n	O, DIFF	FireFly Transmit1 Data Negative
A3	TX1P	GXBL1D_TX_CH2p	O, DIFF	FireFly Transmit1 Data Positive.
A4	GND_2	GND	Power	Ground.
A5	TX3N	GXBL1F_TX_CH2n	O, DIFF	FireFly Transmit3 Data Negative
A6	TX3P	GXBL1F_TX_CH2p	O, DIFF	FireFly Transmit3 Data Positive.
A7	GND_3	GND	Power	Ground.
A8	RSVD_1	NA	NA	NC
A9	RSVD_2	NA	NA	NC
A10	RSVD_3	NA	NA	NC
A11	RSVD_4	NA	NA	NC
A12	RSVD_5	NA	NA	NC
A13	GND_4	GND	Power	Ground.
A14	RX4P	GXBL1N_RX_CH2p	I, DIFF	FireFly Receiver4 Data Positive
A15	RX4N	GXBL1N_RX_CH2n	I, DIFF	FireFly Receiver4 Data Negative
A16	GND_5	GND	Power	Ground.
A17	RX2P	GXBL1F_RX_CH2p	I, DIFF	FireFly Receiver2 Data Positive
A18	RX2N	GXBL1F_RX_CH2n	I, DIFF	FireFly Receiver2 Data Negative
A19	GND_6	GND	Power	Ground.
B1	GND_7	GND	Power	Ground.
B2	TX2N	GXBL1F_TX_CH2n	O, DIFF	FireFly Transmit2 Data Negative
B3	TX2P	GXBL1F_TX_CH2p	O, DIFF	FireFly Transmit2 Data Positive.
B4	GND_8	GND	Power	Ground.
B5	TX4N	GXBL1N_TX_CH2n	O, DIFF	FireFly Transmit4 Data Negative
B6	TX4P	GXBL1N_TX_CH2p	O, DIFF	FireFly Transmit4 Data Positive.
B7	GND_9	GND	Power	Ground.
B8	RSVD_6	NA	NA	NC
B9	RSVD_7	NA	NA	NC
B10	RSVD_8	NA	NA	NC
B11	RSVD_9	NA	NA	NC
B12	RSVD_10	NA	NA	NC
B13	GND_10	GND	Power	Ground.
B14	RX3P	GXBL1L_RX_CH2p	I, DIFF	FireFly Receiver3 Data Positive
B15	RX3N	GXBL1L_RX_CH2n	I, DIFF	FireFly Receiver3 Data Negative
B16	GND_11	GND	Power	Ground.
B17	RX1P	GXBL1D_RX_CH2p	I, DIFF	FireFly Receiver1 Data Positive
B18	RX1N	GXBL1D_RX_CH2n	I, DIFF	FireFly Receiver1 Data Negative
B19	GND_12	GND	Power	Ground.

Table 10 FireFly Power Connector Pin Out

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
1	VCC_TX	VCCTX_F_3V3	O, 3.3V Power	3.3V Transmit Supply Voltage
2	GND_14	GND	Power	Ground
3	MODPRS	IOEXP_P10_F_MODPRS	I, 3.3V CMOS/ 4.7K PU	FireFly Module Present. This Pin is connected to IO Expander2 Port 10 for software access if required
4	MODSEL	IOEXP_P06_F_MODSEL	I, 3.3V CMOS/ 4.7K PU	FireFly Module Select. This Pin is connected to IO Expander2 Port 6 for software access if required
5	INTL	IOEXP_P07_F_INTL	I, 3.3V CMOS/ 4.7K PU	FireFly Module Interrupt. This Pin is connected to IO Expander2 Port 7 for software access if required
6	RESETL	IOEXP_P05_F_RESETL	I, 3.3V CMOS/ 4.7K PU	FireFly Module Reset. This Pin is connected to IO Expander2 Port 5 for software access if required
7	SDA	I2C0_SD1_SDA	IO, 3.3V CMOS	I2C Data. This Pin is connected from 6th pin of I2C Bus switch (U29).
8	SCL	I2C0_SD1_SCL	O, 3.3V CMOS	I2C Clock. This Pin is connected from 7th pin of I2C Bus switch (U29).
9	VCC_1.8V	VCC_F_1V8	O, 3.3V Power	1.8 V supply
10	VCC_RX	VCCRX_F_3V3	O, 3.3V Power	3.3V Receiver Supply Voltage

2.5.3 Pmod Host Port Connectors

Pmod interface or Peripheral Module interface is a standard defined by Digilent Inc The Pmod interface is used to connect low frequency, low I/O pin count peripheral modules to host controller boards. There are twelve-pin of the interface defined, encompassing SPI, I²C, UART, I2S and GPIO protocols.

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports two 12pin Pmod host port connector for plugging Pmod modules. Since Pmod interface specification requires 3.3V IO level, the signals from Board-to-Board connector are connected to Pmod Connectors through Voltage level translator. Pmod Host port connector1 (J2) and Connector2 (J1) are physically located at the top of the board as shown below.

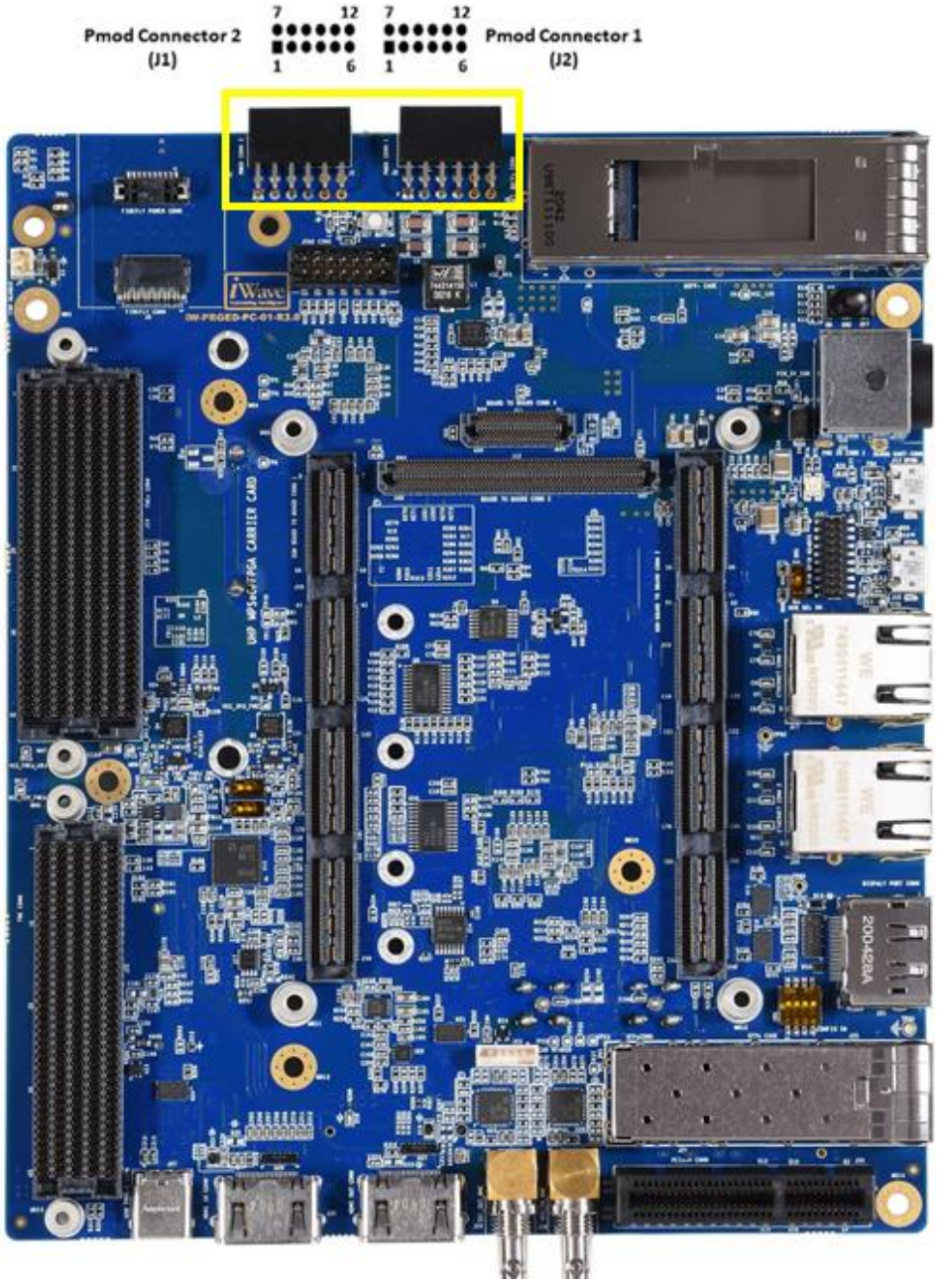

Figure 21: Pmod Host Port Connectors

Table 11: Pmod Connector1 Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	FPGA_LVDS2B_4n_IO42	IO, 3V3 LVCMOS	General purpose Input Output.
2	FPGA_LVDS2B_3n_IO44	IO, 3V3 LVCMOS	General purpose Input Output.
3	FPGA_LVDS2B_2n_IO46	IO, 3V3 LVCMOS	General purpose Input Output.
4	FPGA_LVDS2B_1n_IO48	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	FPGA_LVDS2B_4p_IO41	IO, 3V3 LVCMOS	General purpose Input Output.
8	FPGA_LVDS2B_3p_IO43	IO, 3V3 LVCMOS	General purpose Input Output.
9	FPGA_LVDS2B_2p_IO45	IO, 3V3 LVCMOS	General purpose Input Output.
10	FPGA_LVDS2B_1p_IO47	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

Table 12: Pmod Connector2 Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	FPGA_LVDS2B_7n_IO36	IO, 3V3 LVCMOS	General purpose Input Output.
2	FPGA_LVDS2B_9p_IO31	IO, 3V3 LVCMOS	General purpose Input Output.
3	FPGA_LVDS2B_6n_IO38	IO, 3V3 LVCMOS	General purpose Input Output.
4	FPGA_LVDS2B_5n_IO40	IO, 3V3 LVCMOS	General purpose Input Output.
5	GND	Power	Ground.
6	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
7	FPGA_LVDS2B_9n_IO32	IO, 3V3 LVCMOS	General purpose Input Output.
8	FPGA_LVDS2B_7p_IO35	IO, 3V3 LVCMOS	General purpose Input Output.
9	FPGA_LVDS2B_6p_IO37	IO, 3V3 LVCMOS	General purpose Input Output.
10	FPGA_LVDS2B_5p_IO39	IO, 3V3 LVCMOS	General purpose Input Output.
11	GND	Power	Ground.
12	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.

2.5.4 SMA Connectors

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports two SMA Connectors through transceiver Bank 1E of -Stratix10 GX/SX SoC FPGA. Channel 3 of Transceiver bank 1E is connected to the SMA Connectors.

Channel3-TXP from Board-to-Board Connector1 is connected to SMA Connector (J34) and and Channel3-TXN from Board-to-Board Connector1 is connected to SMA Connector (J35) . SMA connectors (J34 & J35) are physically located at the bottom of the board as shown below.

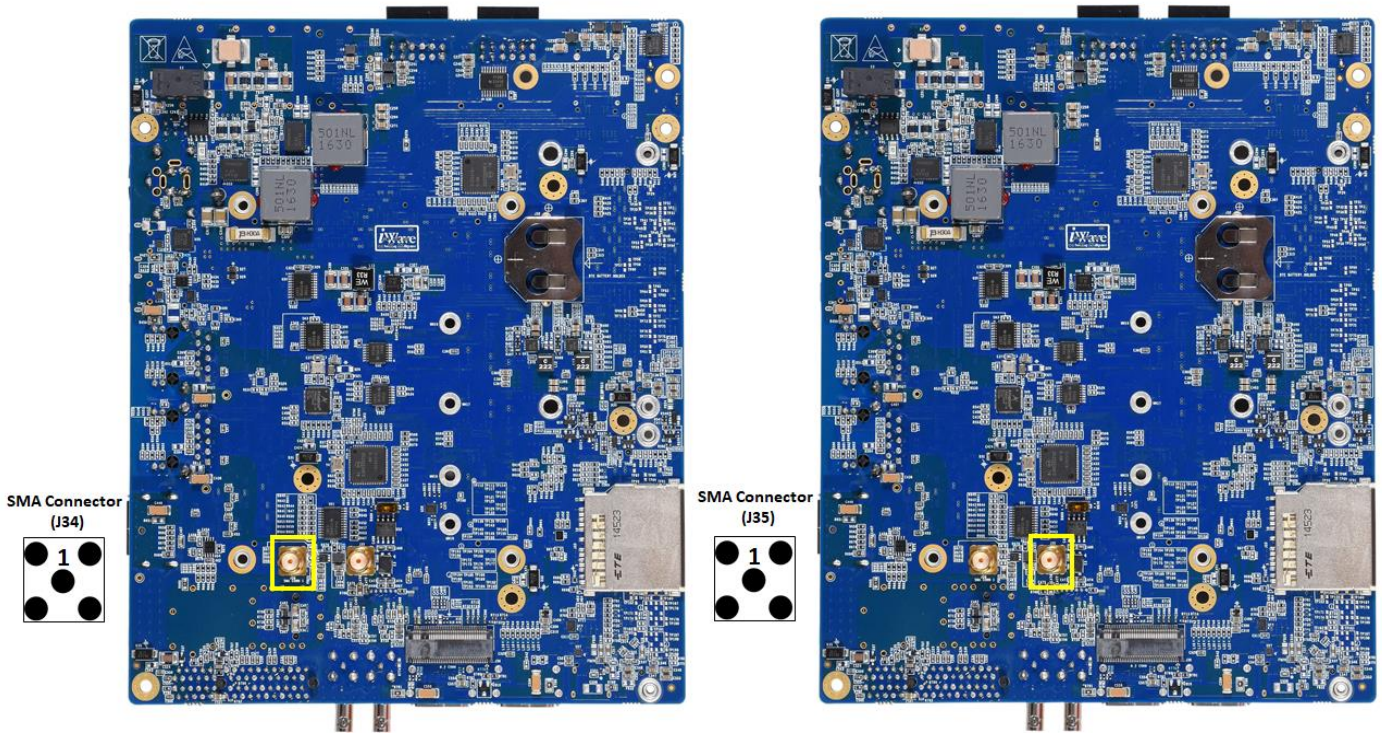

Figure 22: SMA Connectors

Table 13: SMA Connector Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
J34.1	GXBL1E_TX_CH3p	O, DIFF	Transceiver Bank226 channel3 High speed differential transmitter positive.
J35.1	GXBL1E_TX_CH3n	O, DIFF	Transceiver Bank226 channel3 High speed differential transmitter negative.

2.5.5 FMC HPC Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one 400Pin Standard FMC HPC connector to support standard ANSI/VITA 57.1 FMC modules.

The FMC HPC Connector (J22) supports the below mentioned interface from iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM .

- 10 High Speed GX/GXT Transceivers Channels
- 2 Transceiver Reference Clock inputs
- Up to 09 LVDS IOs/18 Single ended (SE) IOs from FPGA IO Banks.
- 2 Clock Input Capable LVDS/SE pins from FPGA IO Banks
- 3 Clock Output Capable LVDS/SE pins from FPGA IO Banks

This 400Pin FMC HPC connector (J22) is physically located at the top of the board as shown below.

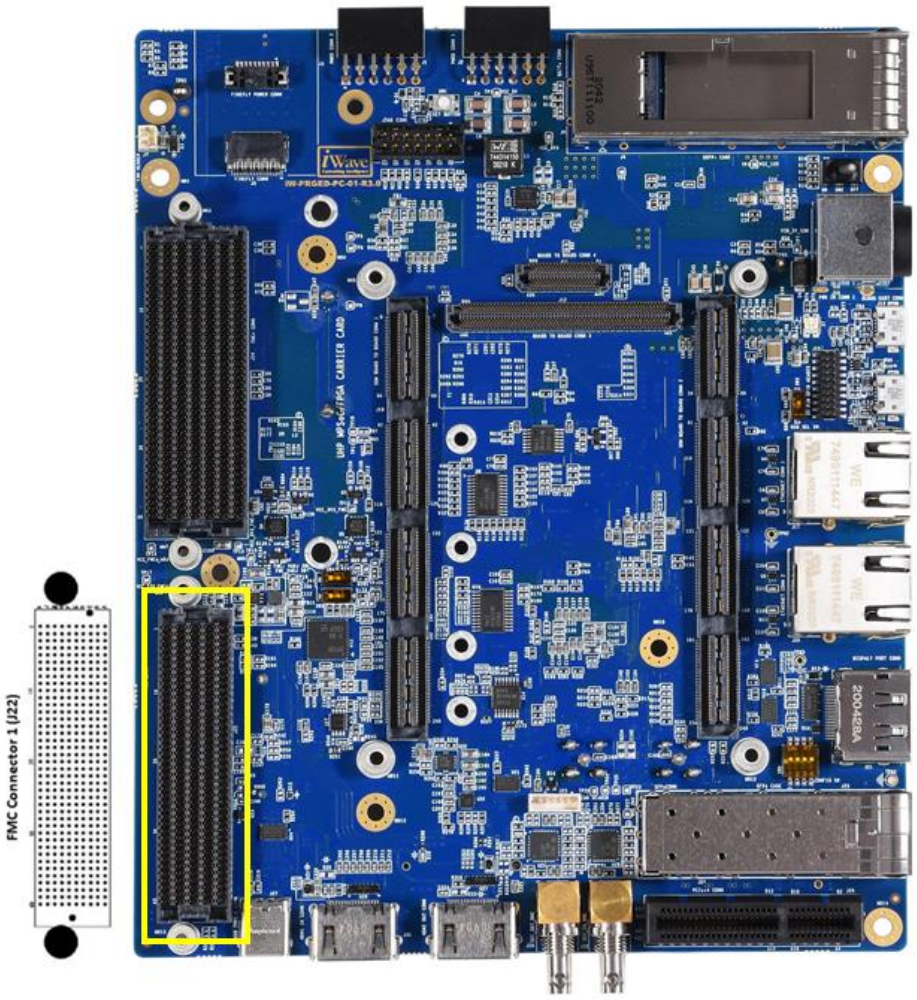

Figure 23: FMC Connector

This 400Pin FMC HPC connector (J22) pin mapping is shown below.

	K	J	H	G	F	E	D	C	B	A
1		GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND
2		NC	PRSNT_M2C_L	CLK1_M2C_P		NC	GND	DP0_C2M_P	GND	DP1_M2C_P
3		NC	GND	CLK1_M2C_N		NC	GND	DP0_C2M_N	GND	DP1_M2C_N
4		GND	NC	GND	NC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5		GND	NC	GND	NC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6		NC	GND	LA00_P_CC		NC	GND	DP0_M2C_P	GND	DP2_M2C_P
7	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N
8	NC	GND	LA02_N	GND	NC	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9		NC	GND	LA03_P		NC	LA01_N_CC	GND	DP8_M2C_N	GND
10	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND	DP3_M2C_P
11	NC	GND	LA04_N	GND	NC	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12		NC	GND	LA08_P		NC	LA05_N	GND	DP7_M2C_P	GND
13	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	DP7_M2C_N	GND
14	NC	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15		NC	GND	LA12_P		NC	LA09_N	LA10_N	GND	DP4_M2C_N
16	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND
17	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	DP6_M2C_N	GND
18		NC	GND	NC		NC	LA13_N	NC	GND	DP5_M2C_P
19	NC	NC	NC	NC	NC	NC	GND	NC	GND	DP5_M2C_N
20	NC	GND	NC	GND	NC	GND	NC	GND	GBTCLK1_M2C_P	GND
21		NC	GND	NC		NC	NC	GND	GBTCLK1_M2C_N	GND
22	NC	NC	NC	NC	NC	NC	GND	NC	GND	DP1_C2M_P
23	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP1_C2M_N
24		NC	GND	NC		NC	NC	GND	DP9_C2M_P	GND
25	NC	NC	NC	NC	NC	NC	GND	GND	DP9_C2M_N	GND
26	NC	GND	NC	GND	NC	GND	NC	NC	GND	DP2_C2M_P
27		NC	GND	NC		NC	NC	NC	GND	DP2_C2M_N
28	NC	NC	NC	NC	NC	NC	GND	GND	DP8_C2M_P	GND
29	NC	GND	NC	GND	NC	GND	TCK	GND	DP8_C2M_N	GND
30		NC	GND	NC		NC	TDI	SCL	GND	DP3_C2M_P
31	NC	NC	NC	NC	NC	NC	TDO	SDA	GND	DP3_C2M_N
32	NC	GND	NC	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND
33		NC	GND	NC		NC	TMS	GND	DP7_C2M_N	GND
34	NC	NC	NC	NC	NC	NC	TRST_L	GA0	GND	DP4_C2M_P
35	NC	GND	NC	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N
36		NC	GND	NC		NC	3P3V	GND	DP6_C2M_P	GND
37	NC	NC	NC	NC	NC	NC	GND	12P0V	DP6_C2M_N	GND
38	NC	GND	NC	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P
39		NC	GND	VADJ		VADJ	GND	3P3V	GND	DP5_C2M_N
40	NC	GND	VADJ	GND		GND	3P3V	GND	NC	GND

Figure 24: FMC HPC Connector Pin Out

Number of Pins - 400

Connector Part Number - ASP-134486-01

Mating Connector - ASP-134488-01 from Samtec

Staking Height - 10mm

Note:

** By default, FMC connector power is disabled as per Vita Specification. While booting the FMC Module EEPROM is read and enabling the FMC connector power.*

** If FMC modules EEPROM is not programmed, then FMC connector power is not enabled.*

Table 14: FMC HPC Connector Pin Assignment

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
1	A1	GND	NA	NA	GND	NA	NA	Power	Ground.
2	A2	DP1_M2C_P	Board to Board Connector 1	17	GXBL1F_RX_CH1p	1F	AD38	I, DIFF	Transceiver Bank1F channel1 High speed differential receiver positive.
3	A3	DP1_M2C_N	Board to Board Connector 1	15	GXBL1M_RX_CH1n	1M	G35	I, DIFF	Transceiver Bank1F channel1 High speed differential receiver Negative.
4	A4	GND	NA	NA	GND	NA	NA	Power	Ground.
5	A5	GND	NA	NA	GND	NA	NA	Power	Ground.
6	A6	DP2_M2C_P	Board to Board Connector 1	57	GXBL1M_RX_CH2p	1M	C36	I, DIFF	Transceiver Bank1M channel2 High speed differential receiver positive.
7	A7	DP2_M2C_N	Board to Board Connector 1	55	GXBL1M_RX_CH2n	1M	C35	I, DIFF	Transceiver Bank1M channel2 High speed differential receiver Negative.
8	A8	GND	NA	NA	GND	NA	NA	Power	Ground.
9	A9	GND	NA	NA	GND	NA	NA	Power	Ground.
10	A10	DP3_M2C_P	Board to Board Connector 1	51	GXBL1M_RX_CH3p	1M	E36	I, DIFF	Transceiver Bank1M channel3 High speed differential receiver positive.
11	A11	DP3_M2C_N	Board to Board Connector 1	49	GXBL1M_RX_CH3n	1M	E35	I, DIFF	Transceiver Bank1M channel3 High speed differential receiver Negative.
12	A12	GND	NA	NA	GND	NA	NA	Power	Ground.
13	A13	GND	NA	NA	GND	NA	NA	Power	Ground.
14	A14	DP4_M2C_P	Board to Board Connector 1	117	GXBL1K_RX_CH0p	1K	W36	I, DIFF	Transceiver Bank1K channel0 High speed differential receiver positive.
15	A15	DP4_M2C_N	Board to Board Connector 1	115	GXBL1K_RX_CH0n	1K	W35	I, DIFF	Transceiver Bank1K channel0 High speed differential receiver Negative.
16	A16	GND	NA	NA	GND	NA	NA	Power	Ground.
17	A17	GND	NA	NA	GND	NA	NA	Power	Ground.
18	A18	DP5_M2C_P	Board to Board Connector 1	111	GXBL1K_RX_CH1p	1K	Y38	I, DIFF	Transceiver Bank1K channel1 High speed differential receiver positive.
19	A19	DP5_M2C_N	Board to Board Connector 1	109	GXBL1K_RX_CH1n	1K	Y37	I, DIFF	Transceiver Bank1K channel1 High speed differential receiver Negative.
20	A20	GND	NA	NA	GND	NA	NA	Power	Ground.
21	A21	GND	NA	NA	GND	NA	NA	Power	Ground.
22	A22	DP1_C2M_P	Board to Board Connector 1	9	GXBL1M_TX_CH1p	1M	H42	O, DIFF	Transceiver Bank1M channel1 High speed differential transmitter positive.
23	A23	DP1_C2M_N	Board to Board Connector 1	11	GXBL1M_TX_CH1n	1M	H41	O, DIFF	Transceiver Bank1M channel1 High speed differential transmitter Negative.
24	A24	GND	NA	NA	GND	NA	NA	Power	Ground.
25	A25	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
26	A26	DP2_C2M_P	Board to Board Connector 1	37	GXBL1M_TX_CH2p	1M	G40	O, DIFF	Transceiver Bank1M channel2 High speed differential transmitter positive.
27	A27	DP2_C2M_N	Board to Board Connector 1	39	GXBL1M_TX_CH2n	1M	G39	O, DIFF	Transceiver Bank1M channel2 High speed differential transmitter Negative.
28	A28	GND	NA	NA	GND	NA	NA	Power	Ground.
29	A29	GND	NA	NA	GND	NA	NA	Power	Ground.
30	A30	DP3_C2M_P	Board to Board Connector 1	43	GXBL1M_TX_CH3p	1M	F42	O, DIFF	Transceiver Bank1M channel3 High speed differential transmitter positive.
31	A31	DP3_C2M_N	Board to Board Connector 1	45	GXBL1M_TX_CH3n	1M	F41	O, DIFF	Transceiver Bank1M channel3 High speed differential transmitter Negative.
32	A32	GND	NA	NA	GND	NA	NA	Power	Ground.
33	A33	GND	NA	NA	GND	NA	NA	Power	Ground.
34	A34	DP4_C2M_P	Board to Board Connector 1	97	GXBL1K_TX_CH0p	1K	AA40	O, DIFF	Transceiver Bank1K channel0 High speed differential transmitter positive.
35	A35	DP4_C2M_N	Board to Board Connector 1	99	GXBL1K_TX_CH0n	1K	AA39	O, DIFF	Transceiver Bank1K channel0 High speed differential transmitter Negative.
36	A36	GND	NA	NA	GND	NA	NA	Power	Ground.
37	A37	GND	NA	NA	GND	NA	NA	Power	Ground.
38	A38	DP5_C2M_P	Board to Board Connector 1	103	GXBL1K_TX_CH1p	1K	Y42	O, DIFF	Transceiver Bank1K channel1 High speed differential transmitter positive.
39	A39	DP5_C2M_N	Board to Board Connector 1	105	GXBL1K_TX_CH1n	1K	Y41	O, DIFF	Transceiver Bank1K channel1 High speed differential transmitter Negative.
40	A40	GND	NA	NA	GND	NA	NA	Power	Ground.
41	B1	CLK_DIR	NA	NA	NA	NA	NA	O, 3.3V	CLK-DIR. This Pin is connected to 15th pin of LVDS IO Expander (U10).
42	B2	GND	NA	NA	GND	NA	NA	Power	Ground.
43	B3	GND	NA	NA	GND	NA	NA	Power	Ground.
44	B4	DP9_M2C_P	Board to Board Connector 2	187	GXBL1C_RX_CH0p	1C	AV30	I, DIFF	Transceiver Bank1C channel0 High speed differential receiver positive.
45	B5	DP9_M2C_N	Board to Board Connector 2	189	GXBL1C_RX_CH0n	1C	AV29	I, DIFF	Transceiver Bank1C channel0 High speed differential receiver Negative.
46	B6	GND	NA	NA	GND	NA	NA	Power	Ground.
47	B7	GND	NA	NA	GND	NA	NA	Power	Ground.
48	B8	DP8_M2C_P	Board to Board Connector 2	199	GXBL1C_RX_CH1p	1C	AY30	I, DIFF	Transceiver Bank1C channel1 High speed differential receiver positive.
49	B9	DP8_M2C_N	Board to Board Connector 2	201	GXBL1C_RX_CH1n	1C	AY29	I, DIFF	Transceiver Bank1C channel1 High speed differential receiver Negative.
50	B10	GND	NA	NA	GND	NA	NA	Power	Ground.
51	B11	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
52	B12	DP7_M2C_P	Board to Board Connector 1	137	GXBL1K_RX_CH3p	1K	V38	I, DIFF	Transceiver Bank1K channel3 High speed differential receiver positive.
53	B13	DP7_M2C_N	Board to Board Connector 1	135	GXBL1K_RX_CH3n	1K	V37	I, DIFF	Transceiver Bank1K channel3 High speed differential receiver Negative.
54	B14	GND	NA	NA	GND	NA	NA	Power	Ground.
55	B15	GND	NA	NA	GND	NA	NA	Power	Ground.
56	B16	DP6_M2C_P	Board to Board Connector 1	143	GXBL1K_RX_CH2p	1K	U35	I, DIFF	Transceiver Bank1K channel2 High speed differential receiver positive.
57	B17	DP6_M2C_N	Board to Board Connector 1	141	GXBL1K_RX_CH2n	1K	U36	I, DIFF	Transceiver Bank1K channel2 High speed differential receiver Negative.
58	B18	GND	NA	NA	GND	NA	NA	Power	Ground.
59	B19	GND	NA	NA	GND	NA	NA	Power	Ground.
60	B20	GBTCLK1_M2C_P	Board to Board Connector 1	98	REFCLK_GXBL1K_CHTp	1K	Y34	I, DIFF	Transceiver Bank1K differential reference clock0 positive.
61	B21	GBTCLK1_M2C_N	Board to Board Connector 1	100	REFCLK_GXBL1K_CHTn	1K	Y33	I, DIFF	Transceiver Bank1K differential reference clock0 negative.
62	B22	GND	NA	NA	GND	NA	NA	Power	Ground.
63	B23	GND	NA	NA	GND	NA	NA	Power	Ground.
64	B24	DP9_C2M_P	Board to Board Connector 2	193	GXBL1C_TX_CH0p	1C	BB34	O, DIFF	Transceiver Bank1C channel0 High speed differential transmitter positive.
65	B25	DP9_C2M_N	Board to Board Connector 2	195	GXBL1C_TX_CH0n	1C	BB33	O, DIFF	Transceiver Bank1C channel0 High speed differential transmitter Negative.
66	B26	GND	NA	NA	GND	NA	NA	Power	Ground.
67	B27	GND	NA	NA	GND	NA	NA	Power	Ground.
68	B28	DP8_C2M_P	Board to Board Connector 2	205	GXBL1C_TX_CH1p	1C	BA36	O, DIFF	Transceiver Bank1C channel1 High speed differential transmitter positive.
69	B29	DP8_C2M_N	Board to Board Connector 2	207	GXBL1C_TX_CH1n	1C	BA35	O, DIFF	Transceiver Bank1C channel1 High speed differential transmitter Negative.
70	B30	GND	NA	NA	GND	NA	NA	Power	Ground.
71	B31	GND	NA	NA	GND	NA	NA	Power	Ground.
72	B32	DP7_C2M_P	Board to Board Connector 1	129	GXBL1K_TX_CH3p	1K	V42	O, DIFF	Transceiver Bank1K channel3 High speed differential transmitter positive.
73	B33	DP7_C2M_N	Board to Board Connector 1	131	GXBL1K_TX_CH3n	1K	V41	O, DIFF	Transceiver Bank1K channel3 High speed differential transmitter Negative.
74	B34	GND	NA	NA	GND	NA	NA	Power	Ground.
75	B35	GND	NA	NA	GND	NA	NA	Power	Ground.
76	B36	DP6_C2M_P	Board to Board Connector 1	123	GXBL1K_TX_CH2p	1K	W40	O, DIFF	Transceiver Bank1K channel2 High speed differential transmitter positive.
77	B37	DP6_C2M_N	Board to Board Connector 1	125	GXBL1K_TX_CH2n	1K	W39	O, DIFF	Transceiver Bank1K channel2 High speed differential transmitter Negative.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
78	**B38**	GND	NA	NA	GND	NA	NA	Power	Ground.
79	**B39**	GND	NA	NA	GND	NA	NA	Power	Ground.
80	**B40**	RES0	NA	NA	NA	NA	NA	NA	NC.
81	**C1**	GND	NA	NA	GND	NA	NA	Power	Ground.
82	**C2**	DP0_C2M_P	Board to Board Connector 1	3	GXBL1M_TX_CH0p	1M	J40	O, DIFF	Transceiver Bank1M channel0 High speed differential transmitter positive.
83	**C3**	DP0_C2M_N	Board to Board Connector 1	5	GXBL1M_TX_CH0n	1M	J39	O, DIFF	Transceiver Bank1M channel0 High speed differential transmitter Negative.
84	**C4**	GND	NA	NA	GND	NA	NA	Power	Ground.
85	**C5**	GND	NA	NA	GND	NA	NA	Power	Ground.
86	**C6**	DP0_M2C_P	Board to Board Connector 1	23	GXBL1M_RX_CH0p	1M	J36	I, DIFF	Transceiver Bank1M channel0 High speed differential receiver positive.
87	**C7**	DP0_M2C_N	Board to Board Connector 1	21	GXBL1M_RX_CH0n	1M	J35	I, DIFF	Transceiver Bank1M channel0 High speed differential receiver Negative.
88	**C8**	GND	NA	NA	GND	NA	NA	Power	Ground.
89	**C9**	GND	NA	NA	GND	NA	NA	Power	Ground.
90	**C10**	LA06_P	Board to Board Connector 2	122	FPGA_LVDS2B_22p_IO5	2B	BB23	IO, 1.8V LVDS	Bank2B LVDS IO22 differential positive.
91	**C11**	LA06_N	Board to Board Connector 2	124	FPGA_LVDS2B_22n_IO6	2B	BB22	IO, 1.8V LVDS	Bank2B LVDS IO22 differential negative
92	**C12**	GND	NA	NA	GND	NA	NA	Power	Ground.
93	**C13**	GND	NA	NA	GND	NA	NA	Power	Ground.
94	**C14**	LA10_P	Board to Board Connector 2	115	FPGA_LVDS2B_15p/CLKOUT_0p	2B	AL26	IO, 1.8V LVDS	Bank2B LVDS IO15 differential positive.
95	**C15**	LA10_N	Board to Board Connector 2	117	FPGA_LVDS2B_15n/CLKOUT_0n	2B	AL25	IO, 1.8V LVDS	Bank2B LVDS IO15 differential negative.
96	**C16**	GND	NA	NA	GND	NA	NA	Power	Ground.
97	**C17**	GND	NA	NA	GND	NA	NA	Power	Ground.
98	**C18**	LA14_P	NA	NA	NA	NA	NA	NA	NC.
99	**C19**	LA14_N	NA	NA	NA	NA	NA	NA	NC.
100	**C20**	GND	NA	NA	GND	NA	NA	Power	Ground.
101	**C21**	GND	NA	NA	GND	NA	NA	Power	Ground.
102	**C22**	LA18_P_CC	NA	NA	NA	NA	NA	NA	NC.
103	**C23**	LA18_N_CC	NA	NA	NA	NA	NA	NA	NC.
104	**C24**	GND	NA	NA	GND	NA	NA	Power	Ground.
105	**C25**	GND	NA	NA	GND	NA	NA	Power	Ground.
106	**C26**	LA27_P	NA	NA	NA	NA	NA	NA	NC.
107	**C27**	LA27_N	NA	NA	NA	NA	NA	NA	NC.
108	**C28**	GND	NA	NA	GND	NA	NA	Power	Ground.
109	**C29**	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
110	**C30**	SCL	NA	NA	I2C0_SD3_SCL	NA	NA	O, 3.3V LVCMOS	FMC+ I2C Clock Signal. This Pin is connected from 12th pin of I2C Bus switch (U29).
111	**C31**	SDA	NA	NA	I2C0_SD3_SDA	NA	NA	IO, 3.3V LVCMOS	FMC+ I2C Data Signal. This Pin is connected from 11th pin of I2C Bus switch (U29).
112	**C32**	GND	NA	NA	GND	NA	NA	Power	Ground.
113	**C33**	GND	NA	NA	GND	NA	NA	Power	Ground.
114	**C34**	GA0	NA	NA	NA	NA	NA	1K, PU	Geographical address 0
115	**C35**	12P0V	NA	NA	VCC_12V_FMC	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
116	**C36**	GND	NA	NA	GND	NA	NA	Power	Ground.
117	**C37**	12P0V	NA	NA	VCC_12V_FMC	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
118	**C38**	GND	NA	NA	GND	NA	NA	Power	Ground.
119	**C39**	3P3V	NA	NA	VCC_3V3_FMC	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
120	**C40**	GND	NA	NA	GND	NA	NA	Power	Ground.
121	**D1**	PG_C2M	NA	NA	NA	NA	NA	O, 3.3V	Power Good Signal from Carrier to FMC Module. This Pin is connected to 17th pin of LVDS IO Expander (U10).
122	**D2**	GND	NA	NA	GND	NA	NA	Power	Ground.
123	**D3**	GND	NA	NA	GND	NA	NA	Power	Ground.
124	**D4**	GBTCLK0_M2C_P	Board to Board Connector 1	4	REFCLK_GXBL1M_CHTp	1M	M34	I, DIFF	Transceiver Bank1M differential reference clock0 positive.
125	**D5**	GBTCLK0_M2C_N	Board to Board Connector 1	6	REFCLK_GXBL1M_CHTn	1M	M33	I, DIFF	Transceiver Bank1M differential reference clock0 Negative.
126	**D6**	GND	NA	NA	GND	NA	NA	Power	Ground.
127	**D7**	GND	NA	NA	GND	NA	NA	Power	Ground.
128	**D8**	LA01_P_CC	Board to Board Connector 1	87	FPGA_LVDS3D_1p_IO47	3D	AB9	IO, 1.8V LVDS	Bank3D LVDS IO1 differential positive.
129	**D9**	LA01_N_CC	Board to Board Connector 1	89	FPGA_LVDS3D_1n_IO48	3D	AB10	IO, 1.8V LVDS	Bank3D LVDS IO1 differential negative.
130	**D10**	GND	NA	NA	GND	NA	NA	Power	Ground.
131	**D11**	LA05_P	Board to Board Connector 2	123	FPGA_LVDS2B_21p_IO7	2B	AV23	IO, 1.8V LVDS	Bank2B LVDS IO21 differential positive.
132	**D12**	LA05_N	Board to Board Connector 2	121	FPGA_LVDS2B_21n_IO8	2B	AU23	IO, 1.8V LVDS	Bank2B LVDS IO21 differential negative
133	**D13**	GND	NA	NA	GND	NA	NA	Power	Ground.
134	**D14**	LA09_P	Board to Board Connector 2	116	FPGA_LVDS2B_13p/CLKIN_0p	2B	AR23	IO, 1.8V LVDS	Bank2B LVDS IO13 differential positive.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
135	**D15**	LA09_N	Board to Board Connector 2	118	FPGA_LVDS2B_13n/CLKIN_0n	2B	AR24	IO, 1.8V LVDS	Bank2B LVDS IO13 differential negative.
136	**D16**	GND	NA	NA	GND	NA	NA	Power	Ground.
137	**D17**	LA13_P	Board to Board Connector 2	103	FPGA_LVDS2B_19n_IO12	2B	AW23	IO, 1.8V LVDS	Bank2B LVDS IO12 differential positive.
138	**D18**	LA13_N	Board to Board Connector 2	105	FPGA_LVDS2B_19p_IO11	2B	AY23	IO, 1.8V LVDS	Bank2B LVDS IO11 differential positive.
139	**D19**	GND	NA	NA	GND	NA	NA	Power	Ground.
140	**D20**	LA17_P_CC	NA	NA	NA	NA	NA	NA	NC.
141	**D21**	LA17_N_CC	NA	NA	NA	NA	NA	NA	NC.
142	**D22**	GND	NA	NA	GND	NA	NA	Power	Ground.
143	**D23**	LA23_P	NA	NA	NA	NA	NA	NA	NC.
144	**D24**	LA23_N	NA	NA	NA	NA	NA	NA	NC.
145	**D25**	GND	NA	NA	GND	NA	NA	Power	Ground.
146	**D26**	LA26_P	NA	NA	NA	NA	NA	NA	NC.
147	**D27**	LA26_N	NA	NA	NA	NA	NA	NA	NC.
148	**D28**	GND	NA	NA	GND	NA	NA	Power	Ground.
149	**D29**	TCK	Board to Board Connector 2	31	SDM_TCK_B2B	SDM	AY11	I, 3.3V CMOS/ 49.9K PU	JTAG Test Clock This Pin is connected to 31st pin of Board-to-Board Connector2 (J19).
150	**D30**	TDI	NA	NA	NA	NA	NA	O, 3.3V CMOS	FMC+ Test Data Output. This pin is connected from D31st pin of FMC+ Connector(J14)
151	**D31**	TDO	NA	NA	FMC2_JTAG_TDO	SDM	NA	O, 3.3V CMOS	NC
152	**D32**	3P3VAUX	NA	NA	VCC_3V3	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
153	**D33**	TMS	Board to Board Connector 2	29	SDM_TMS_B2B	SDM	AY12	I, 3.3V CMOS/ 49.9K PU	JTAG Test Mode Select This Pin is connected to 29th pin of Board-to-Board Connector2 (J19).
154	**D34**	TRST_L	Board to Board Connector 2	25	NC	NC	NC	NA	NC. This Pin is connected to 25th pin of Board-to-Board Connector2 (J19).
155	**D35**	GA1	NA	NA	NA	NA	NA	1K, PD	Geographical address 1
156	**D36**	3P3V	NA	NA	VCC_3V3_FMC	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
157	**D37**	GND	NA	NA	GND	NA	NA	Power	Ground.
158	**D38**	3P3V	NA	NA	VCC_3V3_FMC	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
159	**D39**	GND	NA	NA	GND	NA	NA	Power	Ground.
160	**D40**	3P3V	NA	NA	VCC_3V3_FMC	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
161	**E1**	GND	NA	NA	GND	NA	NA	Power	Ground.
162	**E2**	HA01_P_CC	NA	NA	NA	NA	NA	NA	NC.
163	**E3**	HA01_N_CC	NA	NA	NA	NA	NA	NA	NC.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
164	E4	GND	NA	NA	GND	NA	NA	Power	Ground.
165	E5	GND	NA	NA	GND	NA	NA	Power	Ground.
166	E6	HA05_P	NA	NA	NA	NA	NA	NA	NC.
167	E7	HA05_N	NA	NA	NA	NA	NA	NA	NC.
168	E8	GND	NA	NA	GND	NA	NA	Power	Ground.
169	E9	HA09_P	NA	NA	NA	NA	NA	NA	NC.
170	E10	HA09_N	NA	NA	NA	NA	NA	NA	NC.
171	E11	GND	NA	NA	GND	NA	NA	Power	Ground.
172	E12	HA13_P	NA	NA	NA	NA	NA	NA	NC.
173	E13	HA13_N	NA	NA	NA	NA	NA	NA	NC.
174	E14	GND	NA	NA	GND	NA	NA	Power	Ground.
175	E15	HA16_P	NA	NA	NA	NA	NA	NA	NC.
176	E16	HA16_N	NA	NA	NA	NA	NA	NA	NC.
177	E17	GND	NA	NA	GND	NA	NA	Power	Ground.
178	E18	HA20_P	NA	NA	NA	NA	NA	NA	NC.
179	E19	HA20_N	NA	NA	NA	NA	NA	NA	NC.
180	E20	GND	NA	NA	GND	NA	NA	Power	Ground.
181	E21	HB03_P	NA	NA	NA	NA	NA	NA	NC.
182	E22	HB03_N	NA	NA	NA	NA	NA	NA	NC.
183	E23	GND	NA	NA	GND	NA	NA	Power	Ground.
184	E24	HB05_P	NA	NA	NA	NA	NA	NA	NC.
185	E25	HB05_N	NA	NA	NA	NA	NA	NA	NC.
186	E26	GND	NA	NA	GND	NA	NA	Power	Ground.
187	E27	HB09_P	NA	NA	NA	NA	NA	NA	NC.
188	E28	HB09_N	NA	NA	NA	NA	NA	NA	NC.
189	E29	GND	NA	NA	GND	NA	NA	Power	Ground.
190	E30	HB13_P	NA	NA	NA	NA	NA	NA	NC.
191	E31	HB13_N	NA	NA	NA	NA	NA	NA	NC.
192	E32	GND	NA	NA	GND	NA	NA	Power	Ground.
193	E33	HB19_P	NA	NA	NA	NA	NA	NA	NC.
194	E34	HB19_N	NA	NA	NA	NA	NA	NA	NC.
195	E35	GND	NA	NA	GND	NA	NA	Power	Ground.
196	E36	HB21_P	NA	NA	NA	NA	NA	NA	NC.
197	E37	HB21_N	NA	NA	NA	NA	NA	NA	NC.
198	E38	GND	NA	NA	GND	NA	NA	Power	Ground.
199	E39	VADJ	NA	NA	VCC_FMC_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
200	E40	GND	NA	NA	GND	NA	NA	Power	Ground.
201	F1	PG_M2C	NA	NA	NA	NA	NA	I, 3.3V CMOS/ 10K PU	Power Good Signal from FMC Module to Carrier.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
202	F2	GND	NA	NA	GND	NA	NA	Power	Ground.
203	F3	GND	NA	NA	GND	NA	NA	Power	Ground.
204	F4	HA00_P_CC	NA	NA	NA	NA	NA	NA	NC.
205	F5	HA00_N_CC	NA	NA	NA	NA	NA	NA	NC.
206	F6	GND	NA	NA	GND	NA	NA	Power	Ground.
207	F7	HA04_P	NA	NA	NA	NA	NA	NA	NC.
208	F8	HA04_N	NA	NA	NA	NA	NA	NA	NC.
209	F9	GND	NA	NA	GND	NA	NA	Power	Ground.
210	F10	HA08_P	NA	NA	NA	NA	NA	NA	NC.
211	F11	HA08_N	NA	NA	NA	NA	NA	NA	NC.
212	F12	GND	NA	NA	GND	NA	NA	Power	Ground.
213	F13	HA12_P	NA	NA	NA	NA	NA	NA	NC.
214	F14	HA12_N	NA	NA	NA	NA	NA	NA	NC.
215	F15	GND	NA	NA	GND	NA	NA	Power	Ground.
216	F16	HA15_P	NA	NA	NA	NA	NA	NA	NC.
217	F17	HA15_N	NA	NA	NA	NA	NA	NA	NC.
218	F18	GND	NA	NA	GND	NA	NA	Power	Ground.
219	F19	HA19_P	NA	NA	NA	NA	NA	NA	NC.
220	F20	HA19_N	NA	NA	NA	NA	NA	NA	NC.
221	F21	GND	NA	NA	GND	NA	NA	Power	Ground.
222	F22	HB02_P	NA	NA	NA	NA	NA	NA	NC.
223	F23	HB02_N	NA	NA	NA	NA	NA	NA	NC.
224	F24	GND	NA	NA	GND	NA	NA	Power	Ground.
225	F25	HB04_P	NA	NA	NA	NA	NA	NA	NC.
226	F26	HB04_N	NA	NA	NA	NA	NA	NA	NC.
227	F27	GND	NA	NA	GND	NA	NA	Power	Ground.
228	F28	HB08_P	NA	NA	NA	NA	NA	NA	NC.
229	F29	HB08_N	NA	NA	NA	NA	NA	NA	NC.
230	F30	GND	NA	NA	GND	NA	NA	Power	Ground.
231	F31	HB12_P	NA	NA	NA	NA	NA	NA	NC.
232	F32	HB12_N	NA	NA	NA	NA	NA	NA	NC.
233	F33	GND	NA	NA	GND	NA	NA	Power	Ground.
234	F34	HB16_P	NA	NA	NA	NA	NA	NA	NC.
235	F35	HB16_N	NA	NA	NA	NA	NA	NA	NC.
236	F36	GND	NA	NA	GND	NA	NA	Power	Ground.
237	F37	HB20_P	NA	NA	NA	NA	NA	NA	NC.
238	F38	HB20_N	NA	NA	NA	NA	NA	NA	NC.
239	F39	GND	NA	NA	GND	NA	NA	Power	Ground.
240	F40	VADJ	NA	NA	VCC_FMC_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
241	**G1**	GND	NA	NA	GND	NA	NA	Power	Ground.
242	**G2**	CLK1_M2C_P	Board to Board connector 1	144	FPGA_LVDS3I_10n/CLKOUT_1n	3I	W3	I, 1.8V LVDS	FPGA Bank3I LVDS IO10 differential positive.
243	**G3**	CLK1_M2C_N	Board to Board connector 1	142	FPGA_LVDS3I_10p/CLKOUT_1p	3I	W4	I, 1.8V LVDS	FPGA Bank3I LVDS IO10 differential negative.
244	**G4**	GND	NA	NA	GND	NA	NA	Power	Ground.
245	**G5**	GND	NA	NA	GND	NA	NA	Power	Ground.
246	**G6**	LA00_P_CC	Board to Board connector 1	118	FPGA_LVDS3D_10p/CLKOUT_1p	3D	AC7	I, 1.8V LVDS	FPGA Bank3D LVDS IO10 differential positive.
247	**G7**	LA00_N_CC	Board to Board connector 1	116	FPGA_LVDS3D_10n/CLKOUT_1n	3D	AC8	I, 1.8V LVDS	FPGA Bank3D LVDS IO10 differential negative.
248	**G8**	GND	NA	NA	GND	NA	NA	Power	Ground.
249	**G9**	LA03_P	Board to Board connector 2	126	FPGA_LVDS2B_24p_IO1	67	AL15	IO, 1.8V LVDS	FPGA Bank2B LVDS IO24 differential positive.
250	**G10**	LA03_N	Board to Board connector 2	128	FPGA_LVDS2B_24n_IO2	67	AM15	IO, 1.8V LVDS	FPGA Bank2B LVDS IO24 differential negative.
251	**G11**	GND	NA	NA	GND	NA	NA	Power	Ground.
252	**G12**	LA08_P	Board to Board connector 2	127	FPGA_LVDS2B_23p_IO3	2B	AT22	IO, 1.8V LVDS	FPGA Bank2B LVDS IO23 differential positive.
253	**G13**	LA08_N	Board to Board connector 2	125	FPGA_LVDS2B_23n_IO4	2B	AR22	IO, 1.8V LVDS	FPGA Bank2B LVDS IO23 differential negative.
254	**G14**	GND	NA	NA	GND	NA	NA	Power	Ground.
255	**G15**	LA12_P	Board to Board connector 2	109	FPGA_LVDS2B_12p/CLKIN_1p	2B	AY19	IO, 1.8V LVDS	FPGA Bank2B LVDS IO12 differential positive.
256	**G16**	LA12_N	Board to Board connector 2	111	FPGA_LVDS2B_12n/CLKIN_1n	2B	AW19	IO, 1.8V LVDS	FPGA Bank2B LVDS IO12 differential negative.
257	**G17**	GND	NA	NA	GND	NA	NA	Power	Ground.
258	**G18**	LA16_P	NA	NA	NA	NA	NA	NA	LVDS IO expander U51
259	**G19**	LA16_N	Board to Board connector 2	112	FPGA_LVDS2B_10n/CLKOUT_1n	2B	BA19	IO, 1.8V LVDS	FPGA Bank2B LVDS IO10 differential negative.
260	**G20**	GND	NA	NA	GND	NA	NA	Power	Ground.
261	**G21**	LA20_P	NA	NA	NA	NA	NA	NA	NC.
262	**G22**	LA20_N	NA	NA	NA	NA	NA	NA	NC.
263	**G23**	GND	NA	NA	GND	NA	NA	Power	Ground.
264	**G24**	LA22_P	NA	NA	NA	NA	NA	NA	NC.
265	**G25**	LA22_N	NA	NA	NA	NA	NA	NA	NC.
266	**G26**	GND	NA	NA	GND	NA	NA	Power	Ground.
267	**G27**	LA25_P	NA	NA	NA	NA	NA	NA	NC.
268	**G28**	LA25_N	NA	NA	NA	NA	NA	NA	NC.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
269	**G29**	GND	NA	NA	GND	NA	NA	Power	Ground.
270	**G30**	LA29_P	NA	NA	NA	NA	NA	NA	NC.
271	**G31**	LA29_N	NA	NA	NA	NA	NA	NA	NC.
272	**G32**	GND	NA	NA	GND	NA	NA	Power	Ground.
273	**G33**	LA31_P	NA	NA	NA	NA	NA	NA	NC.
274	**G34**	LA31_N	NA	NA	NA	NA	NA	NA	NC.
275	**G35**	GND	NA	NA	GND	NA	NA	Power	Ground.
276	**G36**	LA33_P	NA	NA	NA	NA	NA	NA	NC.
277	**G37**	LA33_N	NA	NA	NA	NA	NA	NA	NC.
278	**G38**	GND	NA	NA	GND	NA	NA	Power	Ground.
279	**G39**	VADJ	NA	NA	VCC_FMC_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
280	**G40**	GND	NA	NA	GND	NA	NA	Power	Ground.
281	**H1**	VREF_A_M2C	NA	NA	NA	NA	NA	NA	NC.
282	**H2**	PRSNT_M2C_L	NA	NA	NA	NA	NA	I,3.3V CMOS/ 10K PU	Module Preset Signal. This Pin is connected to 4th pin of LVDS IO Expander (U10).
283	**H3**	GND	NA	NA	GND	NA	NA	Power	Ground.
284	**H4**	CLK0_M2C_P	NA	NA	NA	NA	NA	NA	NC.
285	**H5**	CLK0_M2C_N	NA	NA	NA	NA	NA	NA	NC.
286	**H6**	GND	NA	NA	GND	NA	NA	Power	Ground.
287	**H7**	LA02_P	Board to Board connector 1	46	FPGA_LVDS3D_8p_IO33	3D	AC6	IO, 1.8V LVDS	FPGA Bank3D LVDS IO12 differential positive.
288	**H8**	LA02_N	Board to Board connector 1	48	FPGA_LVDS3D_8n_IO34	3D	AB5	IO, 1.8V LVDS	FPGA Bank3D LVDS IO12 differential negative.
289	**H9**	GND	NA	NA	GND	NA	NA	Power	Ground.
290	**H10**	LA04_P	Board to Board connector 1	24	FPGA_LVDS3D_15p/CLKOUT_0p	3D	AD1	I, 1.8V LVDS	FPGA Bank3D LVDS IO15 differential positive.
291	**H11**	LA04_N	Board to Board connector 1	22	FPGA_LVDS3D_15n/CLKOUT_0n	3D	AC1	I, 1.8V LVDS	FPGA Bank3D LVDS IO15 differential negative.
292	**H12**	GND	NA	NA	GND	NA	NA	Power	Ground.
293	**H13**	LA07_P	Board to Board connector 1	50	FPGA_LVDS3D_7p_IO35	3D	AC3	IO, 1.8V LVDS	FPGA Bank3D LVDS IO9 differential positive.
294	**H14**	LA07_N	Board to Board connector 1	52	FPGA_LVDS3D_7n_IO36	3D	AC2	IO, 1.8V LVDS	FPGA Bank3D LVDS IO9 differential negative.
295	**H15**	GND	NA	NA	GND	NA	NA	Power	Ground.
296	**H16**	LA11_P	Board to Board connector 2	95	FPGA_LVDS2B_11p_IO27	2B	BA21	IO, 1.8V LVDS	FPGA Bank2B LVDS IO5 differential positive.
297	**H17**	LA11_N	Board to Board connector 2	97	FPGA_LVDS2B_11n_IO28	2B	AY21	IO, 1.8V LVDS	FPGA Bank2B LVDS IO5 differential negative.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
298	H18	GND	NA	NA	GND	NA	NA	Power	Ground.
299	H19	LA15_P	NA	NA	NA	NA	NA	NA	NC.
300	H20	LA15_N	NA	NA	NA	NA	NA	NA	NC.
301	H21	GND	NA	NA	GND	NA	NA	Power	Ground.
302	H22	LA19_P	NA	NA	NA	NA	NA	NA	NC.
303	H23	LA19_N	NA	NA	NA	NA	NA	NA	NC.
304	H24	GND	NA	NA	GND	NA	NA	Power	Ground.
305	H25	LA21_P	NA	NA	NA	NA	NA	NA	NC.
306	H26	LA21_N	NA	NA	NA	NA	NA	NA	NC.
307	H27	GND	NA	NA	GND	NA	NA	Power	Ground.
308	H28	LA24_P	NA	NA	NA	NA	NA	NA	NC.
309	H29	LA24_N	NA	NA	NA	NA	NA	NA	NC.
310	H30	GND	NA	NA	GND	NA	NA	Power	Ground.
311	H31	LA28_P	NA	NA	NA	NA	NA	NA	NC.
312	H32	LA28_N	NA	NA	NA	NA	NA	NA	NC.
313	H33	GND	NA	NA	GND	NA	NA	Power	Ground.
314	H34	LA30_P	NA	NA	NA	NA	NA	NA	NC.
315	H35	LA30_N	NA	NA	NA	NA	NA	NA	NC.
316	H36	GND	NA	NA	GND	NA	NA	Power	Ground.
317	H37	LA32_P	NA	NA	NA	NA	NA	NA	NC.
318	H38	LA32_N	NA	NA	NA	NA	NA	NA	NC.
319	H39	GND	NA	NA	GND	NA	NA	Power	Ground.
320	H40	VADJ	NA	NA	VCC_FMC_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
321	J1	GND	NA	NA	GND	NA	NA	Power	Ground.
322	J2	CLK3_BIDIR_P	NA	NA	NA	NA	NA	NA	NC.
323	J3	CLK3_BIDIR_N	NA	NA	NA	NA	NA	NA	NC.
324	J4	GND	NA	NA	GND	NA	NA	Power	Ground.
325	J5	GND	NA	NA	GND	NA	NA	Power	Ground.
326	J6	HA03_P	NA	NA	NA	NA	NA	NA	NC.
327	J7	HA03_N	NA	NA	NA	NA	NA	NA	NC.
328	J8	GND	NA	NA	GND	NA	NA	Power	Ground.
329	J9	HA07_P	NA	NA	NA	NA	NA	NA	NC.
330	J10	HA07_N	NA	NA	NA	NA	NA	NA	NC.
331	J11	GND	NA	NA	GND	NA	NA	Power	Ground.
332	J12	HA11_P	NA	NA	NA	NA	NA	NA	NC.
333	J13	HA11_N	NA	NA	NA	NA	NA	NA	NC.
334	J14	GND	NA	NA	GND	NA	NA	Power	Ground.
335	J15	HA14_P	NA	NA	NA	NA	NA	NA	NC.
336	J16	HA14_N	NA	NA	NA	NA	NA	NA	NC.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
337	J17	GND	NA	NA	GND	NA	NA	Power	Ground.
338	J18	HA18_P	NA	NA	NA	NA	NA	NA	NC.
339	J19	HA18_N	NA	NA	NA	NA	NA	NA	NC.
340	J20	GND	NA	NA	GND	NA	NA	Power	Ground.
341	J21	HA22_P	NA	NA	NA	NA	NA	NA	NC.
342	J22	HA22_N	NA	NA	NA	NA	NA	NA	NC.
343	J23	GND	NA	NA	GND	NA	NA	Power	Ground.
344	J24	HB01_P	NA	NA	NA	NA	NA	NA	NC.
345	J25	HB01_N	NA	NA	NA	NA	NA	NA	NC.
346	J26	GND	NA	NA	GND	NA	NA	Power	Ground.
347	J27	HB07_P	NA	NA	NA	NA	NA	NA	NC.
348	J28	HB07_N	NA	NA	NA	NA	NA	NA	NC.
349	J29	GND	NA	NA	GND	NA	NA	Power	Ground.
350	J30	HB11_P	NA	NA	NA	NA	NA	NA	NC.
351	J31	HB11_N	NA	NA	NA	NA	NA	NA	NC.
352	J32	GND	NA	NA	GND	NA	NA	Power	Ground.
353	J33	HB15_P	NA	NA	NA	NA	NA	NA	NC.
354	J34	HB15_N	NA	NA	NA	NA	NA	NA	NC.
355	J35	GND	NA	NA	GND	NA	NA	Power	Ground.
356	J36	HB18_P	NA	NA	NA	NA	NA	NA	NC.
357	J37	HB18_N	NA	NA	NA	NA	NA	NA	NC.
358	J38	GND	NA	NA	GND	NA	NA	Power	Ground.
359	J39	VIO_B_M2C	NA	NA	NA	NA	NA	NA	NC.
360	J40	GND	NA	NA	GND	NA	NA	Power	Ground.
361	K1	VREF_B_M2C	NA	NA	NA	NA	NA	NA	NC.
362	K2	GND	NA	NA	GND	NA	NA	Power	Ground.
363	K3	GND	NA	NA	GND	NA	NA	Power	Ground.
364	K4	CLK2_BIDIR_P	NA	NA	NA	NA	NA	NA	NC.
365	K5	CLK2_BIDIR_N	NA	NA	NA	NA	NA	NA	NC.
366	K6	GND	NA	NA	GND	NA	NA	Power	Ground.
367	K7	HA02_P	NA	NA	NA	NA	NA	NA	NC.
368	K8	HA02_N	NA	NA	NA	NA	NA	NA	NC.
369	K9	GND	NA	NA	GND	NA	NA	Power	Ground.
370	K10	HA06_P	NA	NA	NA	NA	NA	NA	NC.
371	K11	HA06_N	NA	NA	NA	NA	NA	NA	NC.
372	K12	GND	NA	NA	GND	NA	NA	Power	Ground.
373	K13	HA10_P	NA	NA	NA	NA	NA	NA	NC.
374	K14	HA10_N	NA	NA	NA	NA	NA	NA	NC.
375	K15	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC Connector VITA		Board to Board Connectors			Stratic10 GX/SX SoC FPGA SOM			Description
	FMC Connector Pin No	FMC Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	Transceiver Bank	CPU Pin No	Signal Type/ Termination	
376	**K16**	HA17_P_CC	NA	NA	NA	NA	NA	NA	NC.
377	**K17**	HA17_N_CC	NA	NA	NA	NA	NA	NA	NC.
378	**K18**	GND	NA	NA	GND	NA	NA	Power	Ground.
379	**K19**	HA21_P	NA	NA	NA	NA	NA	NA	NC.
380	**K20**	HA21_N	NA	NA	NA	NA	NA	NA	NC.
381	**K21**	GND	NA	NA	GND	NA	NA	Power	Ground.
382	**K22**	HA23_P	NA	NA	NA	NA	NA	NA	NC.
383	**K23**	HA23_N	NA	NA	NA	NA	NA	NA	NC.
384	**K24**	GND	NA	NA	GND	NA	NA	Power	Ground.
385	**K25**	HB00_P_CC	NA	NA	NA	NA	NA	NA	NC.
386	**K26**	HB00_N_CC	NA	NA	NA	NA	NA	NA	NC.
387	**K27**	GND	NA	NA	GND	NA	NA	Power	Ground.
388	**K28**	HB06_P_CC	NA	NA	NA	NA	NA	NA	NC.
389	**K29**	HB06_N_CC	NA	NA	NA	NA	NA	NA	NC.
390	**K30**	GND	NA	NA	GND	NA	NA	Power	Ground.
391	**K31**	HB10_P	NA	NA	NA	NA	NA	NA	NC.
392	**K32**	HB10_N	NA	NA	NA	NA	NA	NA	NC.
393	**K33**	GND	NA	NA	GND	NA	NA	Power	Ground.
394	**K34**	HB14_P	NA	NA	NA	NA	NA	NA	NC.
395	**K35**	HB14_N	NA	NA	NA	NA	NA	NA	NC.
396	**K36**	GND	NA	NA	GND	NA	NA	Power	Ground.
397	**K37**	HB17_P_CC	NA	NA	NA	NA	NA	NA	NC.
398	**K38**	HB17_N_CC	NA	NA	NA	NA	NA	NA	NC.
399	**K39**	GND	NA	NA	GND	NA	NA	Power	Ground.
400	**K40**	VIO_B_M2C	NA	NA	NA	NA	NA	NA	NC.

Note:

**FMC connector supports VADJ 1.8V and 1.2V. By default, VADJ is set to 1.8V. Contact iWave for further details.*

** If VCC_FMC_ADJ voltage changed from default value 1.8 to 1.2V, please make sure that SOM concern IO voltage also to be modified to avoid IO conflict.*

2.5.6 FMC+ HPC Connector

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one 560Pin FMC+ HPC connector to support standard ANSI/VITA 57.4 FMC modules.

The FMC+ HPC Connector (J14) supports the below mentioned interface from iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM module.

- Up to 12 High Speed GXT Transceivers Channels
- Up to 16 High Speed GXT Transceivers Channels (Inclusive of the GXT Channels)
- 2 Transceiver Reference Clock Inputs
- Up to 28 LVDS IOs/56 Single ended (SE) IOs from FPGA IO Banks
- 5 Clock Input Capable LVDS/SE pins from FPGA IO Banks
- 2 Clock Output Capable LVDS/SE pins from FPGA IO Banks

This 560Pin FMC+ HPC connector (J14) is physically located at the top of the board as shown below.

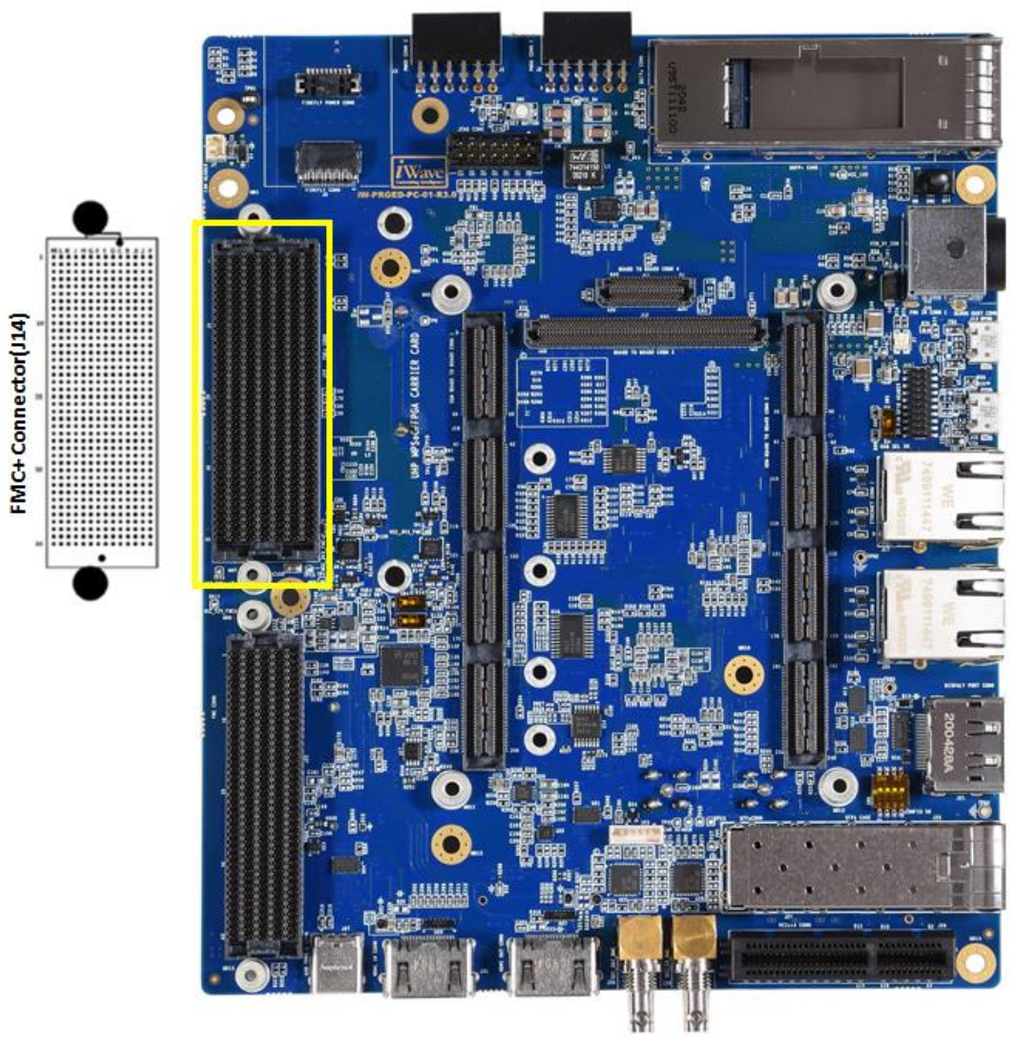

Figure 25: FMC+ Connector

This 560Pin FMC HPC connector (J14) pin mapping is shown below.

	M	L	K	J	H	G	F	E	D	C	B	A	Z	Y
1	GND	NC	NC	GND	NC	GND	PG_M2C	GND	PG_C2M	GND	CLK_DIR	GND	HSPC_PRSNT_M2C_L	GND
2	DP23_M2C_P	GND	GND	CLK3_BIDIR_P	PRSNT_M2C_L	CLK1_M2C_P	GND	NC	GND	DP0_C2M_P	GND	DP1_M2C_P	GND	DP23_C2M_P
3	DP23_M2C_N	GND	GND	CLK3_BIDIR_N	GND	CLK1_M2C_N	GND	NC	GND	DP0_C2M_N	GND	DP1_M2C_N	GND	DP23_C2M_N
4	GND	GBTCLK4_M2C_P	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND	DP22_C2M_P	GND
5	GND	GBTCLK4_M2C_N	NC	GND	NC	GND	NC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND	DP22_C2M_N	GND
6	DP22_M2C_P	GND	GND	NC	GND	LA00_P_CC	GND	NC	GND	DP0_M2C_P	GND	DP2_M2C_P	GND	DP21_C2M_P
7	DP22_M2C_N	GND	NC	NC	LA02_P	LA00_N_CC	NC	NC	GND	DP0_M2C_N	GND	DP2_M2C_N	GND	DP21_C2M_N
8	GND	GBTCLK3_M2C_P	NC	GND	LA02_N	GND	NC	GND	LA01_P_CC	GND	DP8_M2C_P	GND	DP20_C2M_P	GND
9	GND	GBTCLK3_M2C_N	GND	NC	GND	LA03_P	GND	NC	LA01_N_CC	GND	DP8_M2C_N	GND	DP20_C2M_N	GND
10	DP21_M2C_P	GND	NC	NC	LA04_P	LA03_N	NC	NC	GND	LA06_P	GND	DP3_M2C_P	GND	DP10_M2C_P
11	DP21_M2C_N	GND	NC	GND	LA04_N	GND	NC	GND	LA05_P	LA06_N	GND	DP3_M2C_N	GND	DP10_M2C_N
12	GND	GBTCLK2_M2C_P	GND	NC	GND	LA08_P	GND	NC	LA05_N	GND	DP7_M2C_P	GND	DP11_M2C_P	GND
13	GND	GBTCLK2_M2C_N	NC	NC	LA07_P	LA08_N	NC	NC	GND	GND	DP7_M2C_N	GND	DP11_M2C_N	GND
14	DP20_M2C_P	GND	NC	GND	LA07_N	GND	NC	GND	LA09_P	LA10_P	GND	DP4_M2C_P	GND	DP12_M2C_P
15	DP20_M2C_N	GND	GND	NC	GND	LA12_P	GND	NC	LA09_N	LA10_N	GND	DP4_M2C_N	GND	DP12_M2C_N
16	GND	NC	NC	NC	LA11_P	LA12_N	NC	NC	GND	GND	DP6_M2C_P	GND	DP13_M2C_P	GND
17	GND	NC	NC	GND	LA11_N	GND	NC	GND	LA13_P	GND	DP6_M2C_N	GND	DP13_M2C_N	GND
18	DP14_C2M_P	GND	GND	NC	GND	LA16_P	GND	NC	LA13_N	LA14_P	GND	DP5_M2C_P	GND	DP14_M2C_P
19	DP14_C2M_N	GND	NC	NC	LA15_P	LA16_N	NC	NC	GND	LA14_N	GND	DP5_M2C_N	GND	DP14_M2C_N
20	GND	NC	NC	GND	LA15_N	GND	NC	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND	GBTCLK5_M2C_P	GND
21	GND	NC	GND	NC	GND	LA20_P	GND	NC	LA17_N_CC	GND	GBTCLK1_M2C_N	GND	GBTCLK5_M2C_N	GND
22	DP15_C2M_P	GND	NC	NC	LA19_P	LA20_N	NC	NC	GND	LA18_P_CC	GND	DP1_C2M_P	GND	DP15_M2C_P
23	DP15_C2M_N	GND	NC	GND	LA19_N	GND	NC	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N	GND	DP15_M2C_N
24	GND	NC	GND	NC	GND	LA22_P	GND	NC	LA23_N	GND	DP9_C2M_P	GND	DP10_C2M_P	GND
25	GND	NC	NC	NC	LA21_P	LA22_N	NC	NC	GND	GND	DP9_C2M_N	GND	DP10_C2M_N	GND
26	DP16_C2M_P	GND	NC	GND	LA21_N	GND	NC	GND	LA26_P	LA27_P	GND	DP2_C2M_P	GND	DP11_C2M_P
27	DP16_C2M_N	GND	GND	NC	GND	LA25_P	GND	NC	LA26_N	LA27_N	GND	DP2_C2M_N	GND	DP11_C2M_N
28	GND	NC	NC	NC	LA24_P	LA25_N	NC	NC	GND	GND	DP8_C2M_P	GND	DP12_C2M_P	GND
29	GND	NC	NC	GND	LA24_N	GND	NC	GND	TCK	GND	DP8_C2M_N	GND	DP12_C2M_N	GND
30	DP17_C2M_P	GND	GND	NC	GND	LA29_P	GND	NC	TDI	SCL	GND	DP3_C2M_P	GND	DP13_C2M_P
31	DP17_C2M_N	GND	NC	NC	LA28_P	LA29_N	NC	NC	TDO	SDA	GND	DP3_C2M_N	GND	DP13_C2M_N
32	GND	NC	NC	GND	LA28_N	GND	NC	GND	3P3VAUX	GND	DP7_C2M_P	GND	DP16_M2C_P	GND
33	GND	NC	GND	NC	GND	LA31_P	GND	NC	TMS	GND	DP7_C2M_N	GND	DP16_M2C_N	GND
34	DP18_C2M_P	GND	NC	NC	LA30_P	LA31_N	NC	NC	TRST_L	GA0	GND	DP4_C2M_P	GND	DP17_M2C_P
35	DP18_C2M_N	GND	NC	GND	LA30_N	GND	NC	GND	GA1	12P0V	GND	DP4_C2M_N	GND	DP17_M2C_N
36	GND	12P0V	GND	NC	GND	LA33_P	GND	NC	3P3V	GND	DP6_C2M_P	GND	DP18_M2C_P	GND
37	GND	12P0V	NC	NC	LA32_P	LA33_N	NC	NC	GND	12P0V	DP6_C2M_N	GND	DP18_M2C_N	GND
38	DP19_C2M_P	GND	NC	GND	LA32_N	GND	NC	GND	3P3V	GND	GND	DP5_C2M_P	GND	DP19_M2C_P
39	DP19_C2M_N	GND	GND	NC	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N	GND	DP19_M2C_N
40	GND	12P0V	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND	3P3V	GND

Figure 26: FMC+ HPC Connector Pin Out

Number of Pins - 560

Connector Part Number - ASP-184329-01 from Samtec

Mating Connector - ASP-184330-01 from Samtec

Staking Height - 10mm

Note:

** By default, FMC+ connector power is disabled as per Vita Specification. While booting the FMC or FMC+ Modules EEPROM is read and enabling the FMC+ connector power.*

** If FMC & FMC+ modules EEPROM is not programmed, then FMC+ connector power is not enabled.*

Table 15: FMC+ HPC Connector Pin Assignment

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
1	A1	GND	NA	NA	GND	NA	NA	Power	Ground.
2	A2	DP1_M2C_P	Board to Board Connector 3	A36	GXBL1F_RX_CH1p	1F	AD38	I, DIFF	Transceiver Bank1F channel1 High speed differential receiver positive.
3	A3	DP1_M2C_N	Board to Board Connector 3	A37	GXBL1F_RX_CH1n	1G	AD37	I, DIFF	Transceiver Bank1F channel1 High speed differential receiver negative.
4	A4	GND	NA	NA	GND	NA	NA	Power	Ground.
5	A5	GND	NA	NA	GND	NA	NA	Power	Ground.
6	A6	DP2_M2C_P	Board to Board Connector 3	A25	GXBL1F_RX_CH3p	1F	AB38	I, DIFF	Transceiver Bank1F channel3 High speed differential receiver positive.
7	A7	DP2_M2C_N	Board to Board Connector 3	A24	GXBL1F_RX_CH3n	1F	AB37	I, DIFF	Transceiver Bank1F channel3 High speed differential receiver negative.
8	A8	GND	NA	NA	GND	NA	NA	Power	Ground.
9	A9	GND	NA	NA	GND	NA	NA	Power	Ground.
10	A10	DP3_M2C_P	Board to Board Connector 3	B23	GXBL1F_RX_CH4p	1F	AC36	I, DIFF	Transceiver Bank1F channel4 High speed differential receiver positive.
11	A11	DP3_M2C_N	Board to Board Connector 3	B22	GXBL1F_RX_CH4n	1F	AC35	I, DIFF	Transceiver Bank1F channel4 High speed differential receiver negative.
12	A12	GND	NA	NA	GND	NA	NA	Power	Ground.
13	A13	GND	NA	NA	GND	NA	NA	Power	Ground.
14	A14	DP4_M2C_P	Board to Board Connector 3	C9	GXBL1N_RX_CH0p	1N	C32	I, DIFF	Transceiver Bank1N channel0 High speed differential receiver positive.
15	A15	DP4_M2C_N	Board to Board Connector 3	C8	GXBL1N_RX_CH0n	1N	C31	I, DIFF	Transceiver Bank1N channel0 High speed differential receiver negative.
16	A16	GND	NA	NA	GND	NA	NA	Power	Ground.
17	A17	GND	NA	NA	GND	NA	NA	Power	Ground.
18	A18	DP5_M2C_P	Board to Board Connector 3	C29	GXBL1N_RX_CH1n	1N	B29	I, DIFF	Transceiver Bank1N channel1 High speed differential receiver positive.
19	A19	DP5_M2C_N	Board to Board Connector 3	C28	GXBL1N_RX_CH1p	1N	B30	I, DIFF	Transceiver Bank1N channel1 High speed differential receiver negative.
20	A20	GND	NA	NA	GND	NA	NA	Power	Ground.
21	A21	GND	NA	NA	GND	NA	NA	Power	Ground.
22	A22	DP1_C2M_P	Board to Board Connector 3	B30	GXBL1F_TX_CH1p	1F	AF42	O, DIFF	Transceiver Bank1F channel1 High speed differential transmitter positive.
23	A23	DP1_C2M_N	Board to Board Connector 3	B31	GXBL1F_TX_CH1n	1F	AF41	O, DIFF	Transceiver Bank1F channel1 High speed differential transmitter negative.
24	A24	GND	NA	NA	GND	NA	NA	Power	Ground.
25	A25	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
26	**A26**	DP2_C2M_P	Board to Board Connector 3	A28	GXBL1F_TX_CH3p	1F	AD42	O, DIFF	Transceiver Bank1F channel3 High speed differential transmitter positive.
27	**A27**	DP2_C2M_N	Board to Board Connector 3	A29	GXBL1F_TX_CH3n	1F	AD41	O, DIFF	Transceiver Bank1F channel3 High speed differential transmitter negative.
28	**A28**	GND	NA	NA	GND	NA	NA	Power	Ground.
29	**A29**	GND	NA	NA	GND	NA	NA	Power	Ground.
30	**A30**	DP3_C2M_P	Board to Board Connector 3	B26	GXBL1F_TX_CH4p	1F	AC40	O, DIFF	Transceiver Bank1F channel4 High speed differential transmitter positive.
31	**A31**	DP3_C2M_N	Board to Board Connector 3	B27	GXBL1F_TX_CH4n	1F	AC39	O, DIFF	Transceiver Bank1F channel4 High speed differential transmitter negative.
32	**A32**	GND	NA	NA	GND	NA	NA	Power	Ground.
33	**A33**	GND	NA	NA	GND	NA	NA	Power	Ground.
34	**A34**	DP4_C2M_P	Board to Board Connector 3	C41	GXBL1N_TX_CH0p	1N	F38	O, DIFF	Transceiver Bank1N channel0 High speed differential transmitter positive.
35	**A35**	DP4_C2M_N	Board to Board Connector 3	C40	GXBL1N_TX_CH0n	1N	F37	O, DIFF	Transceiver Bank1N channel0 High speed differential transmitter negative.
36	**A36**	GND	NA	NA	GND	NA	NA	Power	Ground.
37	**A37**	GND	NA	NA	GND	NA	NA	Power	Ground.
38	**A38**	DP5_C2M_P	Board to Board Connector 3	C13	GXBL1N_TX_CH1p	1N	C40	O, DIFF	Transceiver Bank1N channel1 High speed differential transmitter positive.
39	**A39**	DP5_C2M_N	Board to Board Connector 3	C12	GXBL1N_TX_CH1n	1N	L37	O, DIFF	Transceiver Bank1N channel1 High speed differential transmitter negative.
40	**A40**	GND	NA	NA	GND	NA	NA	Power	Ground.
41	**B1**	CLK_DIR	NA	NA	NA	NA	NA	O, 3.3V	CLK-DIR This Pin is connected to 16th pin of LVDS IO Expander (U10).
42	**B2**	GND	NA	NA	GND	NA	NA	Power	Ground.
43	**B3**	GND	NA	NA	GND	NA	NA	Power	Ground.
44	**B4**	DP9_M2C_P	Board to Board Connector 3	D43	GXBL1L_RX_CH1p	1L	N36	I, DIFF	Transceiver Bank1L channel1 High speed differential receiver positive.
45	**B5**	DP9_M2C_N	Board to Board Connector 3	D42	GXBL1L_RX_CH1n	1L	N35	I, DIFF	Transceiver Bank1L channel1 High speed differential receiver Negative.
46	**B6**	GND	NA	NA	GND	NA	NA	Power	Ground.
47	**B7**	GND	NA	NA	GND	NA	NA	Power	Ground.
48	**B8**	DP8_M2C_P	Board to Board Connector 3	D51	GXBL1L_RX_CH0p	1L	P38	I, DIFF	Transceiver Bank1L channel0 High speed differential receiver positive.
49	**B9**	DP8_M2C_N	Board to Board Connector 3	D50	GXBL1L_RX_CH0n	1L	P37	I, DIFF	Transceiver Bank1L channel0 High speed differential receiver negative.
50	**B10**	GND	NA	NA	GND	NA	NA	Power	Ground.
51	**B11**	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
52	**B12**	DP7_M2C_P	Board to Board Connector 3	C25	GXBL1N_RX_CH4p	1N	D30	I, DIFF	Transceiver Bank1N channel4 High speed differential receiver positive.
53	**B13**	DP7_M2C_N	Board to Board Connector 3	C24	GXBL1N_RX_CH4n	1N	D29	I, DIFF	Transceiver Bank1N channel4 High speed differential receiver negative.
54	**B14**	GND	NA	NA	GND	NA	NA	Power	Ground.
55	**B15**	GND	NA	NA	GND	NA	NA	Power	Ground.
56	**B16**	DP6_M2C_P	Board to Board Connector 3	C4	GXBL1N_RX_CH3p	1N	A28	I, DIFF	Transceiver Bank1N channel3 High speed differential receiver positive.
57	**B17**	DP6_M2C_N	Board to Board Connector 3	C5	GXBL1N_RX_CH3n	1N	A27	I, DIFF	Transceiver Bank1N channel3 High speed differential receiver negative.
58	**B18**	GND	NA	NA	GND	NA	NA	Power	Ground.
59	**B19**	GND	NA	NA	GND	NA	NA	Power	Ground.
60	**B20**	GBTCLK1_M2C_P	Board to Board Connector 3	C20	REFCLK_GXBL1N_CHTp	1N	H34	I, DIFF	Transceiver Bank1N differential reference clock0 positive.
61	**B21**	GBTCLK1_M2C_N	Board to Board Connector 3	C21	REFCLK_GXBL1N_CHTn	1N	H33	I, DIFF	Transceiver Bank1N differential reference clock0 negative.
62	**B22**	GND	NA	NA	GND	NA	NA	Power	Ground.
63	**B23**	GND	NA	NA	GND	NA	NA	Power	Ground.
64	**B24**	DP9_C2M_P	Board to Board Connector 3	C57	GXBL1L_TX_CH1p	1L	P41	O, DIFF	Transceiver Bank1L channel1 High speed differential Transmitter positive.
65	**B25**	DP9_C2M_N	Board to Board Connector 3	C56	GXBL1L_TX_CH1n	1L	P42	O, DIFF	Transceiver Bank1L channel1 High speed differential Transmitter Negative.
66	**B26**	GND	NA	NA	GND	NA	NA	Power	Ground.
67	**B27**	GND	NA	NA	GND	NA	NA	Power	Ground.
68	**B28**	DP8_C2M_P	Board to Board Connector 3	C52	GXBL1L_TX_CH0p	1L	R40	O, DIFF	Transceiver Bank1L channel0 High speed differential transmitter positive.
69	**B29**	DP8_C2M_N	Board to Board Connector 3	C53	GXBL1L_TX_CH0n	1L	R39	O, DIFF	Transceiver Bank1L channel0 High speed differential transmitter negative.
70	**B30**	GND	NA	NA	GND	NA	NA	Power	Ground.
71	**B31**	GND	NA	NA	GND	NA	NA	Power	Ground.
72	**B32**	DP7_C2M_P	Board to Board Connector 3	C33	GXBL1N_TX_CH4p	1N	A36	O, DIFF	Transceiver Bank1N channel4 High speed differential transmitter positive.
73	**B33**	DP7_C2M_N	Board to Board Connector 3	C32	GXBL1N_TX_CH4n	1N	A35	O, DIFF	Transceiver Bank1N channel4 High speed differential transmitter negative.
74	**B34**	GND	NA	NA	GND	NA	NA	Power	Ground.
75	**B35**	GND	NA	NA	GND	NA	NA	Power	Ground.
76	**B36**	DP6_C2M_P	Board to Board Connector 3	C37	GXBL1N_TX_CH3p	1N	B38	O, DIFF	Transceiver Bank1N channel3 High speed differential transmitter positive.
77	**B37**	DP6_C2M_N	Board to Board Connector 3	C36	GXBL1N_TX_CH3n	1N	B37	O, DIFF	Transceiver Bank1N channel3 High speed differential transmitter negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
78	**B38**	GND	NA	NA	GND	NA	NA	Power	Ground.
79	**B39**	GND	NA	NA	GND	NA	NA	Power	Ground.
80	**B40**	RES0	NA	NA	NA	NA	NA	NA	NC.
81	**C1**	GND	NA	NA	GND	NA	NA	Power	Ground.
82	**C2**	DP0_C2M_P	Board to Board Connector 3	A32	GXBL1F_TX_CH0p	1F	AG40	O, DIFF	Transceiver Bank1F channel0 High speed differential transmitter positive.
83	**C3**	DP0_C2M_N	Board to Board Connector 3	A33	GXBL1F_TX_CH0n	1F	AG39	O, DIFF	Transceiver Bank1F channel0 High speed differential transmitter negative.
84	**C4**	GND	NA	NA	GND	NA	NA	Power	Ground.
85	**C5**	GND	NA	NA	GND	NA	NA	Power	Ground.
86	**C6**	DP0_M2C_P	Board to Board Connector 3	A40	GXBL1F_RX_CH0p	1F	AG36	I, DIFF	Transceiver Bank1F channel0 High speed differential receiver positive.
87	**C7**	DP0_M2C_N	Board to Board Connector 3	A41	GXBL1F_RX_CH0n	1F	AG35	I, DIFF	Transceiver Bank1F channel0 High speed differential receiver negative.
88	**C8**	GND	NA	NA	GND	NA	NA	Power	Ground.
89	**C9**	GND	NA	NA	GND	NA	NA	Power	Ground.
90	**C10**	LA06_P	Board to Board Connector 2	183	FPGA_LVDS2C_23p_IO3	2C	AY16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO23 differential positive.
91	**C11**	LA06_N	Board to Board Connector 2	181	FPGA_LVDS2C_23n_IO4	2C	AW16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO4 differential negative.
92	**C12**	GND	NA	NA	GND	NA	NA	Power	Ground.
93	**C13**	GND	NA	NA	GND	NA	NA	Power	Ground.
94	**C14**	LA10_P	Board to Board Connector 2	176	FPGA_LVDS2C_13p/CLKIN_0p	2C	AP19	IO, 1.8V LVDS	Transceiver Bank2C differential reference clock0 positive.
95	**C15**	LA10_N	Board to Board Connector 2	178	FPGA_LVDS2C_13n/CLKIN_0n	2C	AP18	IO, 1.8V LVDS	Transceiver Bank2C differential reference clock0 negative.
96	**C16**	GND	NA	NA	GND	NA	NA	Power	Ground.
97	**C17**	GND	NA	NA	GND	NA	NA	Power	Ground.
98	**C18**	LA14_P	Board to Board Connector 2	147	FPGA_LVDS2C_9p_IO31	2C	AL20	IO, 1.8V LVDS	FPGA Bank2C LVDS IO31 differential positive.
99	**C19**	LA14_N	Board to Board Connector 2	149	FPGA_LVDS2C_9n_IO32	2C	AL21	IO, 1.8V LVDS	FPGA Bank2C LVDS IO32 differential negative.
100	**C20**	GND	NA	NA	GND	NA	NA	Power	Ground.
101	**C21**	GND	NA	NA	GND	NA	NA	Power	Ground.
102	**C22**	LA18_P_CC	Board to Board Connector 2	152	FPGA_LVDS2C_16p_IO17	2C	AM18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO17 differential positive.
103	**C23**	LA18_N_CC	Board to Board Connector 2	154	FPGA_LVDS2C_16n_IO18	2C	AN18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO18 differential negative.
104	**C24**	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
105	**C25**	GND	NA	NA	GND	NA	NA	Power	Ground.
106	**C26**	LA27_P	Board to Board Connector 1	27	FPGA_LVDS3D_17p_IO15	3D	AE2	IO, 1.8V LVDS	FPGA Bank3D LVDS IO15 differential positive.
107	**C27**	LA27_N	Board to Board Connector 1	29	FPGA_LVDS3D_17n_IO16	3D	AE1	IO, 1.8V LVDS	FPGA Bank93 LVDS IO16 differential negative.
108	**C28**	GND	NA	NA	GND	NA	NA	Power	Ground.
109	**C29**	GND	NA	NA	GND	NA	NA	Power	Ground.
110	**C30**	SCL	NA	NA	I2C0_SD3_SCL	NA	NA	O, 3.3V LVCMOS	FMC+ I2C Clock Signal. This Pin is connected from 12th pin of I2C Bus switch (U29).
111	**C31**	SDA	NA	NA	I2C0_SD3_SDA	NA	NA	IO, 3.3V LVCMOS	FMC+ I2C Data Signal. This Pin is connected from 11th pin of I2C Bus switch (U29).
112	**C32**	GND	NA	NA	GND	NA	NA	Power	Ground.
113	**C33**	GND	NA	NA	GND	NA	NA	Power	Ground.
114	**C34**	GA0	NA	NA	NA	NA	NA	1K, PU	Geographical address 0
115	**C35**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
116	**C36**	GND	NA	NA	GND	NA	NA	Power	Ground.
117	**C37**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
118	**C38**	GND	NA	NA	GND	NA	NA	Power	Ground.
119	**C39**	3P3V	NA	NA	VCC_3V3_FMC+	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
120	**C40**	GND	NA	NA	GND	NA	NA	Power	Ground.
121	**D1**	PG_C2M	NA	NA	NA	NA	NA	O, 3.3V	Power Good Signal from Carrier to FMC Module. This Pin is connected to 18th pin of LVDS IO Expander (U10).
122	**D2**	GND	NA	NA	GND	NA	NA	Power	Ground.
123	**D3**	GND	NA	NA	GND	NA	NA	Power	Ground.
124	**D4**	GBTCLK0_M2C_P	Board to Board Connector 3	B38	REFCLK_GXBL1F_CHTp	1F	AD34	I, DIFF	Transceiver Bank1F differential reference clock0 positive.
125	**D5**	GBTCLK0_M2C_N	Board to Board Connector 3	B39	REFCLK_GXBL1F_CHTn	1F	AD33	I, DIFF	Transceiver Bank1F differential reference clock0 negative.
126	**D6**	GND	NA	NA	GND	NA	NA	Power	Ground.
127	**D7**	GND	NA	NA	GND	NA	NA	Power	Ground.
128	**D8**	LA01_P_CC	Board to Board Connector 2	132	FPGA_LVDS2C_2p_IO45	2C	AJ19	IO, 1.8V LVDS	FPGA Bank2C LVDS IO45 differential positive.
129	**D9**	LA01_N_CC	Board to Board Connector 2	134	FPGA_LVDS2C_2n_IO46	2C	AK18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO46 differential negative.
130	**D10**	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
131	**D11**	LA05_P	Board to Board Connector 2	148	FPGA_LVDS2C_14p_IO21	2C	AR18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO21 differential positive.
132	**D12**	LA05_N	Board to Board Connector 2	150	FPGA_LVDS2C_14n_IO22	2C	AR17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO22 differential negative.
133	**D13**	GND	NA	NA	GND	NA	NA	Power	Ground.
134	**D14**	LA09_P	Board to Board Connector 2	164	FPGA_LVDS2C_20p_IO9	2C	AV16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO9 differential positive.
135	**D15**	LA09_N	Board to Board Connector 2	166	FPGA_LVDS2C_22p_IO5	2C	BB18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO5 differential negative.
136	**D16**	GND	NA	NA	GND	NA	NA	Power	Ground.
137	**D17**	LA13_P	Board to Board Connector 2	169	FPGA_LVDS2C_15p/CLKOUT_0p	2C	AR19	IO, 1.8V LVDS	Bank2C differential reference clock0 positive.
138	**D18**	LA13_N	Board to Board Connector 2	171	FPGA_LVDS2C_15n/CLKOUT_0n	2C	AT19	IO, 1.8V LVDS	Bank2C differential reference clock0 negative.
139	**D19**	GND	NA	NA	GND	NA	NA	Power	Ground.
140	**D20**	LA17_P_CC	Board to Board Connector 2	144	FPGA_LVDS2C_8p_IO33	2C	AL14	IO, 1.8V LVDS	FPGA Bank2C LVDS IO33 differential positive.
141	**D21**	LA17_N_CC	Board to Board Connector 2	146	FPGA_LVDS2C_8n_IO34	2C	AM14	IO, 1.8V LVDS	FPGA Bank2C LVDS IO34 differential negative.
142	**D22**	GND	NA	NA	GND	NA	NA	Power	Ground.
143	**D23**	LA23_P	Board to Board Connector 1	32	FPGA_LVDS3D_14p_IO21	3D	AE3	IO, 1.8V LVDS	FPGA Bank3D LVDS IO21 differential positive.
144	**D24**	LA23_N	Board to Board Connector 1	34	FPGA_LVDS3D_14n_IO22	3D	AE4	IO, 1.8V LVDS	FPGA Bank3D LVDS IO22 differential negative.
145	**D25**	GND	NA	NA	GND	NA	NA	Power	Ground.
146	**D26**	LA26_P	Board to Board Connector 1	38	FPGA_LVDS3D_9p_IO31	3D	AD5	IO, 1.8V LVDS	FPGA Bank3D LVDS IO31 differential positive.
147	**D27**	LA26_N	Board to Board Connector 1	40	FPGA_LVDS3D_9n_IO32	3D	AC5	IO, 1.8V LVDS	FPGA Bank3D LVDS IO32 differential negative.
148	**D28**	GND	NA	NA	GND	NA	NA	Power	Ground.
149	**D29**	TCK	Board to Board Connector 2	31	PS_JTAG_TCK	503	AC26	I, 3.3V CMOS/ 49.9K PU	JTAG Test Clock. This Pin is connected to 31st pin of Board-to-Board Connector2 (J19) through Voltage level translator.
150	**D30**	TDI	Board to Board Connector 2	33	JTAG_TDO	NA	NA	O, 3.3V CMOS	JTAG Test Data Output. This Pin is connected to 33rd pin of Board-to-Board Connector2 (J19) through Voltage level translator.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
151	**D31**	TDO	NA	NA	NA	NA	NA	O, 3.3V CMOS	FMC+ Test Data Output. This pin is connected to D30th pin of FMC Connector(J22)
152	**D32**	3P3VAUX	NA	NA	VCC_3V3	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
153	**D33**	TMS	Board to Board Connector 2	29	PS_JTAG_TMS	503	AD26	I, 3.3V CMOS/ 49.9K PU	JTAG Test Mode Select. This Pin is connected to 29th pin of Board to Board Connector2 (J19) through Voltage level translator..
154	**D34**	TRST_L	Board to Board Connector 2	25	NC	NA	NA	NA	NC. This Pin is connected to 25th pin of Board to Board Connector2 (J8) through Voltage level translator.
155	**D35**	GA1	NA	NA	NA	NA	NA	1K, PU	Geographical address 1
156	**D36**	3P3V	NA	NA	VCC_3V3_FMC+	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
157	**D37**	GND	NA	NA	GND	NA	NA	Power	Ground.
158	**D38**	3P3V	NA	NA	VCC_3V3_FMC+	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
159	**D39**	GND	NA	NA	GND	NA	NA	Power	Ground.
160	**D40**	3P3V	NA	NA	VCC_3V3_FMC+	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.
161	**E1**	GND	NA	NA	GND	NA	NA	Power	Ground.
162	**E2**	HA01_P_CC	NA	NA	NC	NA	NA	NA	NC.
163	**E3**	HA01_N_CC	NA	NA	NC	NA	NA	NA	NC.
164	**E4**	GND	NA	NA	GND	NA	NA	Power	Ground.
165	**E5**	GND	NA	NA	GND	NA	NA	Power	Ground.
166	**E6**	HA05_P	Board to Board connector 1	128	NC	NA	NA	NA	NA
167	**E7**	HA05_N	Board to Board connector 1	134	NC	NA	NA	NA	NA
168	**E8**	GND	NA	NA	GND	NA	NA	Power	Ground.
169	**E9**	HA09_P	Board to Board connector 1	112	NC	NA	NA	NA	NA
170	**E10**	HA09_N	Board to Board connector 1	110	NC	NA	NA	NA	NA
171	**E11**	GND	NA	NA	GND	NA	NA	Power	Ground.
172	**E12**	HA13_P	NA	NA	NC	NA	NA	NA	NC.
173	**E13**	HA13_N	NA	NA	NC	NA	NA	NA	NC.
174	**E14**	GND	NA	NA	GND	NA	NA	Power	Ground.
175	**E15**	HA16_P	NA	NA	NC	NA	NA	NA	NC.
176	**E16**	HA16_N	NA	NA	NC	NA	NA	NA	NC.
177	**E17**	GND	NA	NA	GND	NA	NA	Power	Ground.
178	**E18**	HA20_P	NA	NA	NC	NA	NA	NA	NC.
179	**E19**	HA20_N	NA	NA	NC	NA	NA	NA	NC.
180	**E20**	GND	NA	NA	GND	NA	NA	Power	Ground.
181	**E21**	HB03_P	NA	NA	NC	NA	NA	NA	NC.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
182	**E22**	HB03_N	NA	NA	NC	NA	NA	NA	NC.
183	**E23**	GND	NA	NA	GND	NA	NA	Power	Ground.
184	**E24**	HB05_P	NA	NA	NC	NA	NA	NA	NC.
185	**E25**	HB05_N	NA	NA	NC	NA	NA	NA	NC.
186	**E26**	GND	NA	NA	GND	NA	NA	Power	Ground.
187	**E27**	HB09_P	NA	NA	NC	NA	NA	NA	NC.
188	**E28**	HB09_N	NA	NA	NC	NA	NA	NA	NC.
189	**E29**	GND	NA	NA	GND	NA	NA	Power	Ground.
190	**E30**	HB13_P	NA	NA	NC	NA	NA	NA	NC.
191	**E31**	HB13_N	NA	NA	NC	NA	NA	NA	NC.
192	**E32**	GND	NA	NA	GND	NA	NA	Power	Ground.
193	**E33**	HB19_P	NA	NA	NC	NA	NA	NA	NC.
194	**E34**	HB19_N	NA	NA	NC	NA	NA	NA	NC.
195	**E35**	GND	NA	NA	GND	NA	NA	Power	Ground.
196	**E36**	HB21_P	NA	NA	NC	NA	NA	NA	NC.
197	**E37**	HB21_N	NA	NA	NC	NA	NA	NA	NC.
198	**E38**	GND	NA	NA	GND	NA	NA	Power	Ground.
199	**E39**	VADJ	NA	NA	VCC_FMC+_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
200	**E40**	GND	NA	NA	GND	NA	NA	Power	Ground.
201	**F1**	PG_M2C	NA	NA	NA	NA	NA	I, 3.3V CMOS/ 10K PU	DNP. Power Good Signal from FMC Module to Carrier. This Pin is connected to 20th pin of LVDS IO Expander (U10).
202	**F2**	GND	NA	NA	GND	NA	NA	Power	Ground.
203	**F3**	GND	NA	NA	GND	NA	NA	Power	Ground.
204	**F4**	HA00_P_CC	NA	NA	NC	NA	NA	NA	NC.
205	**F5**	HA00_N_CC	NA	NA	NC	NA	NA	NA	NC.
206	**F6**	GND	NA	NA	GND	NA	NA	Power	Ground.
207	**F7**	HA04_P	Board to Board Connector 1	204	NC	NA	NA	NA	NC.
208	**F8**	HA04_N	Board to Board Connector 1	202	NC	NA	NA	NA	NC.
209	**F9**	GND	NA	NA	GND	NA	NA	Power	Ground.
210	**F10**	HA08_P	Board to Board Connector 1	153	NC	NA	NA	NA	NC.
211	**F11**	HA08_N	Board to Board Connector 1	151	NC	NA	NA	NA	NC.
212	**F12**	GND	NA	NA	GND	NA	NA	Power	Ground.
213	**F13**	HA12_P	Board to Board Connector 1	150	NC	NA	NA	NA	NC.
214	**F14**	HA12_N	Board to Board Connector 1	148	NC	NA	NA	NA	NC.
215	**F15**	GND	NA	NA	NC	NA	NA	Power	Ground.
216	**F16**	HA15_P	NA	NA	NC	NA	NA	NA	NC.
217	**F17**	HA15_N	NA	NA	NC	NA	NA	NA	NC.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
218	**F18**	GND	NA	NA	GND	NA	NA	Power	Ground.
219	**F19**	HA19_P	NA	NA	NC	NA	NA	NA	NC.
220	**F20**	HA19_N	Board to Board Connector 1	10	NC	NA	NA	NA	NC.
221	**F21**	GND	NA	NA	GND	NA	NA	Power	Ground.
222	**F22**	HB02_P	NA	NA	NC	NA	NA	NA	NC.
223	**F23**	HB02_N	NA	NA	NC	NA	NA	NA	NC.
224	**F24**	GND	NA	NA	GND	NA	NA	Power	Ground.
225	**F25**	HB04_P	NA	NA	NC	NA	NA	NA	NC.
226	**F26**	HB04_N	NA	NA	NC	NA	NA	NA	NC.
227	**F27**	GND	NA	NA	GND	NA	NA	Power	Ground.
228	**F28**	HB08_P	NA	NA	NC	NA	NA	NA	NC.
229	**F29**	HB08_N	NA	NA	NC	NA	NA	NA	NC.
230	**F30**	GND	NA	NA	GND	NA	NA	Power	Ground.
231	**F31**	HB12_P	NA	NA	NC	NA	NA	NA	NC.
232	**F32**	HB12_N	NA	NA	NC	NA	NA	NA	NC.
233	**F33**	GND	NA	NA	GND	NA	NA	Power	Ground.
234	**F34**	HB16_P	NA	NA	NC	NA	NA	NA	NC.
235	**F35**	HB16_N	NA	NA	NC	NA	NA	NA	NC.
236	**F36**	GND	NA	NA	GND	NA	NA	Power	Ground.
237	**F37**	HB20_P	NA	NA	NC	NA	NA	NA	NC.
238	**F38**	HB20_N	NA	NA	NC	NA	NA	NA	NC.
239	**F39**	GND	NA	NA	GND	NA	NA	Power	Ground.
240	**F40**	VADJ	NA	NA	VCC_FMC+_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
241	**G1**	GND	NA	NA	GND	NA	NA	Power	Ground.
242	**G2**	CLK1_M2C_P	Board to Board Connector 2	92	FPGA_LVDS3D_3p_IO43	3D	AB7	IO, 1.8V LVDS	FPGA Bank68 LVDS IO43 differential positive.
243	**G3**	CLK1_M2C_N	Board to Board Connector 2	94	FPGA_LVDS3D_3n_IO44	3D	AB8	IO, 1.8V LVDS	FPGA Bank68 LVDS IO44 differential negative.
244	**G4**	GND	NA	NA	GND	NA	NA	Power	Ground.
245	**G5**	GND	NA	NA	GND	NA	NA	Power	Ground.
246	**G6**	LA00_P_CC	Board to Board Connector 2	159	FPGA_LVDS2C_19p_IO11	2C	AW18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO11 differential positive.
247	**G7**	LA00_N_CC	Board to Board Connector 2	161	FPGA_LVDS2C_19n_IO12	2C	AY18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO12 differential negative.
248	**G8**	GND	NA	NA	GND	NA	NA	Power	Ground.
249	**G9**	LA03_P	Board to Board Connector 2	163	FPGA_LVDS2C_21p_IO7	2C	AU18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO7 differential positive.
250	**G10**	LA03_N	Board to Board Connector 2	165	FPGA_LVDS2C_21n_IO8	2C	AV18	IO, 1.8V LVDS	FPGA Bank2C LVDS IO8 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
251	**G11**	GND	NA	NA	GND	NA	NA	Power	Ground.
252	**G12**	LA08_P	Board to Board Connector 2	155	FPGA_LVDS2C_17p_IO15	2C	AT16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO15 differential positive.
253	**G13**	LA08_N	Board to Board Connector 2	157	FPGA_LVDS2C_17n_IO16	2C	AR16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO16 differential negative.
254	**G14**	GND	NA	NA	GND	NA	NA	Power	Ground.
255	**G15**	LA12_P	Board to Board Connector 2	175	FPGA_LVDS2C_12p/CLKIN_1p	2C	AJ26	IO, 1.8V LVDS	Bank2C differential reference clock1 positive.
256	**G16**	LA12_N	Board to Board Connector 2	177	FPGA_LVDS2C_12n/CLKIN_1n	2C	AJ25	IO, 1.8V LVDS	Bank2C differential reference clock1 negative.
257	**G17**	GND	NA	NA	GND	NA	NA	Power	Ground.
258	**G18**	LA16_P	Board to Board Connector 2	131	FPGA_LVDS2C_1p_IO47	2C	AM17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO47 differential positive.
259	**G19**	LA16_N	Board to Board Connector 2	133	FPGA_LVDS2C_1n_IO48	2C	AN17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO48 differential negative.
260	**G20**	GND	NA	NA	GND	NA	NA	Power	Ground.
261	**G21**	LA20_P	Board to Board Connector 2	145	FPGA_LVDS2C_7p_IO35	2C	AJ23	IO, 1.8V LVDS	FPGA Bank2C LVDS IO35 differential positive.
262	**G22**	LA20_N	Board to Board Connector 2	143	FPGA_LVDS2C_7n_IO36	2C	AH24	IO, 1.8V LVDS	FPGA Bank2C LVDS IO36 differential negative.
263	**G23**	GND	NA	NA	GND	NA	NA	Power	Ground.
264	**G24**	LA22_P	Board to Board Connector 1	84	FPGA_LVDS3D_12p/CLKIN_1p	3D	AD8	I, 1.8V LVDS	Bank3D differential reference clock1 positive.
265	**G25**	LA22_N	Board to Board Connector 1	82	FPGA_LVDS3D_12n/CLKIN_1n	3D	AD9	I, 1.8V LVDS	Bank3D differential reference clock1 negative.
266	**G26**	GND	NA	NA	GND	NA	NA	Power	Ground.
267	**G27**	LA25_P	Board to Board Connector 1	44	FPGA_LVDS3D_11p_IO27	3D	AD3	IO, 1.8V LVDS	FPGA Bank3D LVDS IO27 differential positive.
268	**G28**	LA25_N	Board to Board Connector 1	42	FPGA_LVDS3D_11n_IO28	3D	AD4	IO, 1.8V LVDS	FPGA Bank3D LVDS IO28 differential positive.
269	**G29**	GND	NA	NA	GND	NA	NA	Power	Ground.
270	**G30**	LA29_P	Board to Board Connector 1	16	FPGA_LVDS3D_18p_IO13	3D	AF5	IO, 1.8V LVDS	FPGA Bank3D LVDS IO13 differential positive.
271	**G31**	LA29_N	Board to Board Connector 1	18	FPGA_LVDS3D_18n_IO14	3D	AF6	IO, 1.8V LVDS	FPGA Bank3D LVDS IO14 differential negative.
272	**G32**	GND	NA	NA	GND	NA	NA	Power	Ground.
273	**G33**	LA31_P	Board to Board Connector 1	30	FPGA_LVDS3D_20p_IO9	3D	AF12	IO, 1.8V LVDS	FPGA Bank3D LVDS IO9 differential positive.
274	**G34**	LA31_N	Board to Board Connector 1	28	FPGA_LVDS3D_20n_IO10	3D	AF11	IO, 1.8V LVDS	FPGA Bank3D LVDS IO10 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
275	G35	GND	NA	NA	GND	NA	NA	Power	Ground.
276	G36	LA33_P	Board to Board Connector 1	130	FPGA_LVDS3I_13p/CLKIN_0p	3I	AA4	I, 1.8V LVDS	Bank3I differential reference clock0 positive.
277	G37	LA33_N	Board to Board Connector 1	132	FPGA_LVDS3I_13n/CLKIN_0n	3I	Y4	I, 1.8V LVDS	Bank3I differential reference clock0 negative.
278	G38	GND	NA	NA	GND	NA	NA	Power	Ground.
279	G39	VADJ	NA	NA	VCC_FMC+_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
280	G40	GND	NA	NA	GND	NA	NA	Power	Ground.
281	H1	VREF_A_M2C	NA	NA	NC	NA	NA	NA	NC.
282	H2	PRSNT_M2C_L	NA	NA	NA	NA	NA	I,3.3V/10K PU	Module Present Signal. This Pin is connected to 5th pin of LVDS IO Expander (U10).
283	H3	GND	NA	NA	GND	NA	NA	Power	Ground.
284	H4	CLK0_M2C_P	Board To Board Connector 2	104	FPGA_LVDS2B_20p_IO9	2B	AU22	IO, 1.8V LVDS	FPGA Bank2B LVDS IO9 differential positive.
285	H5	CLK0_M2C_N	Board To Board Connector 2	106	FPGA_LVDS2B_20n_IO10	2B	AV22	IO, 1.8V LVDS	FPGA Bank2B LVDS IO9 differential negative.
286	H6	GND	NA	NA	GND	NA	NA	Power	Ground.
287	H7	LA02_P	Board to Board Connector 2	156	FPGA_LVDS2C_18p_IO13	2C	AU17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO13 differential positive.
288	H8	LA02_N	Board to Board Connector 2	158	FPGA_LVDS2C_18n_IO14	2C	AT17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO14 differential negative.
289	H9	GND	NA	NA	GND	NA	NA	Power	Ground.
290	H10	LA04_P	Board to Board Connector 2	162	FPGA_LVDS2C_20p_IO9	2C	AV16	IO, 1.8V LVDS	FPGA Bank2C LVDS IO9 differential positive.
291	H11	LA04_N	Board to Board Connector 2	160	FPGA_LVDS2C_20n_IO10	2C	AV17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO10 differential negative.
292	H12	GND	NA	NA	GND	NA	NA	Power	Ground.
293	H13	LA07_P	Board to Board Connector 2	151	FPGA_LVDS2C_11p_IO27	2C	AK23	IO, 1.8V LVDS	FPGA Bank2C LVDS IO27 differential positive.
294	H14	LA07_N	Board to Board Connector 2	153	FPGA_LVDS2C_11n_IO28	2C	AL22	IO, 1.8V LVDS	FPGA Bank2C LVDS IO28 differential negative.
295	H15	GND	NA	NA	GND	NA	NA	Power	Ground.
296	H16	LA11_P	Board to Board Connector 2	170	FPGA_LVDS2C_10p/CLKOUT_1p	2C	AK22	IO, 1.8V LVDS	Bank2C differential reference clock1 positive.
297	H17	LA11_N	Board to Board Connector 2	172	FPGA_LVDS2C_10n/CLKOUT_1n	2C	AK21	IO, 1.8V LVDS	Bank2C differential reference clock1 negative.
298	H18	GND	NA	NA	GND	NA	NA	Power	Ground.
299	H19	LA15_P	Board to Board Connector 2	182	FPGA_LVDS2C_24p_IO1	2C	AY17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO1 differential positive.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
300	**H20**	LA15_N	Board to Board Connector 2	184	FPGA_LVDS2C_24n_IO2	2C	BA17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO2 differential negative.
301	**H21**	GND	NA	NA	GND	NA	NA	Power	Ground.
302	**H22**	LA19_P	Board to Board Connector 2	140	FPGA_LVDS2C_6p_IO37	2C	AL17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO37 differential positive.
303	**H23**	LA19_N	Board to Board Connector 2	142	FPGA_LVDS2C_6n_IO38	2C	AK17	IO, 1.8V LVDS	FPGA Bank2C LVDS IO38 differential negative.
304	**H24**	GND	NA	NA	GND	NA	NA	Power	Ground.
305	**H25**	LA21_P	Board to Board Connector 2	139	FPGA_LVDS2C_5p_IO39	2C	AM19	IO, 1.8V LVDS	FPGA Bank2C LVDS IO39 differential positive.
306	**H26**	LA21_N	Board to Board Connector 2	141	FPGA_LVDS2C_5n_IO40	2C	AM20	IO, 1.8V LVDS	FPGA Bank2C LVDS IO40 differential negative.
307	**H27**	GND	NA	NA	GND	NA	NA	Power	Ground.
308	**H28**	LA24_P	Board to Board Connector 1	12	FPGA_LVDS3D_16p_IO17	3D	AE7	IO, 1.8V LVDS	FPGA Bank3D LVDS IO17 differential positive.
309	**H29**	LA24_N	Board to Board Connector 1	14	FPGA_LVDS3D_16n_IO18	3D	AF7	IO, 1.8V LVDS	FPGA Bank3D LVDS IO18 differential negative.
310	**H30**	GND	NA	NA	GND	NA	NA	Power	Ground.
311	**H31**	LA28_P	Board to Board Connector 1	31	FPGA_LVDS3D_19p_IO11	3D	AE8	IO, 1.8V LVDS	FPGA Bank3D LVDS IO11 differential positive.
312	**H32**	LA28_N	Board to Board Connector 1	33	FPGA_LVDS3D_19n_IO12	3D	AE9	IO, 1.8V LVDS	FPGA Bank3D LVDS IO12 differential negative.
313	**H33**	GND	NA	NA	GND	NA	NA	Power	Ground.
314	**H34**	LA30_P	Board to Board Connector 1	58	FPGA_LVDS3D_13p/CLKIN_0p	3D	AE6	I, 1.8V LVDS	Bank3D differential reference clock0 positive.
315	**H35**	LA30_N	Board to Board Connector 1	56	FPGA_LVDS3D_13n/CLKIN_0n	3D	AD6	I, 1.8V LVDS	Bank3D differential reference clock0 negative.
316	**H36**	GND	NA	NA	GND	NA	NA	Power	Ground.
317	**H37**	LA32_P	Board to Board Connector 1	91	FPGA_LVDS3D_2p_IO45	3D	AB13	IO, 1.8V LVDS	FPGA Bank3D LVDS IO45 differential positive.
318	**H38**	LA32_N	Board to Board Connector 1	93	FPGA_LVDS3D_2n_IO46	3D	AB12	IO, 1.8V LVDS	FPGA Bank3D LVDS IO46 differential negative.
319	**H39**	GND	NA	NA	GND	NA	NA	Power	Ground.
320	**H40**	VADJ	NA	NA	VCC_FMC+_ADJ	NA	NA	O, 1.8V Power	Carrier Board Supply Voltage.
321	**J1**	GND	NA	NA	GND	NA	NA	Power	Ground.
322	**J2**	CLK3_BIDIR_P	NA	NA	NC	NA	NA	NA	NC.
323	**J3**	CLK3_BIDIR_N	NA	NA	NC	NA	NA	NA	NC.
324	**J4**	GND	NA	NA	GND	NA	NA	Power	Ground.
325	**J5**	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
326	**J6**	HA03_P	Board to Board Connector 1	238	NC	NA	NA	NA	NC.
327	**J7**	HA03_N	Board to Board Connector 1	236	NC	NA	NA	NA	NC.
328	**J8**	GND	NA	NA	GND	NA	NA	Power	Ground.
329	**J9**	HA07_P	Board to Board Connector 1	147	NC	NA	NA	NA	NC.
330	**J10**	HA07_N	Board to Board Connector 1	149	NC	NA	NA	NA	NC.
331	**J11**	GND	NA	NA	GND	NA	NA	Power	Ground.
332	**J12**	HA11_P	Board to Board Connector 1	154	NC	NA	NA	NA	NC.
333	**J13**	HA11_N	Board to Board Connector 1	152	NC	NA	NA	NA	NC.
334	**J14**	GND	NA	NA	GND	NA	NA	Power	Ground.
335	**J15**	HA14_P	NA	NA	NC	NA	NA	NA	NC.
336	**J16**	HA14_N	NA	NA	NC	NA	NA	NA	NC.
337	**J17**	GND	NA	NA	GND	NA	NA	Power	Ground.
338	**J18**	HA18_P	Board to Board Connector 1	172	NC	NA	NA	NA	NC.
339	**J19**	HA18_N	NA	NA	NC	NA	NA	NA	NC.
340	**J20**	GND	NA	NA	GND	NA	NA	Power	Ground.
341	**J21**	HA22_P	NA	NA	NC	NA	NA	NA	NC.
342	**J22**	HA22_N	NA	NA	NC	NA	NA	NA	NC.
343	**J23**	GND	NA	NA	GND	NA	NA	Power	Ground.
344	**J24**	HB01_P	NA	NA	NC	NA	NA	NA	NC.
345	**J25**	HB01_N	NA	NA	NC	NA	NA	NA	NC.
346	**J26**	GND	NA	NA	GND	NA	NA	Power	Ground.
347	**J27**	HB07_P	NA	NA	NC	NA	NA	NA	NC.
348	**J28**	HB07_N	NA	NA	NC	NA	NA	NA	NC.
349	**J29**	GND	NA	NA	GND	NA	NA	Power	Ground.
350	**J30**	HB11_P	NA	NA	NC	NA	NA	NA	NC.
351	**J31**	HB11_N	NA	NA	NC	NA	NA	NA	NC.
352	**J32**	GND	NA	NA	GND	NA	NA	Power	Ground.
353	**J33**	HB15_P	NA	NA	NC	NA	NA	NA	NC.
354	**J34**	HB15_N	NA	NA	NC	NA	NA	NA	NC.
355	**J35**	GND	NA	NA	GND	NA	NA	Power	Ground.
356	**J36**	HB18_P	NA	NA	NC	NA	NA	NA	NC.
357	**J37**	HB18_N	NA	NA	NC	NA	NA	NA	NC.
358	**J38**	GND	NA	NA	GND	NA	NA	Power	Ground.
359	**J39**	VIO_B_M2C	NA	NA	NC	NA	NA	NA	NC.
360	**J40**	GND	NA	NA	GND	NA	NA	Power	Ground.
361	**K1**	VREF_B_M2C	NA	NA	NC	NA	NA	NA	NC.
362	**K2**	GND	NA	NA	GND	NA	NA	Power	Ground.
363	**K3**	GND			GND	NA	NA	Power	Ground.
364	**K4**	CLK2_BIDIR_P	NA	NA	NA	NA	NA	NA	NA

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
365	K5	CLK2_BIDIR_N	NA	NA	NA	NA	NA	NA	NA
366	K6	GND	NA	NA	GND	NA	NA	Power	Ground.
367	K7	HA02_P	Board to Board Connector 1	108	NC	NA	NA	NA	NC.
368	K8	HA02_N	Board to Board Connector 1	106	NC	NA	NA	NA	NC.
369	K9	GND	NA	NA	GND	NA	NA	Power	Ground.
370	K10	HA06_P	Board to Board Connector 1	78	NC	NA	NA	NA	NC.
371	K11	HA06_N	Board to Board Connector 1	104	NC	NA	NA	NA	NC.
372	K12	GND	NA	NA	GND	NA	NA	Power	Ground.
373	K13	HA10_P	Board to Board Connector 1	136	NC	NA	NA	NA	NC.
374	K14	HA10_N	Board to Board Connector 1	138	NC	NA	NA	NA	NC.
375	K15	GND	NA	NA	GND	NA	NA	Power	Ground.
376	K16	HA17_P_CC	NA	NA	NC	NA	NA	NA	NC.
377	K17	HA17_N_CC	NA	NA	NC	NA	NA	NA	NC.
378	K18	GND	NA	NA	GND	NA	NA	Power	Ground.
379	K19	HA21_P	NA	NA	NC	NA	NA	NA	NC.
380	K20	HA21_N	NA	NA	NC	NA	NA	NA	NC.
381	K21	GND	NA	NA	GND	NA	NA	Power	Ground.
382	K22	HA23_P	NA	NA	NC	NA	NA	NA	NC.
383	K23	HA23_N	NA	NA	NC	NA	NA	NA	NC.
384	K24	GND	NA	NA	GND	NA	NA	Power	Ground.
385	K25	HB00_P_CC	NA	NA	NC	NA	NA	NA	NC.
386	K26	HB00_N_CC	NA	NA	NC	NA	NA	NA	NC.
387	K27	GND	NA	NA	GND	NA	NA	Power	Ground.
388	K28	HB06_P_CC	NA	NA	NC	NA	NA	NA	NC.
389	K29	HB06_N_CC	NA	NA	NC	NA	NA	NA	NC.
390	K30	GND	NA	NA	GND	NA	NA	Power	Ground.
391	K31	HB10_P	NA	NA	NC	NA	NA	NA	NC.
392	K32	HB10_N	NA	NA	NC	NA	NA	NA	NC.
393	K33	GND	NA	NA	GND	NA	NA	Power	Ground.
394	K34	HB14_P	NA	NA	NC	NA	NA	NA	NC.
395	K35	HB14_N	NA	NA	NC	NA	NA	NA	NC.
396	K36	GND	NA	NA	GND	NA	NA	Power	Ground.
397	K37	HB17_P_CC	NA	NA	NC	NA	NA	NA	NC.
398	K38	HB17_N_CC	NA	NA	NC	NA	NA	NA	NC.
399	K39	GND	NA	NA	GND	NA	NA	Power	Ground.
400	K40	VIO_B_M2C	NA	NA	NC	NA	NA	NA	NC.
401	L1	RES1	NA	NA	NC	NA	NA	NA	NC.
402	L2	GND	NA	NA	GND	NA	NA	Power	Ground.
403	L3	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
404	**L4**	GBTCLK4_M2C_P	Board to Board Connector 3	B42	REFCLK_GXBL1D_CHBp	1D	AP34	I, DIFF	Transceiver Bank1D differential reference clock0 positive.
405	**L5**	GBTCLK4_M2C_N	Board to Board Connector 3	B43	REFCLK_GXBL1D_CHBn	1D	AP33	I, DIFF	Transceiver Bank1D differential reference clock0 Negative.
406	**L6**	GND	NA	NA	GND	NA	NA	Power	Ground.
407	**L7**	GND	NA	NA	GND	NA	NA	Power	Ground.
408	**L8**	GBTCLK3_M2C_P	Board to Board Connector 4	A6	FPGA_LVDS2A_23p_IO3	2A	AW24	I, DIFF	FPGA Bank2A LVDS IO3 differential positive.
409	**L9**	GBTCLK3_M2C_N	Board to Board Connector 4	A7	FPGA_LVDS2A_23n_IO4	2A	AY24	I, DIFF	FPGA Bank2A LVDS IO4 differential negative.
410	**L10**	GND	NA	NA	GND	NA	NA	Power	Ground.
411	**L11**	GND	NA	NA	GND	NA	NA	Power	Ground.
412	**L12**	GBTCLK2_M2C_P	Board to Board Connector 3	C48	REFCLK_GXBL1L_CHTp	1L	T34	I, DIFF	Transceiver Bank1L differential reference clock0 positive.
413	**L13**	GBTCLK2_M2C_P	Board to Board Connector 3	C49	REFCLK_GXBL1L_CHTn	1L	T33	I, DIFF	Transceiver Bank1L differential reference clock0 Negative.
414	**L14**	GND	NA	NA	GND	NA	NA	Power	Ground.
415	**L15**	GND	NA	NA	GND	NA	NA	Power	Ground.
416	**L16**	SYNC_C2M_P	NA	NA	NC	NA	NA	NA	NC.
417	**L17**	SYNC_C2M_N	NA	NA	NC	NA	NA	NA	NC.
418	**L18**	GND	NA	NA	GND	NA	NA	Power	Ground.
419	**L19**	GND	NA	NA	GND	NA	NA	Power	Ground.
420	**L20**	REFCLK_C2M_P	NA	NA	NC	NA	NA	NA	NC.
421	**L21**	REFCLK_C2M_N	NA	NA	NC	NA	NA	NA	NC.
422	**L22**	GND	NA	NA	GND	NA	NA	Power	Ground.
423	**L23**	GND	NA	NA	GND	NA	NA	Power	Ground.
424	**L24**	REFCLK_M2C_P	NA	NA	NC	NA	NA	NA	NC.
425	**L25**	REFCLK_M2C_N	NA	NA	NC	NA	NA	NA	NC.
426	**L26**	GND	NA	NA	GND	NA	NA	Power	Ground.
427	**L27**	GND	NA	NA	GND	NA	NA	Power	Ground.
428	**L28**	SYNC_M2C_P	NA	NA	NC	NA	NA	NA	NC.
429	**L29**	SYNC_M2C_N	NA	NA	NC	NA	NA	NA	NC.
430	**L30**	GND	NA	NA	GND	NA	NA	Power	Ground.
431	**L31**	GND	NA	NA	GND	NA	NA	Power	Ground.
432	**L32**	RES2	NA	NA	NC	NA	NA	NA	NC.
433	**L33**	RES3	NA	NA	NC	NA	NA	NA	NC.
434	**L34**	GND	NA	NA	GND	NA	NA	Power	Ground.
435	**L35**	GND	NA	NA	GND	NA	NA	Power	Ground.
436	**L36**	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
437	L37	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
438	L38	GND	NA	NA	GND	NA	NA	Power	Ground.
439	L39	GND	NA	NA	GND	NA	NA	Power	Ground.
440	L40	12P0V	NA	NA	VCC_12V_FMC+	NA	NA	O, 12V Power	Carrier Board Supply Voltage.
441	M1	GND	NA	NA	GND	NA	NA	Power	Ground.
442	M2	DP23_M2C_P	Board to Board Connector 4	D16	FPGA_LVDS2A_12p/CLKIN_1p	2A	AM29	I, DIFF	Transceiver Bank2A channel3 High speed differential receiver positive.
443	M3	DP23_M2C_N	Board to Board Connector 4	D17	FPGA_LVDS2A_12n/CLKIN_1n	2A	AL29	I, DIFF	Transceiver Bank2A channel3 High speed differential receiver negative.
444	M4	GND	NA	NA	GND	NA	NA	Power	Ground.
445	M5	GND	NA	NA	GND	NA	NA	Power	Ground.
446	M6	DP22_M2C_P	Board to Board Connector 4	C14	FPGA_LVDS2A_6p_IO37	2A	AR29	I, DIFF	FPGA Bank2A LVDS IO37 differential positive.
447	M7	DP22_M2C_N	Board to Board Connector 4	C15	FPGA_LVDS2A_6n_IO38	2A	AT29	I, DIFF	FPGA Bank2A LVDS IO38 differential negative.
448	M8	GND	NA	NA	GND	NA	NA	Power	Ground.
449	M9	GND	NA	NA	GND	NA	NA	Power	Ground.
450	M10	DP21_M2C_P	Board to Board Connector 4	D13	FPGA_LVDS2A_2p_IO45	2A	AL30	I, DIFF	FPGA Bank2A LVDS IO45 differential positive.
451	M11	DP21_M2C_N	Board to Board Connector 4	D12	FPGA_LVDS2A_2n_IO46	2A	AM30	I, DIFF	FPGA Bank2A LVDS IO46 differential negative.
452	M12	GND	NA	NA	GND	NA	NA	Power	Ground.
453	M13	GND	NA	NA	GND	NA	NA	Power	Ground.
454	M14	DP20_M2C_P	Board to Board Connector 4	C19	FPGA_LVDS2A_5p_IO39	2A	AP28	I, DIFF	FPGA Bank2A LVDS IO39 differential positive.
455	M15	DP20_M2C_N	Board to Board Connector 4	C18	FPGA_LVDS2A_5n_IO40	2A	AR28	I, DIFF	FPGA Bank2A LVDS IO40 differential negative.
456	M16	GND	NA	NA	GND	NA	NA	Power	Ground.
457	M17	GND	NA	NA	GND	NA	NA	Power	Ground.
458	M18	DP14_C2M_P	Board to Board Connector 4	A18	FPGA_LVDS2A_20p_IO9	2A	AV25	O, DIFF	FPGA Bank2A LVDS IO9 differential positive.
459	M19	DP14_C2M_N	Board to Board Connector 4	A19	FPGA_LVDS2A_20n_IO10	2A	AW25	O, DIFF	FPGA Bank2A LVDS IO10 differential negative.
460	M20	GND	NA	NA	GND	NA	NA	Power	Ground.
461	M21	GND	NA	NA	GND	NA	NA	Power	Ground.
462	M22	DP15_C2M_P	Board to Board Connector 4	B12	FPGA_LVDS2A_16p_IO17	2A	BB25	O, DIFF	FPGA Bank2A LVDS IO17 differential positive.
463	M23	DP15_C2M_N	Board to Board Connector 4	B13	FPGA_LVDS2A_16n_IO18	2A	BA25	O, DIFF	FPGA Bank2A LVDS IO18 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
464	M24	GND	NA	NA	GND	NA	NA	Power	Ground.
465	M25	GND	NA	NA	GND	NA	NA	Power	Ground.
466	M26	DP16_C2M_P	Board to Board Connector 3	A44	GXBL1D_TX_CH5p	1D	AP42	O, DIFF	Transceiver Bank1D channel5 High speed differential Transmitter positive.
467	M27	DP16_C2M_N	Board to Board Connector 3	A45	GXBL1D_TX_CH5n	1D	AP41	O, DIFF	Transceiver Bank1D channel5 High speed differential Transmitter Negative.
468	M28	GND	NA	NA	GND	NA	NA	Power	Ground.
469	M29	GND	NA	NA	GND	NA	NA	Power	Ground.
470	M30	DP17_C2M_P	Board to Board Connector 3	B46	GXBL1L_TX_CH5p	1D	K42	O, DIFF	Transceiver Bank1L channel5 High speed differential Transmitter positive.
471	M31	DP17_C2M_N	Board to Board Connector 3	B47	GXBL1L_TX_CH5n	1D	K41	O, DIFF	Transceiver Bank1L channel5 High speed differential Transmitter Negative.
472	M32	GND	NA	NA	GND	NA	NA	Power	Ground.
473	M33	GND	NA	NA	GND	NA	NA	Power	Ground.
474	M34	DP18_C2M_P	Board to Board Connector 3	A52	GXBL1F_TX_CH5p	1F	AB42	O, DIFF	Transceiver Bank1F channel5 High speed differential transmitter positive.
475	M35	DP18_C2M_N	Board to Board Connector 3	A53	GXBL1F_TX_CH5n	1F	AB41	O, DIFF	Transceiver Bank1F channel5 High speed differential transmitter negative.
476	M36	GND	NA	NA	GND	NA	NA	Power	Ground.
477	M37	GND	NA	NA	GND	NA	NA	Power	Ground.
478	M38	DP19_C2M_P	Board to Board Connector 3	A48	GXBL1N_TX_CH5p	1F	B34	O, DIFF	Transceiver Bank1N channel5 High speed differential transmitter positive.
479	M39	DP19_C2M_N	Board to Board Connector 3	A49	GXBL1N_TX_CH5n	1F	B33	O, DIFF	Transceiver Bank1N channel5 High speed differential transmitter negative.
480	M40	GND	NA	NA	GND	NA	NA	Power	Ground.
481	Y1	GND	NA	NA	GND	NA	NA	Power	Ground.
482	Y2	DP23_C2M_P	Board to Board Connector 4	C6	FPGA_LVDS2A_8p_IO33	2A	AK29	O, DIFF	FPGA Bank2A LVDS IO33 differential positive.
483	Y3	DP23_C2M_N	Board to Board Connector 4	C7	FPGA_LVDS2A_8n_IO34	2A	AK30	O, DIFF	FPGA Bank2A LVDS IO34 differential negative.
484	Y4	GND	NA	NA	GND	NA	NA	Power	Ground.
485	Y5	GND	NA	NA	GND	NA	NA	Power	Ground.
486	Y6	DP21_C2M_P	Board to Board Connector 4	D4	FPGA_LVDS2A_4p_IO41	2A	AP29	O, DIFF	FPGA Bank2A LVDS IO41 differential positive.
487	Y7	DP21_C2M_N	Board to Board Connector 4	D5	FPGA_LVDS2A_4n_IO42	2A	AR30	O, DIFF	FPGA Bank2A LVDS IO42 differential negative.
488	Y8	GND	NA	NA	GND	NA	NA	Power	Ground.
489	Y9	GND	NA	NA	GND	NA	NA	Power	Ground.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
490	**Y10**	DP10_M2C_P	Board to Board Connector 3	C45	GXBL1L_RX_CH3p	1L	K38	I, DIFF	Transceiver Bank1L channel3 High speed differential receiver positive.
491	**Y11**	DP10_M2C_N	Board to Board Connector 3	C44	GXBL1L_RX_CH3n	1L	K37	I, DIFF	Transceiver Bank1L channel3 High speed differential receiver Negative.
492	**Y12**	GND	NA	NA	GND	NA	NA	Power	Ground.
493	**Y13**	GND	NA	NA	GND	NA	NA	Power	Ground.
494	**Y14**	DP12_M2C_P	Board to Board Connector 4	B17	FPGA_LVDS2A_14p_IO21	2A	BA27	I, DIFF	FPGA Bank2A LVDS IO21 differential positive.
495	**Y15**	DP12_M2C_N	Board to Board Connector 4	B16	FPGA_LVDS2A_14n_IO22	2A	BB27	I, DIFF	FPGA Bank2A LVDS IO22 differential negative.
496	**Y16**	GND	NA	NA	GND	NA	NA	Power	Ground.
497	**Y17**	GND	NA	NA	GND	NA	NA	Power	Ground.
498	**Y18**	DP14_M2C_P	Board to Board Connector 4	B9	FPGA_LVDS2A_17p_IO15	2A	AW26	I, DIFF	FPGA Bank2A LVDS IO15 differential positive.
499	**Y19**	DP14_M2C_N	Board to Board Connector 4	B8	FPGA_LVDS2A_17n_IO16	2A	AY26	I, DIFF	FPGA Bank2A LVDS IO16 differential negative.
500	**Y20**	GND	NA	NA	GND	NA	NA	Power	Ground.
501	**Y21**	GND	NA	NA	GND	NA	NA	Power	Ground.
502	**Y22**	DP15_M2C_P	Board to Board Connector 4	B5	FPGA_LVDS2A_18p_IO13	2A	BB24	I, DIFF	FPGA Bank2A LVDS IO13 differential positive.
503	**Y23**	DP15_M2C_N	Board to Board Connector 4	B4	FPGA_LVDS2A_18n_IO14	2A	BA24	I, DIFF	FPGA Bank2A LVDS IO14 differential negative.
504	**Y24**	GND	NA	NA	GND	NA	NA	Power	Ground.
505	**Y25**	GND	NA	NA	GND	NA	NA	Power	Ground.
506	**Y26**	DP11_C2M_P	Board to Board Connector 3	D58	GXBL1L_TX_CH4p	1L	L40	O, DIFF	Transceiver Bank1L channel4 High speed differential Transmitter positive.
507	**Y27**	DP11_C2M_N	Board to Board Connector 3	D59	GXBL1L_TX_CH4n	1L	L39	O, DIFF	Transceiver Bank1L channel4 High speed differential Transmitter Negative.
508	**Y28**	GND	NA	NA	GND	NA	NA	Power	Ground.
509	**Y29**	GND	NA	NA	GND	NA	NA	Power	Ground.
510	**Y30**	DP13_C2M_P	Board to Board Connector 4	A14	FPGA_LVDS2A_21p_IO7	2A	AR27	O, DIFF	FPGA Bank2A LVDS IO7 differential positive.
511	**Y31**	DP13_C2M_N	Board to Board Connector 4	A15	FPGA_LVDS2A_21n_IO8	2A	AT26	O, DIFF	FPGA Bank2A LVDS IO8 differential negative.
512	**Y32**	GND	NA	NA	GND	NA	NA	Power	Ground.
513	**Y33**	GND	NA	NA	GND	NA	NA	Power	Ground.
514	**Y34**	DP17_M2C_P	Board to Board Connector 3	A56	GXBL1L_RX_CH5p	1L	H38	I, DIFF	Transceiver Bank1L channel5 High speed differential receiver positive.
515	**Y35**	DP17_M2C_N	Board to Board Connector 3	A57	GXBL1L_RX_CH5n	1L	H37	I, DIFF	Transceiver Bank1L channel5 High speed differential receiver Negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
516	**Y36**	GND	NA	NA	GND	NA	NA	Power	Ground.
517	**Y37**	GND	NA	NA	GND	NA	NA	Power	Ground.
518	**Y38**	DP19_M2C_P	Board to Board Connector 3	B58	GXBL1N_RX_CH5p	1N	F30	I, DIFF	Transceiver Bank1N channel5 High speed differential receiver positive.
519	**Y39**	DP19_M2C_N	Board to Board Connector 3	B59	GXBL1N_RX_CH5n	1N	F29	I, DIFF	Transceiver Ban1N channel5 High speed differential receiver negative.
520	**Y40**	GND	NA	NA	GND	NA	NA	Power	Ground.
521	**Z1**	HSPC_PRSNT_M2C_L	NA	NA	NA	NA	NA	I,3.3V/10K PU	FMC+ Module Present Signal. This Pin is connected to 6th pin of LVDS IO Expander (U10).
522	**Z2**	GND	NA	NA	GND	NA	NA	Power	Ground.
523	**Z3**	GND	NA	NA	GND	NA	NA	Power	Ground.
524	**Z4**	DP22_C2M_P	Board to Board Connector 4	C11	FPGA_LVDS2A_7p_IO35	2A	AM27	O, DIFF	FPGA Bank2A LVDS IO35 differential positive.
525	**Z5**	DP22_C2M_N	Board to Board Connector 4	C10	FPGA_LVDS2A_7n_IO36	2A	AL27	O, DIFF	FPGA Bank2A LVDS IO36 differential negative.
526	**Z6**	GND	NA	NA	GND	NA	NA	Power	Ground.
527	**Z7**	GND	NA	NA	GND	NA	NA	Power	Ground.
528	**Z8**	DP20_C2M_P	Board to Board Connector 4	C2	FPGA_LVDS2A_9p_IO31	2A	AP26	O, DIFF	FPGA Bank2A LVDS IO31 differential positive.
529	**Z9**	DP20_C2M_N	Board to Board Connector 4	C3	FPGA_LVDS2A_9n_IO32	2A	AN27	O, DIFF	FPGA Bank2A LVDS IO32 differential negative.
530	**Z10**	GND	NA	NA	GND	NA	NA	Power	Ground.
531	**Z11**	GND	NA	NA	GND	NA	NA	Power	Ground.
532	**Z12**	DP11_M2C_P	Board to Board Connector 3	D47	GXBL1L_RX_CH4p	1L	D47	I, DIFF	Transceiver Bank1L channel4 High speed differential receiver positive.
533	**Z13**	DP11_M2C_N	Board to Board Connector 3	D46	GXBL1L_RX_CH4n	1L	D46	I, DIFF	Transceiver Bank1L channel4 High speed differential receiver Negative.
534	**Z14**	GND	NA	NA	GND	NA	NA	Power	Ground.
535	**Z15**	GND	NA	NA	GND	NA	NA	Power	Ground.
536	**Z16**	DP13_M2C_P	Board to Board Connector 4	A3	FPGA_LVDS2A_24p_IO1	2A	AT25	I, DIFF	FPGA Bank2A LVDS IO1 differential positive.
537	**Z17**	DP13_M2C_N	Board to Board Connector 4	A2	FPGA_LVDS2A_24n_IO2	2A	AU25	I, DIFF	FPGA Bank2A LVDS IO2 differential negative.
538	**Z18**	GND	NA	NA	GND	NA	NA	Power	Ground.
539	**Z19**	GND	NA	NA	GND	NA	NA	Power	Ground.
540	**Z20**	GBTCLK5_M2C_P	Board to Board Connector 4	D9	FPGA_LVDS2A_11p_IO27	2A	AM28	I, DIFF	FPGA Bank2A LVDS IO27 differential positive.
541	**Z21**	GBTCLK5_M2C_N	Board to Board Connector 4	D8	FPGA_LVDS2A_11n_IO28	2A	AN28	I, DIFF	FPGA Bank2A LVDS IO28 differential negative.

Sl.no	FMC+ Connector VITA		Board to Board Connectors			Stratic10 SOC FPGA SOM			Description
	FMC+ Connector Pin No	FMC+ Connector Pin Name	Board to Board Connector Number	Board to Board Connector Pin Number	Board to Board Connector Signal Name (SOM)	SoC Bank	SoC Pin No	Signal Type/ Termination	
542	**Z22**	GND	NA	NA	GND	NA	NA	Power	Ground.
543	**Z23**	GND	NA	NA	GND	NA	NA	Power	Ground.
544	**Z24**	DP10_C2M_P	Board to Board Connector 3	D54	GXBL1L_TX_CH3p	1L	M42	O, DIFF	Transceiver Bank1L channel3 High speed differential Transmitter positive.
545	**Z25**	DP10_C2M_N	Board to Board Connector 3	D55	GXBL1L_TX_CH3n	1L	M41	O, DIFF	Transceiver Bank1L channel3 High speed differential Transmitter Negative.
546	**Z26**	GND	NA	NA	GND	NA	NA	Power	Ground.
547	**Z27**	GND	NA	NA	GND	NA	NA	Power	Ground.
548	**Z28**	DP12_C2M_P	Board to Board Connector 4	A10	FPGA_LVDS2A_22p_IO5	2A	AT27	O, DIFF	FPGA Bank2A LVDS IO6 differential positive.
549	**Z29**	DP12_C2M_N	Board to Board Connector 4	A11	FPGA_LVDS2A_22n_IO6	2A	AU27	O, DIFF	FPGA Bank2A LVDS IO6 differential negative.
550	**Z30**	GND	NA	NA	GND	NA	NA	Power	Ground.
551	**Z31**	GND	NA	NA	GND	NA	NA	Power	Ground.
552	**Z32**	DP16_M2C_P	Board to Board Connector 3	B50	GXBL1D_RX_CH5p	1D	AP38	I, DIFF	Transceiver Bank1D channel5 High speed differential receiver positive.
553	**Z33**	DP16_M2C_N	Board to Board Connector 3	B51	GXBL1D_RX_CH5n	1D	AP37	I, DIFF	Transceiver Bank1D channel5 High speed differential receiver Negative.
554	**Z34**	GND	NA	NA	GND	NA	NA	Power	Ground.
555	**Z35**	GND	NA	NA	GND	NA	NA	Power	Ground.
556	**Z36**	DP18_M2C_P	Board to Board Connector 3	B54	GXBL1F_RX_CH5p	1F	AA36	I, DIFF	Transceiver Bank1F channel5 High speed differential receiver positive.
557	**Z37**	DP18_M2C_N	Board to Board Connector 3	B55	GXBL1F_RX_CH5n	1F	AA35	I, DIFF	Transceiver Bank1F channel5 High speed differential receiver negative.
558	**Z38**	GND	NA	NA	GND	NA	NA	Power	Ground.
559	**Z39**	GND	NA	NA	GND	NA	NA	Power	Ground.
560	**Z40**	3P3V	NA	NA	VCC_3V3_FMC+	NA	NA	O, 3.3V Power	Carrier Board Supply Voltage.

Note:

** FMC+ connector supports VADJ 1.8V and 1.2V. By default, VADJ is set to 1.8V. Contact iWave for further details.*

** If VCC_FMC+_ADJ voltage changed from default value 1.8 to 1.2V, please make sure that SOM concern IO voltage also to be modified to avoid IO conflict.*

2.6 Additional Features

2.6.1 Clock Synthesizers

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports two 10-output Clock Synthesizer “SI5341B-D-GM” for on board clock distribution. This Clock Generator outputs are connected to Transceiver Banks Reference Clock on Board-to-Board Connectors through 0.01uF AC coupling capacitors. An external 48MHz crystal is connected to this Clock Synthesizer for reference. This Clock Synthesizer supports from 100 Hz to 1028 MHz clock output and is configured through HPS I2C0.

Table 16: Clock Synthesizer 1 Output Clocks

Pin No	Pin Name	Signal Name	Programmed Frequency	Connected To
23	OUT0b	GXBL1C_RX_CH5n	TBD	B2B-2 220th pin.
24	OUT0	GXBL1C_RX_CH5p		B2B-2 218th pin.
27	OUT1b	REFCLK_GXBL1C_CHTn	TBD	B2B-2 190th pin.
28	OUT1	REFCLK_GXBL1C_CHTp		B2B-2 188th pin.
30	OUT2b	GXBL1K_RX_CH5n	TBD	B21-1 169th pin.
31	OUT2	GXBL1K_RX_CH5p		B2B-1 171th pin.
34	OUT3b	GXBL1E_RX_CH5n	TBD	B2B-2 232th pin.
35	OUT3	GXBL1E_RX_CH5p		B2B-2 230th pin.
37	OUT4b	PCIe_REFCLKn	TBD	PCIex 4 connector A14th pin.
38	OUT4	PCIe_REFCLKP		PCIex 4 connector A13th pin.
41	OUT5b	GXBL1M_RX_CH5n	TBD	B2B-1 75th pin.
42	OUT5	GXBL1M_RX_CH5p		B2B-1 77th pin.
44	OUT6b	REFCLK_GXBL1M_CHBn	TBD	B2B-1 66th pin.
45	OUT6	REFCLK_GXBL1M_CHBp		B2B-1 64th pin.
50	OUT7b	REFCLK_GXBL1K_CHBn	TBD	B2B-1 160th pin.
51	OUT7	REFCLK_GXBL1K_CHBp		B2B-1 158th pin.
53	OUT8b	REFCLK_GXBL1E_CHBn	TBD	B2B-1 220th pin.
54	OUT8	REFCLK_GXBL1E_CHBp		B2B-1 218th pin.
58	OUT9b	REFCLK_GXBL1C_CHBn	TBD	B2B-2 225th pin.
59	OUT9	REFCLK_GXBL1C_CHBp		B2B-2 223th pin.

Table 17 Clock Synthesizer 2 Output Clocks

Pin No	Pin Name	Signal Name	Programmed Frequency	Connected To
23	OUT0b	CLKGEN_REFIN_N	TBD	B2B-3 A1st pin.
24	OUT0	CLKGEN_REFIN_P		B2B-3 A2nd pin.
27	OUT1b	NC	TBD	B2B-3 A20th pin.
28	OUT1	NC		B2B-3 A21st pin.
30	OUT2b	REFCLK_GXBL1N_CHBn	TBD	B2B-3 C16th pin.
31	OUT2	REFCLK_GXBL1N_CHBp		B2B-3 C17th pin.
34	OUT3b	FPGA_LVDS2A_19n_IO12	TBD	B2B-4 B1st pin.
35	OUT3	FPGA_LVDS2A_19p_IO11		B2B-4 B2nd pin.
37	OUT4b	REFCLK_GXBL1D_CHTn	TBD	B2B-3 B18th pin.
38	OUT4	REFCLK_GXBL1D_CHTp		B2B-3 B19th pin.
41	OUT5b	FPGA_LVDS2A_13n/CLKIN_0n	TBD	B2B-4 D19th pin.
42	OUT5	FPGA_LVDS2A_13p/CLKIN_0p		B2B-4 D20th pin.
44	OUT6b	NC	TBD	B2B-3 D38th pin.
45	OUT6	NC		B2B-3 D39th pin.
50	OUT7b	GXBL1D_TX_CH2p	TBD	B2B-3 B35th pin.
51	OUT7	GXBL1D_TX_CH2n		B2B-3 B34th pin.
53	OUT8b	NC	TBD	B2B-3 A59th pin.
54	OUT8	NC		B2B-3 A60th pin.
58	OUT9b	REFCLK_GXBL1L_CHBp	TBD	B2B-3 D2nd pin
59	OUT9	REFCLK_GXBL1L_CHBn		B2B-3 D3rd pin.

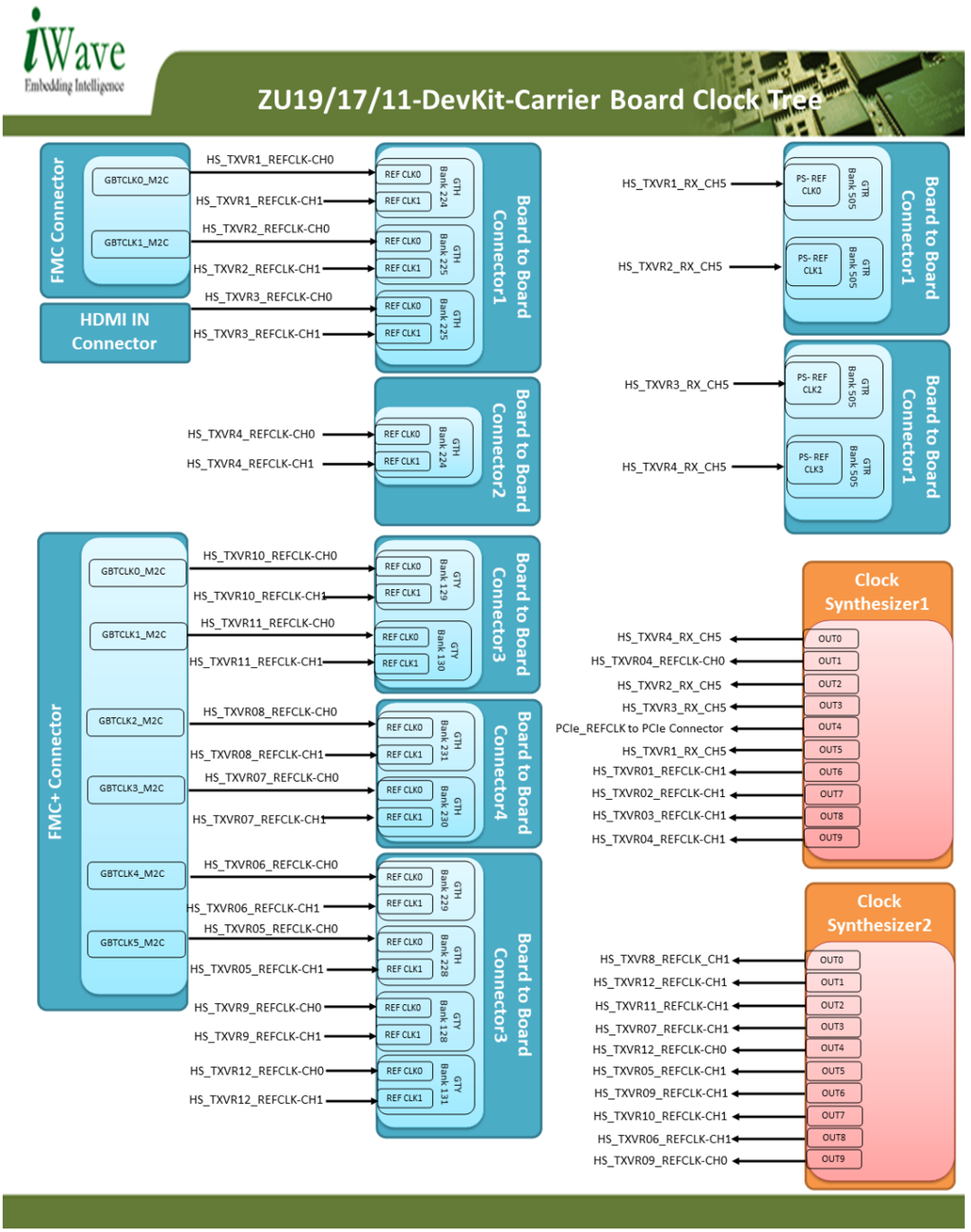

Figure 27: Clock Tree

2.6.2 JTAG Connector

A 14-pin JTAG Header is available in iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Carrier board for debug purpose. JTAG signals from Board-to-Board connector2 are directly connected to JTAG Header (J8) and same JTAG signals are also connected to FMC+ & FMC connector. JTAG-HS2/ JTAG-HS3 programming cable can be plugged to this JTAG Header for programming and debugging purpose. This JTAG Header (J8) is physically located at the top of the board as shown below.

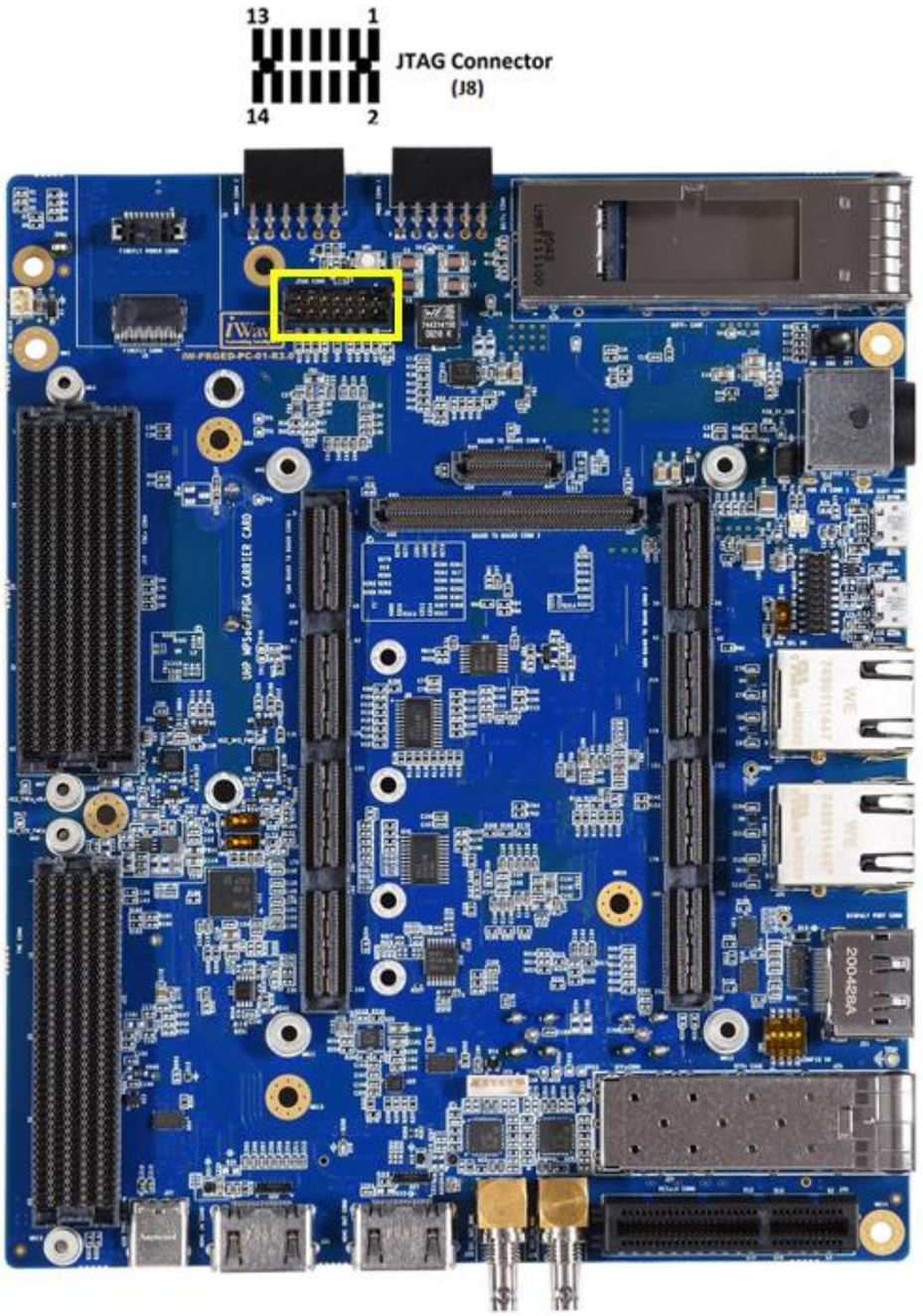

Figure 28: JTAG Connector

Table 18: JTAG Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	NC	-	Not Connected
2	VCC_3V3	O, 3.3V Power	3V3 Supply Voltage.
3	GND	Power	Ground
4	SDM_TMS_B2B	I, 3V3 LVCMOS/ 49.9K PU	JTAG test mode select.
5	GND	Power	Ground
6	SDM_TCK_B2B	I, 3V3 LVCMOS/ 49.9K PU	JTAG test Clock
7	GND	Power	Ground
8	SDM_TDO_B2B	O,3V3 LVCMOS/ 49.9K PU	JTAG test data output.
9	GND	Power	Ground
10	SDM_TDI_B2B	I, 3V3 LVCMOS	JTAG test data input
11	GND	Power	Ground
12	NC	-	Not Connected
13	GND	Power	Ground
14	NC	-	Not Connected (TP10)

2.6.3 IO Expanders

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA development Platform supports three GPIO 16-Bit port Expander. Refer below table for IO Expander pin mapping.

Table 19 IO EXPANDER 1 Output

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
IO EXPANDER 1 (TCA6416APWR) - I2C address : 0x20				
4	P00	IOEXP_P00_SFP_TFAULT	I, 3.3V CMOS/ 4.7K PU	Connected to SFP+
5	P01	IOEXP_P01_SFP_RX_LOS	I, 3.3V CMOS/ 4.7K PU	Connected to SFP+
6	P02	IOEXP_P02_SFP_MOD_ABS	I, 3.3V CMOS/ 4.7K PU	Connected to SFP+
7	P03	IOEXP_P03_SFP_RS1	I, 3.3V CMOS/ 4.7K PU	Connected to SFP+
8	P04	IOEXP_P04_SFP_RS0	O, 3.3V CMOS/ 4.7K PU	Connected to SFP+
9	P05	IOEXP_P05_SFP_TDIS	O, 3.3V CMOS/ 4.7K PD	Connected to SFP+
10	P06	IOEXP_P07_SDI_IN_CD_INT	I, 3.3V CMOS	Connected to SDI Video IN
11	P07	IOEXP_P10_SDI_CD_INT	I, 3.3V CMOS	Connected to SDI VIDEO OUT
13	P10	IOEXP_P11_MUX_SEL1	O, 3.3V CMOS	Connected to MUX Selection Switch
14	P11	IOEXP_P12_MUX_SEL2	O, 3.3V CMOS	Connected to MUX Selection Switch
15	P12	IOEXP_P13_MUX_SEL3	O, 3.3V CMOS	Connected to MUX Selection Switch
16	P13	IOEXP_P14_MUX_SEL4	O, 3.3V CMOS	Connected to MUX Selection Switch
17	P14	B_IO_EXP_INT2	I, 3.3V CMOS/ 4.7K PU	Connected to IO EXPANDER 2
18	P15	B_IO_EXP_INT3	I, 3.3V CMOS/ 4.7K PU	Connected to IO EXPANDER 3
19	P16	IOEXP_FMC_LA16P	IO, 1.8V CMOS	Connected to FMC connector G18th pin
20	P17	OEXP_HDMI_TX_CEC	I, 3.3V CMOS	Connected from HDMI OUT

Table 20 IO EXPANDER 2 Output

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
IO EXPANDER 2 (TCA6416APWR)- I2C address: 0x21				
4	P00	IOEXP_P00_Q_MODESEL	O, 3.3V CMOS/ 4.7K PD	Connected to QSFP28 Connector
5	P01	IOEXP_P01_Q_RESETL	O, 3.3V CMOS/ 4.7K PU	Connected to QSFP28 Connector
6	P02	IOEXP_P02_Q_LPMODE	O, 3.3V CMOS/ 4.7K PD	Connected to QSFP28 Connector
7	P03	IOEXP_P03_Q_INTL	I, 3.3V CMOS/ 4.7K PU	Connected to QSFP28 Connector
8	P04	IOEXP_P04_Q_MODPRSL	I, 3.3V CMOS/ 4.7K PU	Connected to QSFP28 Connector
9	P05	IOEXP_P05_F_RESETL	O, 3.3V CMOS/ 4.7K PU	Connected to FireFly Power Connector
10	P06	IOEXP_P06_F_MODSEL	O, 3.3V CMOS/ 4.7K PU	Connected to FireFly Power Connector
11	P07	IOEXP_P07_F_INTL	I, 3.3V CMOS/ 4.7K PU	Connected to FireFly Power Connector
13	P10	IOEXP_P10_F_MODPRS	I, 3.3V CMOS/ 4.7K PU	Connected to FireFly Power Connector
14	P11	IOEXP_P11_HDMI_TX_OE	O, 3.3V CMOS	Connected to IO HDMI OUT
15	P12	IOEXP_HDMI_RX_CEC_SINK	I, 3.3V CMOS	Connected to IO HDMI OUT
16	P13	NC	NC	NC.
17	P14	B_M2_PCI_RST#	O, 3.3V CMOS/ 4.7K PU	Connected to M.2 PCIe Connector
18	P15	B_M2_PCI_WAK#	I, 3.3V CMOS/ 4.7K PU	Connected to M.2 PCIe Connector
19	P16	B_PCI_CLKREQ#	I, 3.3V CMOS/ 4.7K PU	Connected to PCIex 4 Connector
20	P17	NC	NC	NC.

Table 21 IO EXPANDER 3 Output

Pin No	Pin Name	Signal Name	Signal Type / Termination	Description
IO EXPANDER 3 (TCA9535PWR)- I2C address : 0x23				
4	P00	B_FMC_PR_M2C_L	I, 3.3V CMOS/ 10K PU	Connected to FMC connector
5	P01	B_FMC+_PR_M2C_L	I, 3.3V CMOS/ 10K PU	Connected to FMC+ connector
6	P02	B_HSPC_PRSNT_M2C_L	I, 3.3V CMOS/ 10K PU	Connected to FMC+ connector
7	P03	EN_VCC_12V_FMC	O, 3.3V CMOS/ 10K PD	Connected to FMC Power
8	P04	EN_VCC_3V3_FMC	O, 3.3V CMOS/ 1K PD	Connected to FMC Power
9	P05	EN_VCC_FMC_ADJ	O, 3.3V CMOS/ 10K PD	Connected to FMC Power
10	P06	EN_VCC_FMC+_ADJ	O, 3.3V CMOS/ 10K PD	Connected to FMC+ Power
11	P07	B_PCI/SATA_CONFIG	O, 3.3V CMOS/ 10K PU	Connected to PCIex 4 Connector
13	P10	EN_VCC_12V_FMC+	O, 3.3V CMOS/ 10K PD	Connected to FMC+ Power
14	P11	EN_VCC_3V3_FMC+	O, 3.3V CMOS/ 1K PD	Connected to FMC+ Power
15	P12	B_FMC_CLK_DIR	I, 3.3V CMOS	Connected to FMC connector
16	P13	B_FMC+_CLK_DIR	I, 3.3V CMOS	Connected to FMC+ connector
17	P14	B_FMC_PG_C2M	O, 3.3V CMOS/ 10K PD	Connected to FMC connector
18	P15	B_FMC+_PG_C2M	O, 3.3V CMOS/ 10K PD	Connected to FMC+ connector
19	P16	B_FMC_PG_M2C	I, 3.3V CMOS/ 10K PD	Connected to FMC connector
20	P17	B_FMC+_PG_M2C	I, 3.3V CMOS/ 10K PD	Connected to FMC+ connector

2.6.4 I2C Expander

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports one 4 channel I2C Bus Switch (PI4MSD5V9546ALEX). I2C tree shown below.

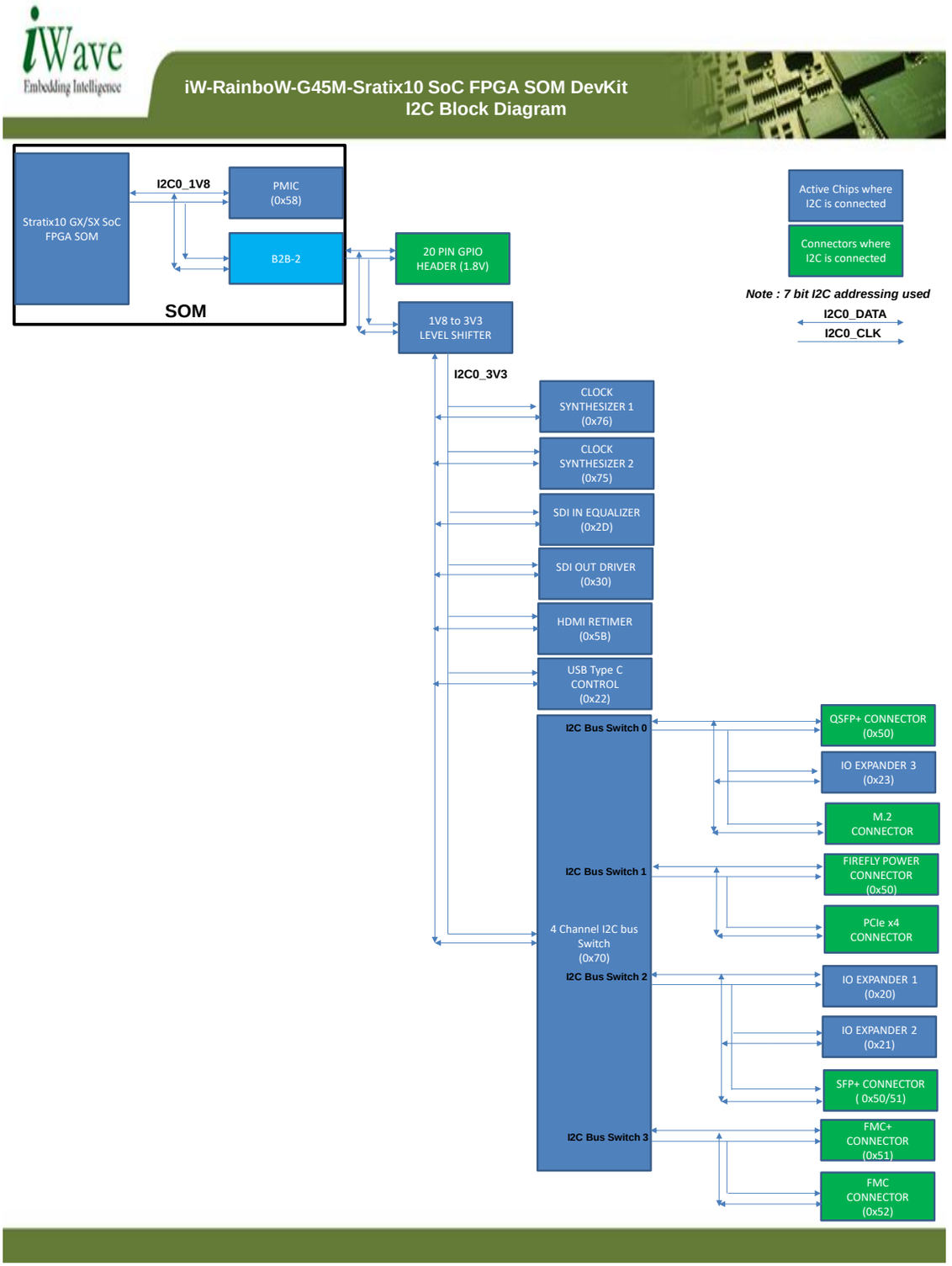

Figure 29 I2C Tree

2.6.5 GPIO Header

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports GPIO Header (J15) for General Purpose. This Header signals are directly connected from Board to Board 1 & 2 connectors. This header supports I2C0, UART1, SPI0, CAN1, HPS & FPGA GPIOs. This GPIO Header (J15) is physically located at the top of the board as shown below.

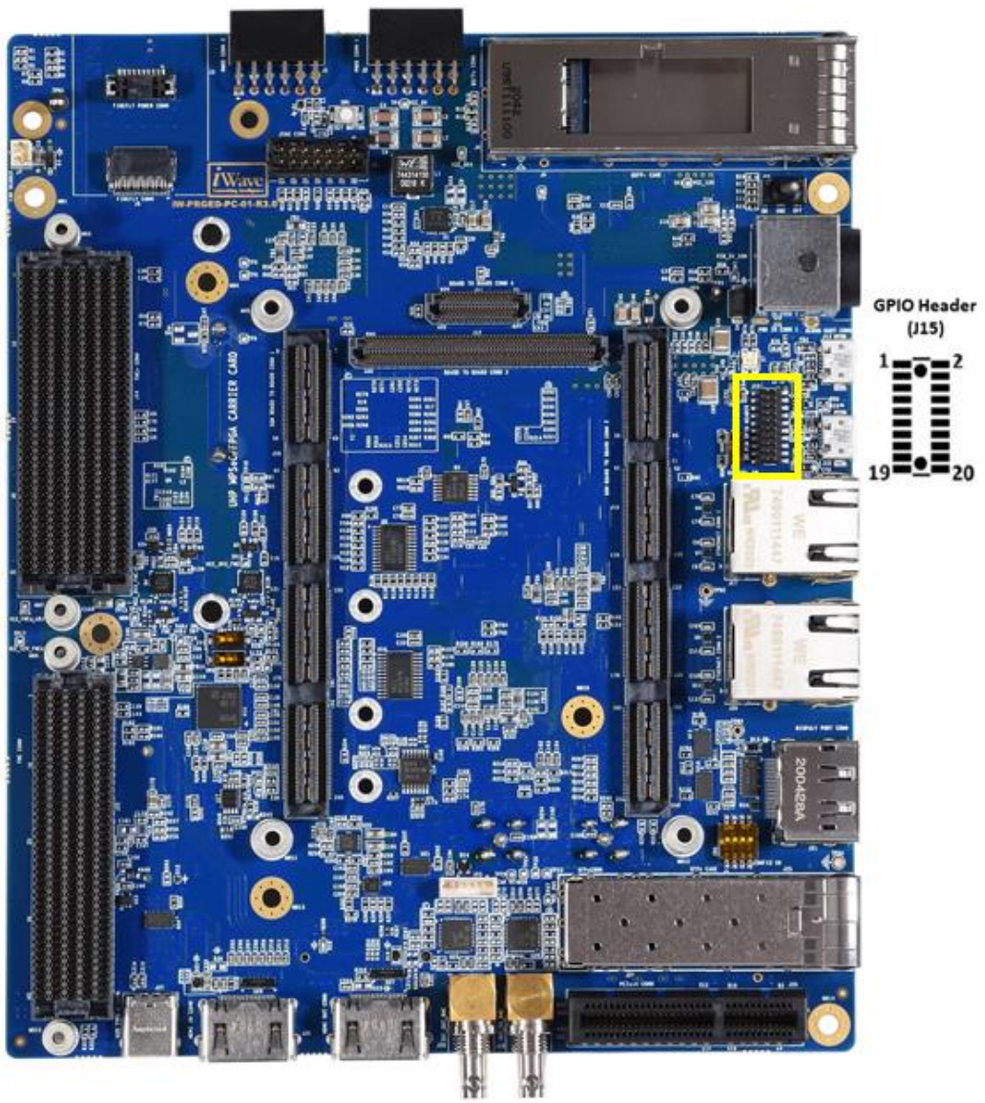

Figure 30: GPIO Header

Table 22: GPIO Header Pin Assignment

Pin No	Signal Name	Signal Type/ Termination	Description
1	VCC_1V8	O, 1.8V Power	1V8 Supply Voltage.
2	VCC_5V	O, 5V Power	5V Supply Voltage.
3	FPGA_LVDS3I_7p_IO35	I, 1.8V LVCMOS	This pin can be configured as General-Purpose Input/Output if required. This Pin is connected to 211th pin of Board-to-Board Connector1 (J8).

Pin No	Signal Name	Signal Type/ Termination	Description
4	HPS_I2C0_SDA	IO, 1.8V OD/ 4.7K PU	I2C0 data. This Pin is connected to 46th pin of Board-to-Board Connector2 (J19).
5	FPGA_LVDS3I_7n_IO36	O, 1.8V LVCMOS	This pin can be configured as General-Purpose Input/Output if required. This Pin is connected to 213rd pin of Board-to-Board Connector1 (J8).
6	HPS_I2C0_SCL	IO, 1.8V OD/ 4.7K PU	I2C0 Clock. This Pin is connected to 48th pin of Board-to-Board Connector2 (J19).
7	NC	NA	NC.
8	IO3V4_10	O, 1.8V LVCMOS	This pin can be configured as General-Purpose Input/Output if required. This Pin is connected to 50th pin of Board-to-Board Connector2 (J19).
9	FPGA_LVDS3I_2n_IO46	O, 1.8V LVCMOS	SPI Chip select 1. Same pin can be configured as General-Purpose Input/Output if required. This Pin is connected to 176rd pin of Board-to-Board Connector1 (J8).
10	IO3V5_10	I, 1.8V LVCMOS	This pin can be configured as General-Purpose Input/Output if required. This Pin is connected to 52nd pin of Board-to-Board Connector2 (J19).
11	GND	Power	Ground
12	GND	Power	Ground
13	HPS_SPIS0_CLK/UART0_CTS_N	O, 1.8V LVCMOS	SPI Clock output. Same pin can be configured as a UART0 CTS if required. This Pin is connected to 61st pin of Board-to-Board Connector2 (J19).
14	NC	NA	NC.
15	HPS_SPIS0_SS0_N/UART0_TX	O, 1.8V LVCMOS	SPI Chip select 0. Same pin can be configured as UART0_TX if required. This Pin is connected to 63rd pin of Board-to-Board Connector2 (J19).
16	NC	NA	NC.
17	HPS_SPIS0_MOSI/UART0_RTS	IO, 1.8V LVCMOS	SPI Master output Slave input. Same pin can be configured as UART0 RTS if required. This Pin is connected to 65th pin of Board-to-Board Connector2 (J19).
18	HPS_SPIS0_MISO/UART0_RX	IO, 1.8V LVCMOS	SPI Master input Slave output. Same pin can be configured as UART0_RX if required. This Pin is connected to 67th pin of Board-to-Board Connector2 (J19).
19	GND	Power	Ground
20	GND	Power	Ground

2.6.6 Power ON/OFF Switch

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform has power ON/OFF switch (SW2) to control the Main power Input ON/OFF functionality. This power ON/OFF switch is physically located at the top of the board as shown below.

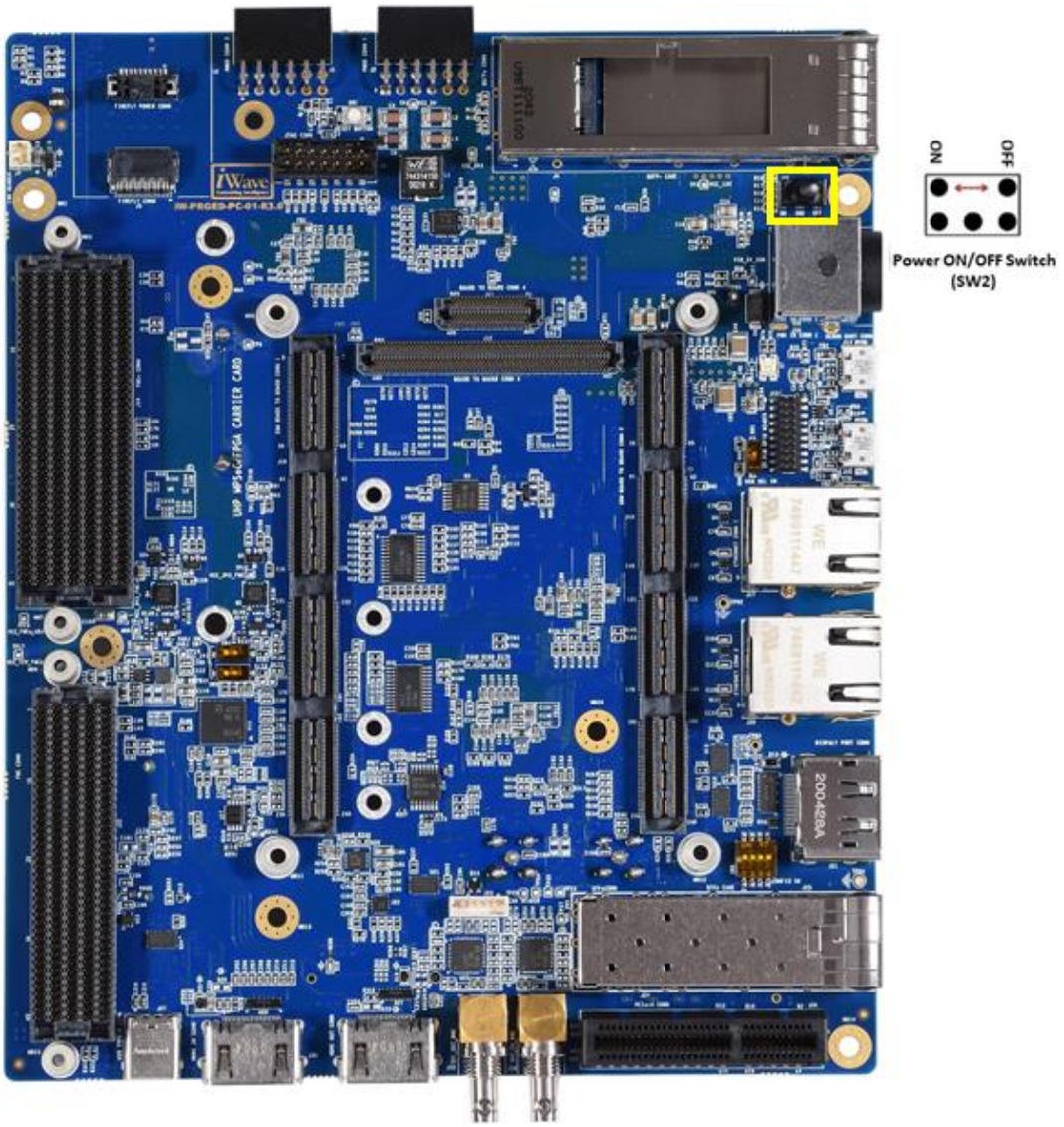

Figure 31: Power On/Off Switch

2.6.7 Reset Switch

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports Push button switch (SW1) to reset the iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM. Reset signal of Board-to-Board connector2 Pin 35 (RESET_SW_IN) is directly connected from Reset Push button switch. This Reset Push button switch (SW1) is physically located at the top of the board as shown below.

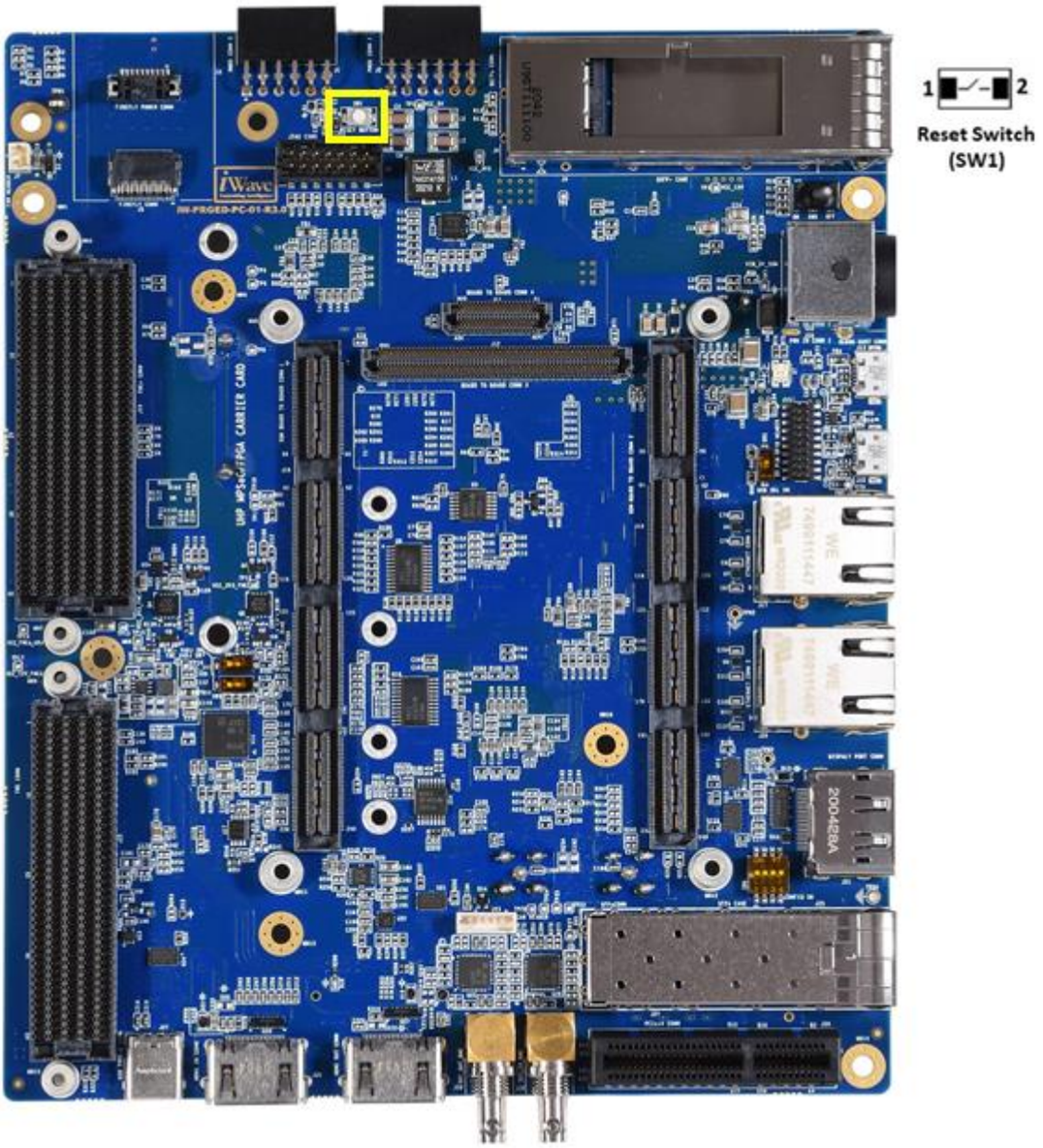

Figure 32: Reset Switch

2.6.8 RTC Coin Cell Holder

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports Coin Cell Holder to connect “2032” series 3V coin cell. This coin cell voltage is connected to iW-RainboW-G45M-Stratix10 GX/SX SoC SOM for RTC back up voltage when VCC main power is off. This Coin Cell Holder (J32) is physically located at the bottom of the board as shown below.

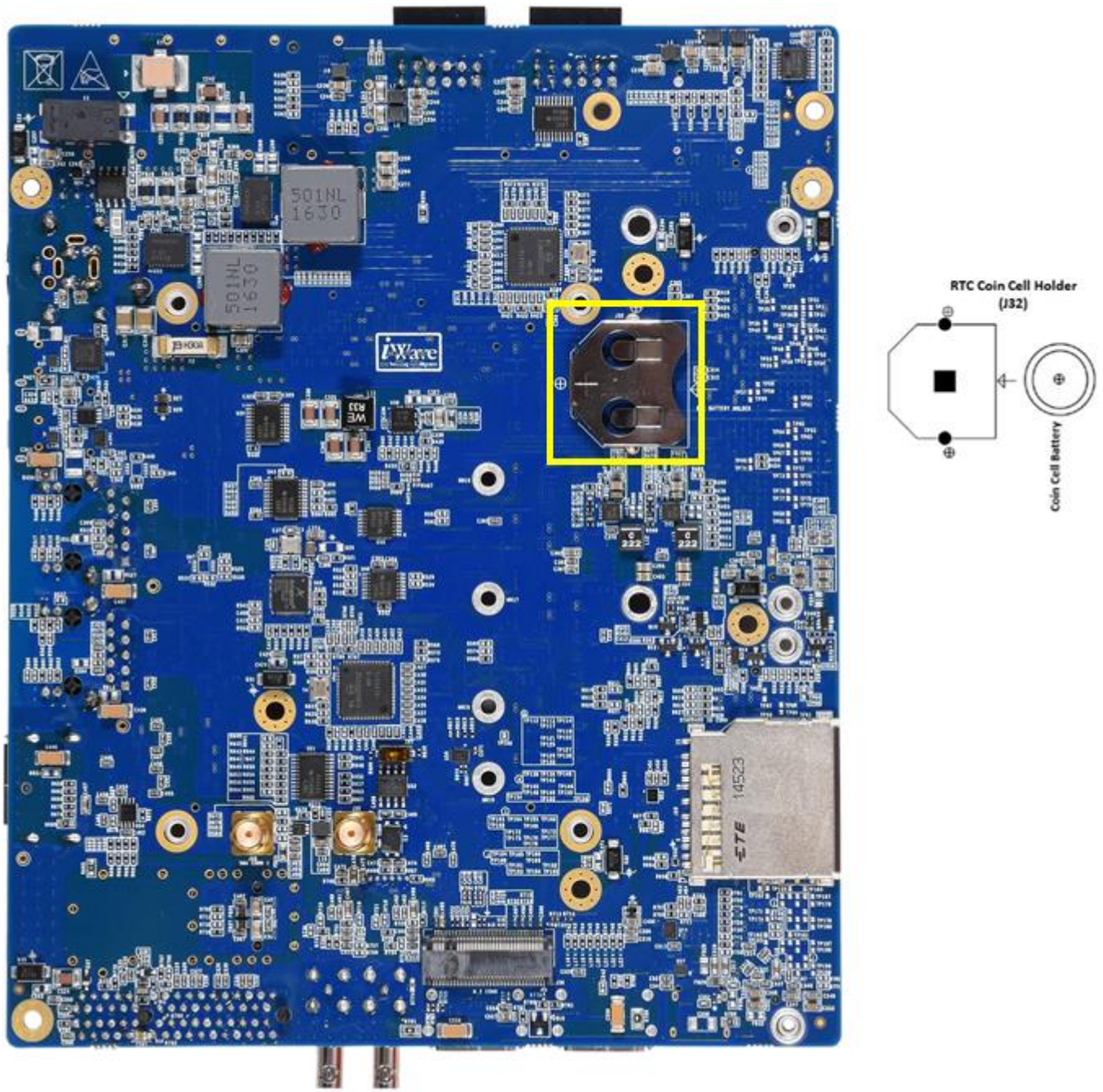

Figure 33: RTC Coin Cell Holder

2.6.9 12V Fan Header

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform supports a 12-Fan Header (J7) to connect cooling Fan if required. The Fan Header (J7) is physically located on topside of the carrier board as shown below.

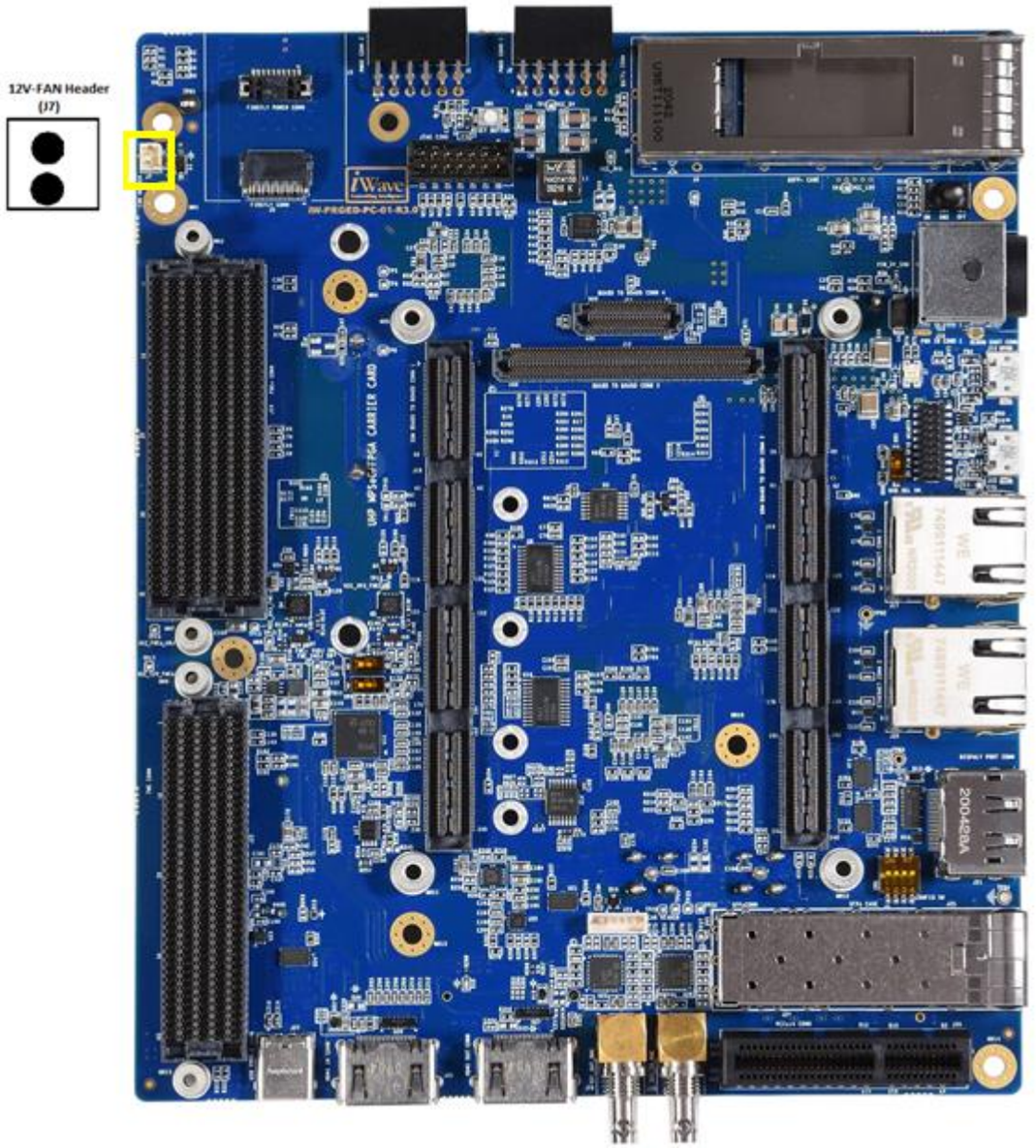

Figure 34: 12V-Fan Header

Table 23: 12V Fan Header Pinout

Sl. No.	Power Rail	Signal Type/ Termination	Description
1	VCC_12V [1]	O, 12V Power	Supply Voltage.
2	GND	Power	Ground.

[1] *Do not connect the SOM Heat Sink Fan to 12V FAN Connector in Carrier board. By Default, iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development platform comes with Heat Sink + Fan mounted on SOM itself.*

3. TECHNICAL SPECIFICATION

This section provides detailed information about the iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Carrier Board technical specification with Electrical, Environmental and Mechanical characteristics.

3.1 Power Input Requirement

The iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform is designed to work with 12V external power and uses on board voltage regulators for internal power management. 12V power input from an external power supply is connected to the iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Carrier Board through Power Jack (J10). This connector is physically placed at the top of the board as shown below.

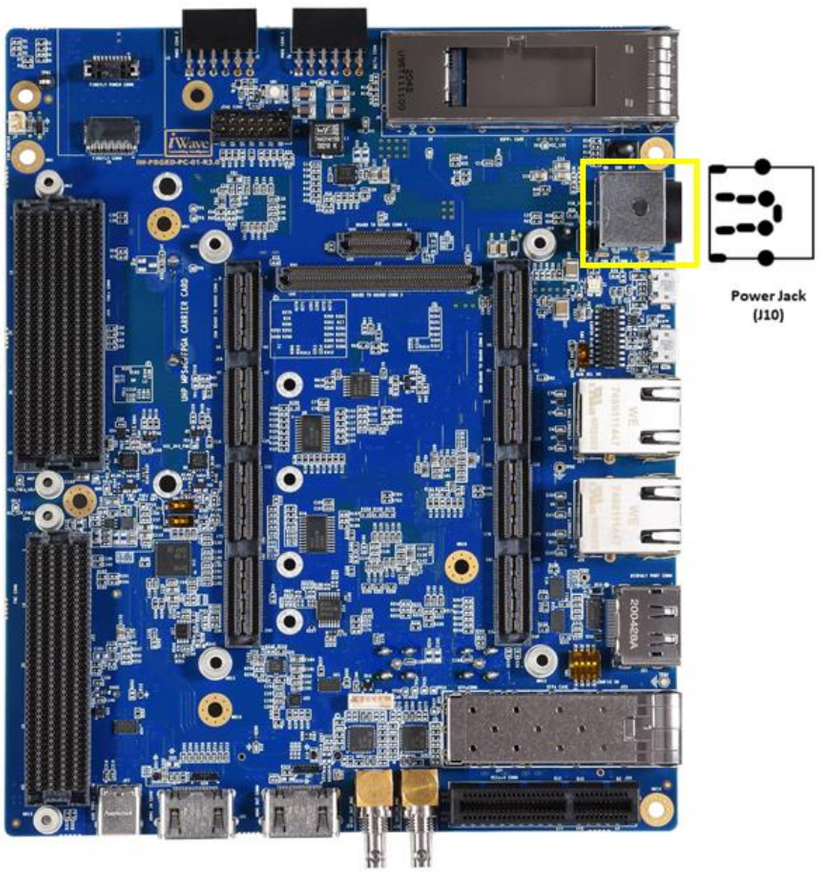

Figure 35: Power Jack

The below table provides the Power Input Requirement iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Carrier Board.

Table 24: Power Input Requirement

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Input Ripple
1	VCC_12V	11.75V	12V	12.25V	±50mV
2	VRTC_3V0[1]	0	3V	3.15V	±20mV

[1] *The iW-RainboW-G45D-Stratix10 DevKit uses this voltage as backup power source to On-SOM PMIC RTC controller when VCC is off.*

3.2 Power Output Specification

The Stratix10 Carrier Board has dedicated power regulator to provide +5V power to SOM for VCC power supply. Also +3V RTC power from coin cell holder is provided for Real time clock support.

The Stratix10 Carrier Board also shares different on-board power to FMC connectors, Pmod connectors and GPIO Header for its Add-On Module power.

Table 25: Power Output Specification

Sl. No.	Power Rail	Min (V)	Typical (V)	Max(V)	Max Output Current
To Board to Board Connector2 (for Stratix10 SOM)					
1	VCC_5V	4.85V	5V	5.15V	40A
2	VRTC_3V0	0V	3V	3.15V	-
To FMC Connector					
1	VCC_FMC_ADJ	1.75	1.8	1.85	4A
2	VCC_3V3	3.15	3.3	3.45	3A
3	3P3VAUX	3.15	3.3	3.45	100mA
4	VCC_12V	11.75V	12V	12.25V	1A
To FMC+ Connector					
1	VCC_FMC_ADJ	1.75	1.8	1.85	4A
2	VCC_3V3	3.15	3.3	3.45	3A
3	3P3VAUX	3.15	3.3	3.45	100mA
4	VCC_12V	11.75V	12V	12.25V	1A
To Pmod Connector1					
1	VCC_3V3	3.15	3.3	3.45	500mA
To Pmod Connector2					
1	VCC_3V3	3.15	3.3	3.45	500mA
To GPIO Header					
1	VCC_5V	3.15	3.3	3.45	500mA
2	VCC_1V8	1.75	1.8	1.85	200mA

3.3 Environmental Characteristics

3.3.1 Environmental Specification

The below table provides the Environment specification of iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development platform.

Table 26: Environmental Specification

Parameters	Min	Max
Operating temperature range[1]	0°C	70°C

[1] *iWave only guarantees the component selection for the given operating temperature.*

3.3.2 RoHS Compliance

iWave's iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development platform is designed by using RoHS compliant components and manufactured on lead free production process.

3.3.3 Electrostatic Discharge

iWave's iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development platform is sensitive to electro static discharge and so high voltages caused by static electricity could damage some of the devices on board. It is packed with necessary protection while shipping. Do not open or use board except at an electrostatic free workstation.

3.4 Mechanical Characteristics

3.4.1 Carrier Board Mechanical Dimensions

The Ultra-High-Performance Carrier board PCB form factor is 140mm x 170mm and Board mechanical dimension is shown below.

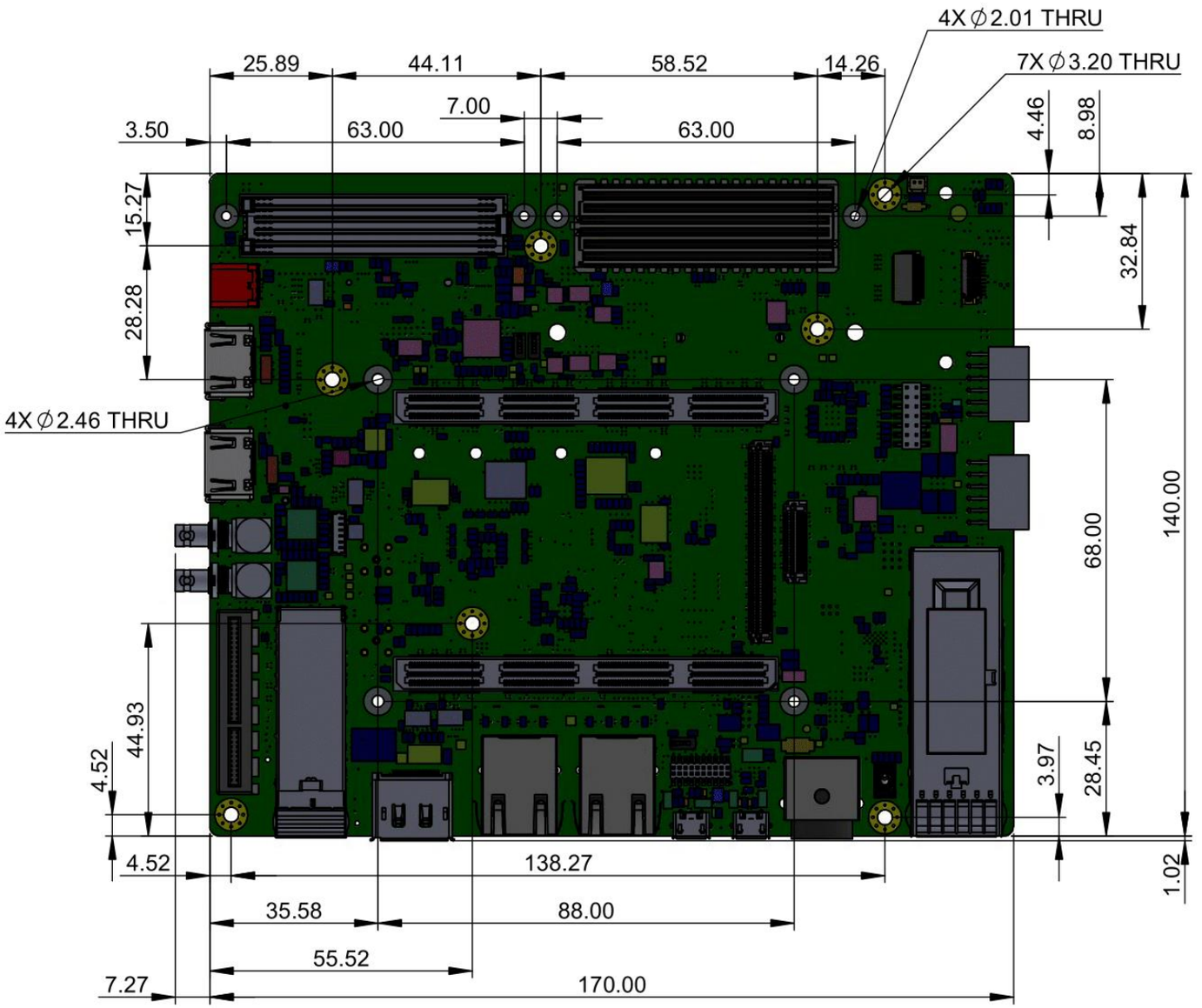

Figure 36: Carrier board Mechanical dimension – Top View

The Ultra-High-Performance Carrier board PCB thickness is 1.55mm±0.1mm, top side maximum height component is Ethernet Magjack Connector (15.00mm) and bottom side maximum height component is SMA Connector (9.55mm). Please refer the below figure for height details of the iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development Platform.

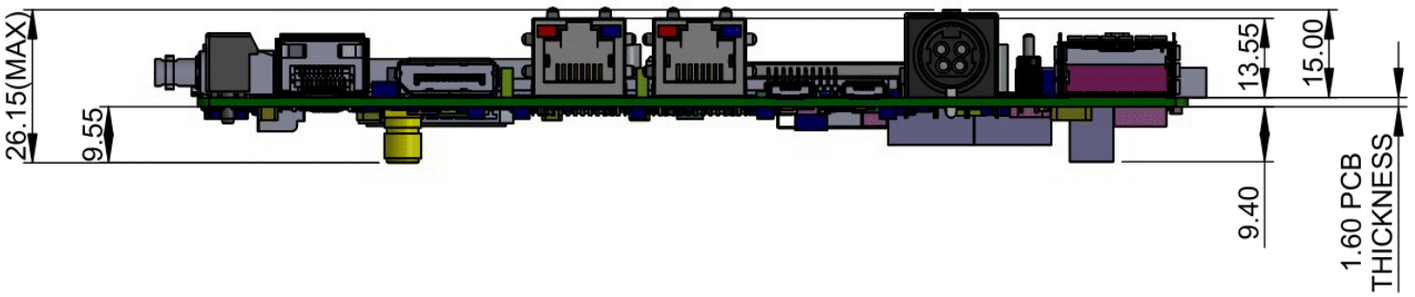

Figure 37: Carrier board Mechanical dimension – Side View

Guidelines to insert the iW-RainboW-G45M Stratix10 GX/SX SoC FPGA SOM into Carrier Board

- Make sure the power is not provided to the carrier Board
- Insert the iW-RainboW-G45M Stratix10 GX/SX SoC FPGA SOM in to the Board to Board(B2B).
- Check the position of B2B1, B2B2, B2B3 and B2B4 of Stratix10 SOM is proper while inserting.
- Press the SOM in to B2B connectors by applying pressure on the spacer areas such that the board is fixed firmly into the B2B connectors.
- Apply screws to fix them firmly in place.
- To remove the SOM from carrier board, remove the screws and lift the SOM near the B2B3 & B2B4 connectors by applying pressure on the spacers at the other end.

3.4.2 FAN Sink Fixing procedure on SOM with Carrier Board

Proper care must be taken when fixing the FAN Sink onto the Development board to avoid any damage to the board during the process. The procedure for fixing the FAN Sink onto the Development platform is available in the FAN Sink datasheet. Contact iWave if the FAN Sink datasheet is not available.

4. ORDERING INFORMATION

The below table provides the standard orderable part numbers for iW-RainboW-G45D-Stratix10 GX/SX SoC FPGA Development platform which includes iW-RainboW-G45M-Stratix10 GX/SX SoC FPGA SOM and Carrier Board.

Table 27: Orderable Product Part Numbers

Product Part Number	Description	Temperature
iW-G45D-S085-4E008G-E032G-BEA	SX850 (Speed - 2) Stratix 10 SOC, 8GB HPS DDR4 with ECC, Dual 8GB FPGA DDR4, 32GB eMMC, Extended	Extended

Note: For Development platform identification purpose, Product part number is pasted as Label with Barcode readable format.