AC/DC Secondary-Side Synchronous Rectification and Rapid Charge™ Interface Controller for AFC with DLNK Technology

NDA Confidential

1 Description

The iW661 is an AC/DC secondary-side combo controller for Samsung Adaptive Fast Charging (AFC) which includes USB interface, secondary-to-primary digital communication and synchronous rectification functions in a single IC.

The iW661 allows rapid charging of AFC enabled mobile devices (MDs). The iW661-11 also supports Qualcomm® Quick Charge™ 2.0 (QC 2.0) and automatically distingugishes between the AFC and QC 2.0 protocols. It resides on the secondary side of an AC/DC power supply and allows the adapter to be configured for multi-level output voltage and current.

The iW661 uses Dialog's proprietary secondary-to-primary digital link (DLNK) communication technology. When paired with Dialog's primary-side controller, the iW1791, the iW661 transmits all necessary information for rapid charge through a single optocoupler, including output voltage requests, output current limits, output voltage undershoot, output over-voltage, and fault and reset signals.

The iW661 is also an advanced synchronous rectifier (SR) controller with an integrated MOSFET driver, enabling discontinuous mode flyback converters with high efficiency operation. The device works with an external power MOSFET to replace the main rectifying diode on the secondary side of a flyback converter, improving efficiency by reducing secondary-side conduction losses. Dialog's digital adaptive turn-off control technology minimizes turn-off deadtime, eliminating the need for an additional Schottky diode that is typically needed in parallel with the synchronous MOSFET in conventional synchronous rectifiers.

In addition, the iW661 implements Dialog's proprietary D- impedance detection and D+/D- OVP to address soft short issues in the output cables and connectors that can be caused by such things as a poor or loose connection between the cable connector and the socket, contamination in the USB connector, or a worn-out cable, and provides protection against the damages. The iW661 can be used in Dialog's primary-side controlled AC/DC systems to achieve fast voltage transition, low no-load power consumption, and fast dynamic load response.

Qualcomm® Quick Charge™ 2.0 is a product of Qualcomm Technologies, Inc.

2 Features

- Proprietary secondary-to-primary digital communication transmits all information for rapid charge with a single optocoupler: output voltage requests, output current limits, output voltage undershoot, over-voltage protection, and other fault and reset signals
- Lossless MOSFET V_{DS} sensing for SR timing control with digital adaptive turn-off control
- Optimized 5V MOSFET gate driver
- High-voltage drain sensing up to 100V with no additional external clamping circuits required
- Supports Samsung AFC for multi-level output voltages and currents
- Backward compatible with USB Battery Charger Specification Revision 1.2 (USB BC1.2) Dedicated Charging Port (DCP)
- Supports Qualcomm Quick Charge 2.0 Class A High Voltage Dedicated Charging Port (HVDCP) with voltage configuration of 5V and 9V in iW661-11 and automatically differentiates between AFC and QC 2.0
- Proprietary D- impedance detection and D+/D- over-voltage protection (OVP) address soft short issues in the output cables and connectors and provides protection against damages
- Programmable active fast discharge from a high voltage to 5V at MD unplug or from a high voltage level to a lower level upon request with built-in switch or external switch
- Intelligent low power mode enables < 20mW no-load power consumption
- On-chip temperature sensing circuit
- 10-lead MSOP package

3 Applications

- AFC AC/DC adapters for smart phones, tablets, and other portable devices

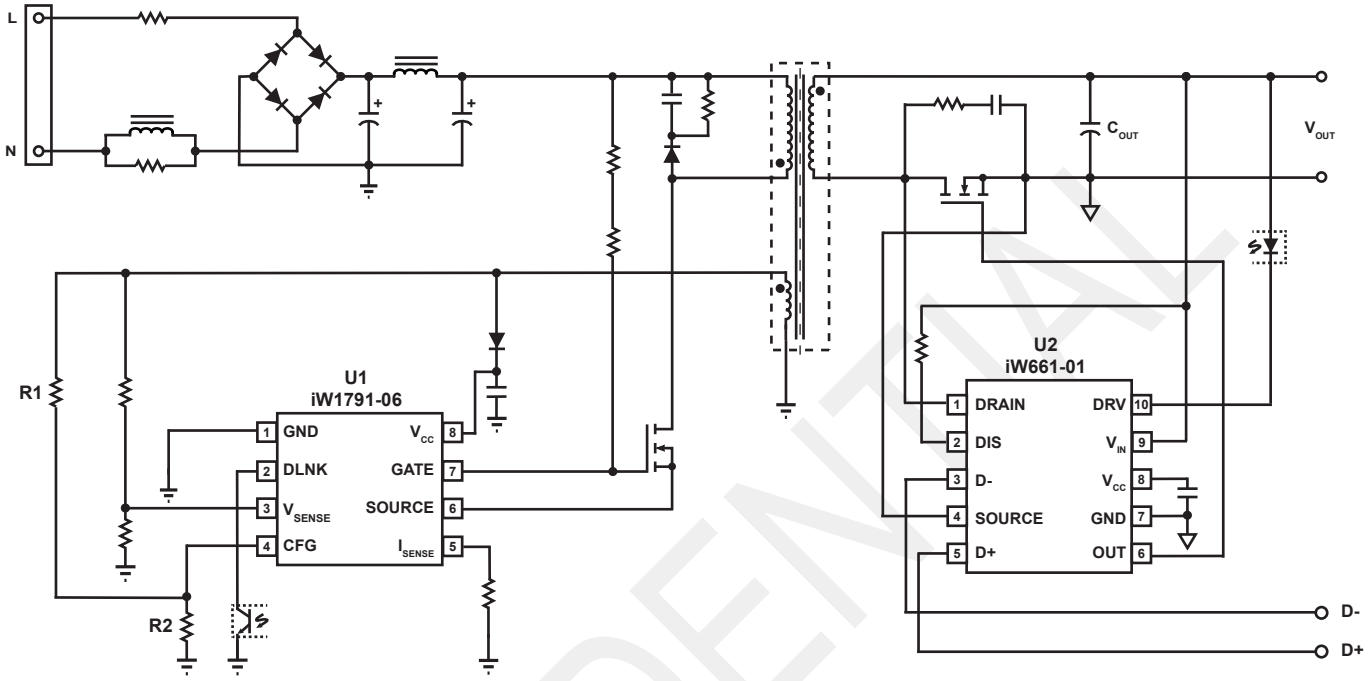


Figure 3.1 : iW661 15W Typical Application Circuit for Multi-Level Output Voltage and Current (Using iW1791 as Primary-Side Controller. Achieving < 20mW No-Load Power Consumption.)

4 Pinout Description

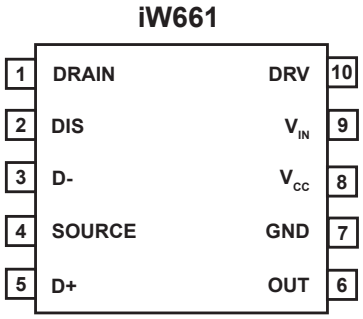


Figure 4.1 : 10-Lead MSOP Package

Pin No.	Pin Name	Type	Pin Description
1	DRAIN	Analog Input	Synchronous rectifier MOSFET drain voltage sensing and the Pulse Linear Regulator (PLR) input.
2	DIS	Analog Output	Discharging circuit. Used for fast discharging of output capacitor.
3	D-	Analog Input	USB D- signal.
4	SOURCE	Analog input	Synchronous rectifier MOSFET source voltage sensing input.
5	D+	Analog Input	USB D+ signal.
6	OUT	Output	Synchronous rectifier MOSFET driver.
7	GND	Ground	Ground.
8	V_{CC}	Power Input	LDO and PLR output. Connect this pin to a capacitor.
9	V_{IN}	Analog Input	Input of the internal LDO and output voltage sensing circuit. Connect to adapter/charger output for bias voltage. The internal LDO clamps the V_{CC} voltage at 5V when V_{IN} > 5V.
10	DRV	Analog Output	External circuit drive. Can be used for optocoupler LED drive with automatic current limiting for transmiting signals to primary side.

5 Absolute Maximum Ratings

Absolute maximum ratings are the parameter values or ranges which can cause permanent damage if exceeded. For maximum safe operating conditions, refer to Electrical Characteristics in Section 6.

Parameter	Symbol	Value	Units
V_{IN} DC supply voltage range (I_{CC} = 15mA max)	V_{IN}	-0.3 to 33	V
Continuous DC supply current at V_{IN} pin (V_{IN} = 25V)	I_{VO}	15	mA
Continuous DC supply current at V_{CC} pin (V_{CC} = 5.5V)	I_{VCC}	15	mA
Gate peak output current	I_G	±3	A
DRAIN pin voltage (Note 1)	V_D	-1.5 to 100	V
DRAIN pin peak current	I_{DRAIN}	-40 to 350	mA
SOURCE pin voltage		-0.6 to 5	V
OUT pin voltage	V_{OUT}	-0.6 to V_{CC} +0.6	V
V_{CC} pin voltage	V_{CC}	-0.6 to 6	V
DIS pin voltage	V_{DIS}	30	V
DRV pin voltage	V_{DRV}	30	V
D+ pin voltage (Note 2)	V_{D+}	-0.3 to 10	V
D- pin voltage (Note 2)	V_{D-}	-0.3 to 10	V
Junction temperature	T_J	-40 to 150	°C
Storage temperature		-65 to 150	°C
ESD rating per JEDEC JS-001-2017 (D+ and D- pins)		± 6,000	V
ESD rating per JEDEC JS-001-2017 (all other pins)		± 2,000	V

Notes:

Note 1: The DRAIN pin voltage should not be below -0.6V for more than 500ns.

Note 2: The D+ and D- pins should not be above 7V for more than 10ms. A minimum of 50Ω series resistance is recommended if the voltage on the D+/D- lines could exceed 7V.

6 Electrical Characteristics

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{CC} Power Blocks						
Switching between LDO and PLR						
PLR disable rising threshold at V_{IN} pin	$V_{LR\_DISABLE}$		4.2	4.45	4.7	V
PLR enable falling threshold at V_{IN} pin	V_{LR_ENABLE}		3.85	4.07	4.25	V
LDO						
DC input voltage (Note 2)	$V_{IN\_DC\_MAX}$				25	V
DC regulation voltage	V_{CC_LDO}	V_{IN} = 6V, I_{LDO} = 5mA	4.7	5	5.35	V
Pulse Linear Regulator (PLR)						
Regulated output voltage at V_{CC}	V_{PLROUT}	10mA Loading at V_{CC}		5		V
Bias Voltage Supply						
DC supply operating voltage (Note 2)	V_{CC}				5.5	V
Bias current	I_{CC_BIAS}	OUT pin floating, 50kHz		1.2		mA
Bias current, no load	I_{CC_NL}	OUT pin floating, 1kHz		0.8		mA
UVLO at V_{CC} Pin						
V_{CC} POR threshold	V_{CC_POR}	Voltage applied on V_{CC}, V_{IN} floating		3.1		V
V_{CC} UVLO threshold	V_{CC_UVLO}	Voltage applied on V_{CC}, V_{IN} floating		2.75		V
Synchronous Rectifier Blocks						
Gate pull-up resistor	R_{UP}			4		Ω
Gate pull-down resistor	R_{DOWN}			2		Ω
Gate output high voltage (Note 1)	V_{G_H}			V_{CC}-0.2		V
Gate output low voltage (Note 1)	V_{G_L}			0.15		V
Gate rising time (Note 1)	t_{G_RISE}	1V to 4V, 3.3nF		44		ns
Gate falling time (Note 1)	t_{G_FALL}	4V to 1V, 3.3nF		31		ns
SR function enable threshold, at V_{IN} pin	V_{SR_ENABLE}		2	2.2	2.5	V
SR function enable hysteresis, at V_{IN} pin	$V_{SR\_ENABLE\_HYS}$		0.15	0.18	0.24	V

6 Electrical Characteristics (continued)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Turn-on threshold	V_{ON_TH}		-150	-120	-80	mV
Turn-off threshold, initial	$V_{OFF\_TH\_INIT}$			0		mV
Minimum off delay comparator threshold	$V_{MIN\_OFF\_TH}$			0.7		V
Minimum on time	t_{ON_MIN}		0.7	0.8	0.9	µs
Minimum off time, initial (Note 1) (Note 3)	$t_{OFF\_MIN\_INIT}$		2.2	2.5	2.8	µs
Protocol Blocks						
Protocol function enable threshold, at V_{IN} pin	V_{PR_ENABLE}		2.8	3.1	3.4	V
Protocol function disable threshold, at V_{IN} pin	$V_{PR\_DISABLE}$		2.6	2.9	3.2	V
Discharge/UV/OV Thresholds						
Threshold to end fast discharge (Note 1)	$V_{IN(DIS)}$	V_{IN} ≤ 5V		+10		%
		V_{IN} > 5V		+12		%
Under-voltage threshold	$V_{IN(UV)}$	V_{IN} = 5V	-6	-5	-4	%
		V_{IN} = 9V/12V	-7	-6	-4	%
		All other voltages	-8	-7.5	-5	%
Over-voltage threshold	$V_{IN(OV)}$	V_{IN} ≤ 5V		6.17		V
		V_{IN} > 5V		+23		%
DRV SECTION (Pin 10)						
DRV pin sink current	I_{DRV}		2	2.6	10	mA
DIS SECTION						
DIS pin sink current (Note 2)	I_{DIS}	On state			500	mA
D+ and D- SECTION						
Data detection voltage (D+ only)	V_{DAT_REF}		0.25	0.35	0.4	V
V_{OUT} selection reference	V_{SEL_REF}		1.8	2	2.2	V
D+ to D- resistance when shorted	R_{DCP_DAT}	D+ = D- = 0.6V	9	17	35	Ω
D+ pull-down resistance	$R_{DAT\_LKG\_DP}$	After POR		400		kΩ
D- pull-down resistance	R_{DM_DWN}			19.53		kΩ
D- AFC T_X voltage source	V_{TX_SRC}		1.6	1.8	2	V
D- AFC R_X logic high threshold	V_{RX_VIH}		1.15	1.25	1.35	V
D- AFC R_X logic low hysteresis	$V_{RX\_VI\_HY}$			0.14		V
D- AFC R_X logic low threshold	V_{RX_VIL}		1.05	1.15	1.25	V

6 Electrical Characteristics (continued)

V_{CC} = 5V, -40°C ≤ T_A ≤ 85°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
D- AFC T_X logic high threshold	V_{TX_VOH}		1.4	1.8	2.2	V
D- AFC T_X logic low threshold	V_{TX_VOL}		0	0	0.3	V
D+ OVP threshold	V_{DP_OVP}			4.5		V
D- OVP threshold	V_{DM_OVP}			4.5		V
D- to GND low impedance threshold (Note1)	R_{DM_FAULT}	When D- is not connected with R_{DM}	250		410	Ω
TIMING SECTION (Pin 3)						
New voltage request interval (Note 1)	$T_{V\_NEW\_REQUEST}$	When not at continuous mode	200			ms
AFC D- signal de-glitch filter (Note 1)	T_{GLITCH_AFC}			5		us
Slave ping-to-ping pulse width variation during one AFC protocol (Note 1)	$t_{SPING\_VARIATION}$				10	us
Glitch filter timer for D+ staying between V_{DAT_REF} and V_{SEL_REF} before D+/D- short switch is turned off (Note 1)	$T_{GLITCH\_BC\_DONE}$			1.25		s
Low V_{OUT} Pre-load SECTION						
Pre-load enable threshold (based on requested voltage) (Note 1)	$V_{PRE-LOAD}$			4.8		V
Pre-load resistor	$R_{PRE-LOAD}$		800	1000	1400	Ω
THERMAL CHARACTERISTICS						
Over-temperature threshold after startup (Note 1)	T_{OT}			140		°C
Over-temperature threshold hysteresis (Note 1)	T_{OT_HYS}			20		°C
Over-temperature threshold at startup (Note 1)	T_{OT_ST}			120		°C

Notes:

Note 1: These parameters are not 100% tested. They are guaranteed by design and/or characterization.

Note 2: The parameters are recommended maximum operation range of the pin.

Note 3: It is the initial minimum off time at POR. The minimum off time adaptively changes based on the system operation. Refer to Section 9 for details.

7 Typical Performance Characteristics

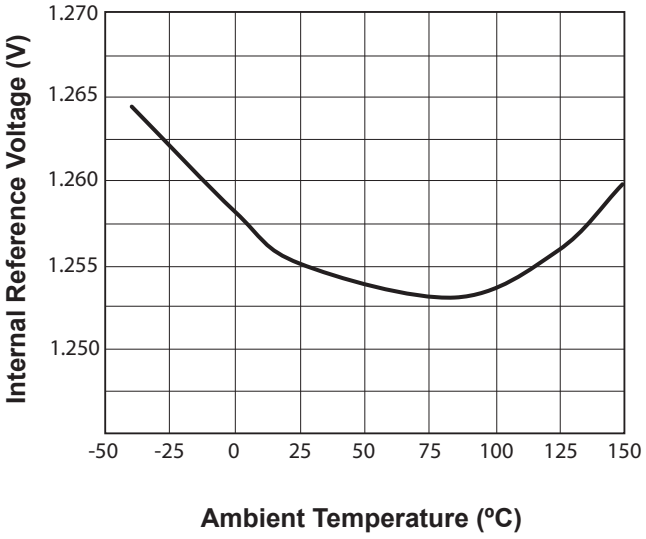


Figure 7.1 : Internal Reference Voltage vs. Ambient Temperature

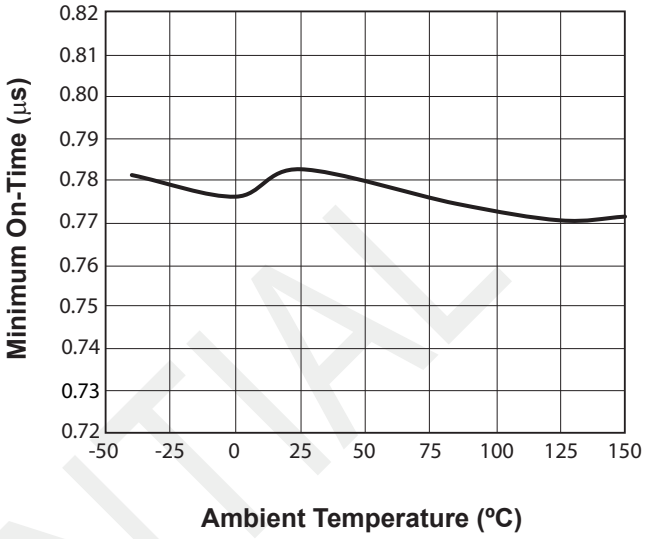


Figure 7.2 : Minimum On-Time vs. Ambient Temperature

8 Functional Block Diagram

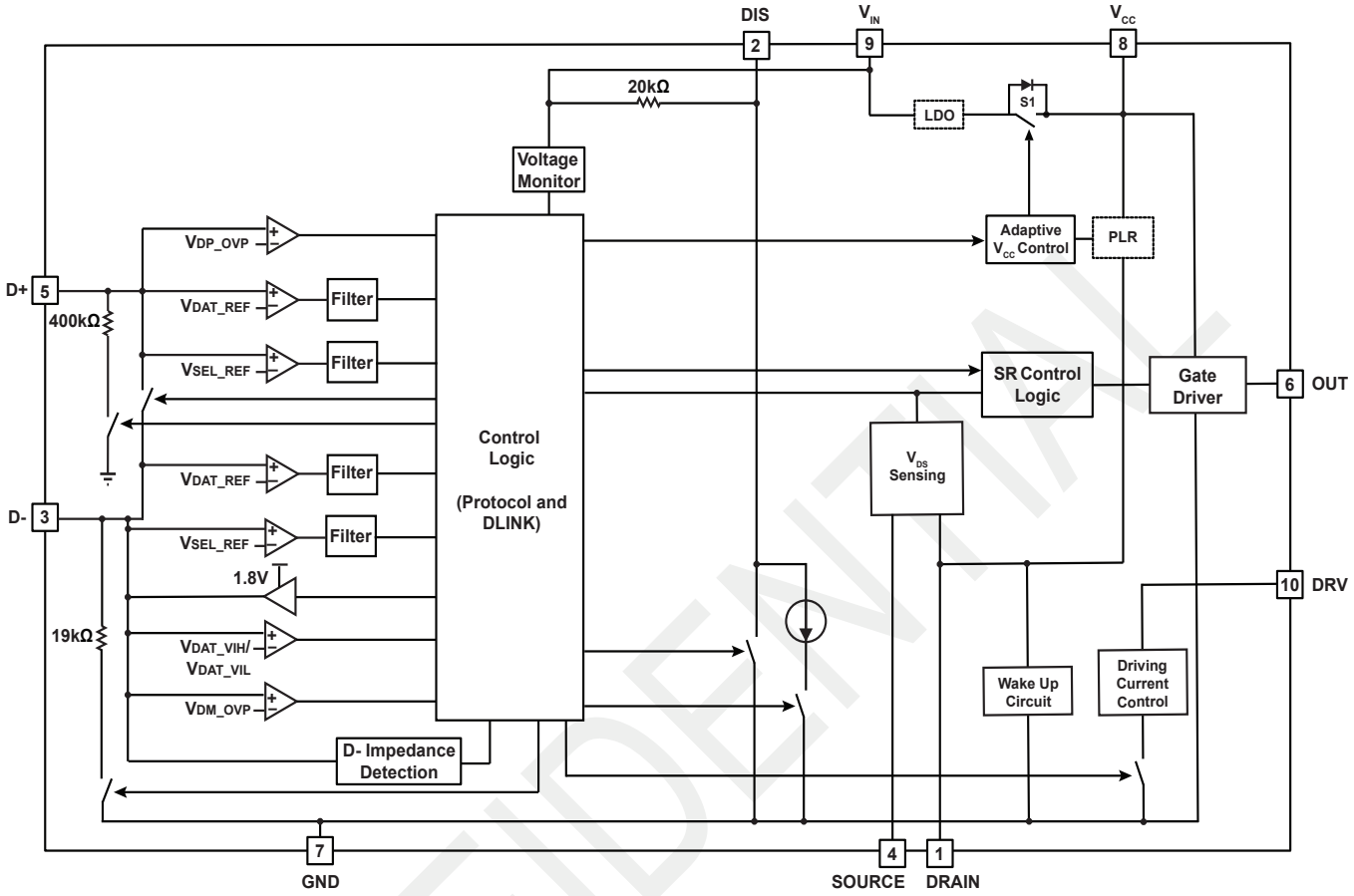


Figure 8.1 : iW661 Functional Block Diagram

9 Theory of Operation

The iW661 is an AC/DC secondary-side combo controller for synchronous rectifier control, secondary-primary communication and AFC protocol interfacing with MDs equipped with AFC technology to configure the travel adapter (TA) output voltage and current limit to different levels for rapid charging. It provides high-performance and cost-effective rapid charge solutions by integrating all secondary-side control functions into one single controller.

The iW661 is also backward compatible with USB BC1.2 compliant MDs and other MDs to provide a 5V/2A output by default setting. The iW661-11 also supports the QC 2.0 protocol. The iW661 can be detected as a DCP if an AFC-equipped MD is connected. After the initial detection stage, the iW661 interprets D+/D- signal voltage to be AFC device and reads its associated output voltage/current requests. A valid request is encoded to certain pulse patterns and sent to the primary side. The constant current (CC) limit setting is also sent together with the voltage request. Besides the voltage and current information, the iW661 also monitors the adapter output voltage and sends over-voltage or under-voltage information to primary side. The iW661 also features a programmable fast/slow active discharging function to discharge the output capacitor in a short time after a request for a lower voltage or unplug of AFC-equipped MDs.

With Dialog's proprietary secondary-side to primary-side digital communication technology and protocol, the iW661 can send various information through the optocoupler, including voltage/current requests, under-voltage, over-voltage and other requests. With this innovative technology and the primary feedback technology, any travel adapter using the

iW661 and iW1791 as secondary and primary controllers can use one of optocouplers to provide higher power density, lowest cost solutions without sacrificing the system performance.

The iW661 should be paired with Dialog's primary-side controller, iW1791, for dynamic multi-level voltage and current configuration and control. The iW1791 has a built-in circuit to decode the different pulse patterns for voltage configuration, current limit setting, V_{OUT} under-voltage and over-voltage detection, and the iW1791 responds accordingly based on the decoded information.

The iW661 builds in the synchronous rectifier (SR) control function with a MOSFET driver that uses a new, proprietary digital adaptive turn-off control technology to minimize the turn-off deadtime. This results in a lower diode conduction loss at the deadtime so that no parallel Schottky diode is required. It measures the voltage across the synchronous MOSFET to achieve lossless current sensing for the driver timing control. The digital SR logic control block generates the gate driver control signal based on the drain-to-source voltage of the synchronous MOSFET. The gate driver control signal is fed into the integrated MOSFET driver to drive the synchronous MOSFET.

The iW661 SR control and driver is optimized for high efficiency operation of multi-level output systems up to 12V with a minimum of external components. The DRAIN pin of the iW661 has a 100V rating to support high output voltage without the need of an additional clamping circuit. The PLR circuit controlled by the adaptive V_{CC} control block is built in to provide sufficient SR MOSFET driving voltage for high efficiency SR operation at output voltages down to the sub-3V level.

9.1 Pin Detail

Pin 1 – DRAIN

Synchronous MOSFET drain voltage sensing, Pulse Linear Regulator (PLR) input and wakeup circuit output. Connect this pin as close to the drain of the MOSFET as possible to avoid noise picked up from the traces.

A 20Ω resistor is recommended between MOSFET and the pin to limit the negative current within -40mA.

Pin 2 – DIS

Programmable active discharge. This pin provides fast and slow discharge paths for the external circuit, such as an output capacitor. When there is a request for a lower voltage or the USB MD is unplugged at a high voltage, the internal active discharge switches are turned on.

Pin 3 – D-

USB D- signal.

Pin 4 – SOURCE

Synchronous MOSFET source voltage sensing. Connect this pin as close to the source of the MOSFET as possible to avoid noise picked up from the traces.

Pin 5 – D+

USB D+ signal.

Pin 6 – OUT

Gate drive for the external synchronous MOSFET switch.

Pin 7 – GND

Ground.

Pin 8 – V_{CC}

Output of Pulse Linear Regulator and the internal linear regulator. It provides bias voltage for the controller. A capacitor (typical 4.7µF) must be connected between the V_{CC} pin and GND.

Pin 9 – V_{IN}

Internal linear regulator (LDO) input. Connect this pin to the flyback output. The internal linear regulator output is internally connected to V_{CC} through a MOSFET (S1 in Figure 4).

This pin is also the input of some comparators for control purposes.

Pin 10 – DRV

External circuit drive. This pin drives the external circuit, such as the optocoupler, to send out all the information for rapid charge. The DRV pin sink current at ON state is limited to a range such that a low-cost optocoupler can be used.

9.2 Initialization and Handshaking

An AC/DC power adaptor designed with the iW1791 and iW661 starts up initially at a default 5V/2A state. When the output voltage of the AC/DC adapter, which is also the V_{IN} voltage for the iW661, is above V_{PR_ENABLE}, and the V_{CC} voltage for the iW661 is above V_{CC_POR}, the iW661 begins to work at 5V state and the D+/D- short switch is turned on. The USB BC1.2 or AFC-enabled MD detects the D- voltage while applying a voltage on D+ and vice versa. The iW661 is designed such that the impedance between D+ and D- is low enough to meet the specifications of USB BC1.2 and AFC during the initial detection when the D+/D- short switch is on. The iW661 ensures that D+ stays between V_{DAT_REF} and V_{SEL_REF} for at least 1.25 second without any glitch before it turns off the D+/D- short switch and turns on the D- pull-down switch. The handshaking between the iW661 and AFC-equipped MD finishes after D- is pulled down for 20ms and the iW661 starts to take voltage requests from the MD.

9.3 Output Cable Soft Short Detection and MD Fault Code Protection

The iW661 features proprietary D- impedance detection and D+/D- OVP, which address soft short issues in the output cables and connectors and provides protection against damages. During IC initialization and handshaking with MD, the iW661 checks for an output soft short by checking the equivalent resistance at D-. At power-up, the iW661 detects the equivalent resistance at D- immediately after V_{CC} rises above V_{CC_POR} and V_{IN} rises above V_{PR_ENABLE}. This detection happens when the TA is plugged to the wall outlet while the MD can be attached or detached to the TA. The iW661 sends out a signal to the iW1791 if the equivalent resistance on D- is detected to be less than 410Ω. When the D+ voltage is below $V_{DAT\text{-}REF}$, D- impedance detection happens periodically every 2.2 seconds.

When the iW661 detects D+/D- OVP or receives a fault code from the MD, it sends out a signal to the iW1791 to shut down the TA.

9.4 Voltage and Current Request Interpretation and Encoding

After handshaking with the MD, the iW661 monitors the voltage changes of D+ and D-. If there is a valid signal pulse qualified as a Master Ping of AFC protocol, the iW661 responds with a Slave Ping and receives the incoming signals for voltage and current information. If the incoming signal is qualified as a valid AFC voltage/current request, the iW661 enters AFC mode and repeats the same pattern to inform the MD that this voltage/current request can be supported. Such a two-way request/response is repeated twice more (total of three rounds) before the iW661 sends out voltage/current request to the iW1791. The iW1791 changes the voltage regulation and current limit accordingly. If the MD requested a voltage/current setting which cannot be supported by iW661, the iW661 responds with all the supported voltage/current combinations to the MD. The supported voltage/current configurations and V_I_BYTEs for the iW661-01 option are listed in table 9.1. For availability of other product options to support more voltage/current combinations, please contact Dialog.

V_{BUS}	AFC Mode		
	AFC V_I_Byte (HEX)	Voltage/Current Request from MD	Actual Output Voltage/ Current
5V	08	5V/2A	5V/2A
9V	46	9V/1.67A	9V/1.67A

Table 9.1: Supported Output Voltages/Currents and V_I_BYTES in iW661-01

After initialization and handshaking with MD, if there is a D+/D- combination change, and the D+/D- voltage combination is a valid QC2.0 request and passes the 40ms deglitch filter, the iW661-11 enters QC2.0 mode. The iW661-0X options do not support QC 2.0.

The iW661-11 interprets the D+/D- combination according to QC2.0 specification. The interpretation of D+/D- combination and the voltage requests are listed in Table 9.2.

Please note that a voltage at D+ or D- is detected as:

a) 0V, if it is lower than V_{DAT_REF};

b) 0.6V, if it is between V_{DAT_REF} and V_{SEL_REF};

c) 3.3V, if it is higher than V_{SEL_REF}.

D+	D-	V_{OUT}
0.6V	0.6V	9V
3.3V	0.6V	9V
0.6V	0V	5V
0V	0/0.6/3.3V	5V
All other combinations		Stays unchanged

Table 9.2: D+/D- Signals and Adapter V_{OUT} (aka V_{BUS}, V_{CC})

The iW1791 uses the patented primary-feedback control to achieve the multi-level constant-voltage and multi-level CC regulations. The CC limit is given by

$$I_{CC\_LIMIT} = 0.4\,k_{CC} \times \frac{N}{R_S} \times \eta_x \qquad (9.1)$$

where N is the transformer primary to secondary side winding turns ratio, R_S is the current sense resistor, η_X is the transformer conversion efficiency, and k_{CC} is a coefficient set by the iW661 (see Section 11 for pre-defined k_{CC} information).

The iW661 has a built-in encoder to generate different patterns and to drive the SR MOSFET so that the different voltage information together with the associated current limit setting can be sent to the primary side through the power transformer.

9.5 Programmable Active Discharge

Discharge of the output capacitor is necessary for quick voltage transition from a higher level to a lower level when there is a lower voltage request. It is even more important to discharge the output capacitor quickly from a high level to 5V after the MD is unplugged from the TA in order to ensure the safety of other non-AFC-enabled MDs. An internal switch between the DIS pin and GND pin is turned on to provide a path from the output voltage through an external

resistor, the DIS pin, and the internal switch to ground. The discharging time is programmable with the external resistor. A resistance of 47Ω or higher is recommended for the external resistor to prevent over-current or over-heat inside the IC. If a certain application uses a larger output capacitor or requires faster discharging, an external P-channel FET can be used and the iW661 DIS pin can be used to drive the FET. When the MD is unplugged, the iW661 resets to its initial setting. The active fast discharge starts after a confirmed lower voltage request or after 40ms de-glitch of D+ voltage drop; it stops when the active discharge threshold of target voltage is reached or a 200ms timer (including de-glitch time) expires to avoid excess load current and high power dissipation inside the IC. After the active fast discharge stops, a slow discharge path continues to discharge the output capacitor until the 200ms timer expires.

9.6 V_{BUS} Monitoring

In addition to encoding and transmitting the output voltage and current request, the iW661 monitors the V_{BUS} for both under-voltage and over-voltage. The V_{BUS} under-voltage or voltage undershoot is usually caused by a sudden load current increase. The iW661 also monitors the V_{BUS} over-voltage, especially the over-voltage caused by the output voltage setting mismatch between the iW1791 and iW661.

When a load transient event from light load to heavy load happens, the output voltage drops. If the output voltage drops to the voltage undershoot threshold, the iW661 turns on the LED of the optocoupler by controlling the DRV pin sink current, and the DLNK pin of the iW1791 is pulled down by the transistor of the optocoupler. After the iW1791 receives this DLNK pin signal, it can intelligently confirm if this signal is caused by an undershoot event and distinguish it from a voltage and current request, and then it promptly increases the switching frequency and the t_{ON} to delivery more power to the secondary side in order to bring the output voltage back to regulation. The undershoot detection signal of the iW661 is backward compatible with Dialog's secondary-side voltage position monitor, the iW628.

While the iW1791 can protect against the V_{BUS} over-voltage through the V_{SENSE} signal in most condtions, it is difficult for the iW1791 to protect the over-voltage caused by output voltage setting mismatch between the iW1791 and the iW661. The iW1791/iW661 chipset adds one more layer of OVP. When the V_{BUS} rises to above the over-voltage threshold of the iW661's present setting, the iW661 drives the DRV pin in a special switching pattern serving as a OVP signal and turns on both the fast and slow discharge. After the iW1791 receives this OVP signal, it shuts down the power supply promptly.

In this way, through the single optocoupler and proprietary digital communication the iW661 transmits to the iW1791 all the necessary information for a high-performance rapid-charge AC/DC system design including output voltage requests, output current limits, output voltage undershoot and output over-voltage.

V_{CC} Powering in the iW661

Internal circuits of the controller require bias voltage from the capacitor at the V_{CC} pin to operate. The internal linear regulator (LDO) and the internal pulse linear regulator (PLR) are the two power sources available in the iW661 to power V_{CC}. The LDO utilizes the stable system output voltage to power V_{CC} thus it is preferred when the output voltage is sufficiently high to achieve high efficiency driving of the SR MOSFET. However, when the system output voltage drops low, it may not be able to provide sufficient voltage to drive the SR MOSFET efficiently. Thus the PLR circuit is introduced to power V_{CC} under such conditions. The PLR utilizes the pulsating voltage at the SR MOSFET DRAIN pin to power V_{CC} so it can maintain relatively high V_{CC} when the system output voltage drops low.

When the system output voltage is above $V_{LR\_DISABLE}$, the PLR circuit is at the OFF state. The MOSFET (S1) will be at the ON state to minimize the voltage drop between the V_{IN} pin and V_{CC} pin. The flyback system output provides the operating current through the LDO at the V_{IN} pin into the V_{CC} pin. The LDO regulates the V_{CC} voltage at 5V. When the flyback output is close to 5V, the LDO cannot maintain V_{CC} regulation and it operates at pass through mode. In this mode the drop-out voltage from the V_{IN} pin to V_{CC} pin is smaller than 0.4V when the V_{IN} pin current is 5mA.

When the system output voltage drops below the V_{LR_ENABLE}, the adaptive V_{CC} control chooses either the LDO or the PLR to obtain high enough V_{CC} based on the system operation condition. If the PLR is set to the ON state, the PLR will provide power to V_{CC} and the V_{CC} voltage may go higher than the system output voltage at the V_{IN} pin. The switch S1

will be at the OFF state to avoid current going from the V_{CC} pin to the V_{IN} pin. Although the switch S1 is turned off, the LDO may still be able to charge the capacitor at V_{CC} through the body diode of S1 if the V_{CC} voltage is below V_{IN}.

With this scheme, the iW661 always maintains sufficient V_{CC} voltage to drive the SR MOSFET under all output voltage and loading conditions. Thus it is optimized for multi-level output applications.

9.7 V_{DS} Sensing and Synchronous Rectifier Driving Scheme

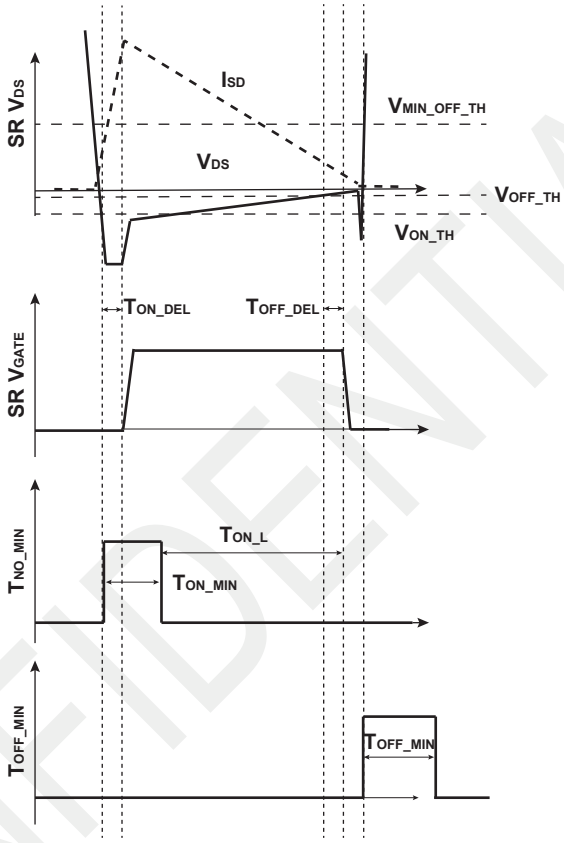


Figure 9.2 : SR Control Block Sequencing Diagram

The synchronous rectifier (SR) control block monitors the synchronous MOSFET's drain-to-source voltage (V_{DS}) to determine the driver timing. When the V_{DS} is below the V_{ON_TH} (-120mV), the control block turns on the synchronous MOSFET with its built-in driver. The driver has a minimum on-time (T_{ON_MIN}) to avoid the noise from turning off the driver immediately.

As the current I_{SD} decreases, V_{DS} increases and gets close to 0 mV. The SR driver is turned off when the V_{DS} reaches V_{OFF_TH}. The iW661 builds in Dialog's proprietary adaptive turn-off technology to minimize the turn-off deadtime.

After the SR driver turns off, the V_{DS} rises. When the V_{DS} reaches $V_{MIN\_OFF\_TH}$, the SR control block initiates a minimum off-time timer during which the SR remains off to avoid the ringing from turning on the synchronous MOSFET. The drain-to-source voltage of the synchronous MOSFET has a ringing after the secondary current reaches zero, which is caused by the magnetizing inductance of the transformer and the parasitic capacitances of the MOSFETs and the transformer. Depending on the damping factor, this ringing may reach the turn-on threshold of iW661 in its first ringing cycle. The initial T_{OFF_MIN} is designed to be 2.5µs to prevent the ringing from turning on the synchronous MOSFET. In typical 10W to 25W designs, the ringing frequency is between 500kHz and 1MHz. Thus the 2.5µs T_{OFF_MIN} is long enough to cover the first ringing cycle. The iW661 measures the ringing frequency and adaptively adjusts the T_{OFF_MIN}

to effectively block the first ringing cycle.

If the T_{ON_L} in Figure 9.2 is smaller than 100ns, the following T_{OFF_MIN} is doubled.

During the start-up, the system output voltage may be too low to reset the transformer so that the system may operate at the Continuous Current Mode (CCM). To avoid the SR operation at CCM, a comparator at V_{IN} pin monitors the system output. When V_{IN} voltage is lower than 2.2V (typical), the whole SR control block is disabled.

9.8 Design Considerations

To increase D+/D- noise immunity, RC filters can be added to D+/D- traces or pins as shown in Figure 9.3. Since the AFC specification requires the capacitance from D+ or D- to GND to be less than 500pF and iW661 D+/D- pins can have up to 100pF internal capacitance, the maximum external capacitance on D+ or D- can be 400pF each. The USB BC1.2 requires a maximum of 200Ω of D+ to D- resistance during DCP mode while the iW661 has internal resistance up to 22Ω when D+ and D- are shorted internally. The maximum total resistance for R_{DP} and R_{DM} is 178Ω so that R_{DP} or R_{DM} can be up to 89Ω each.

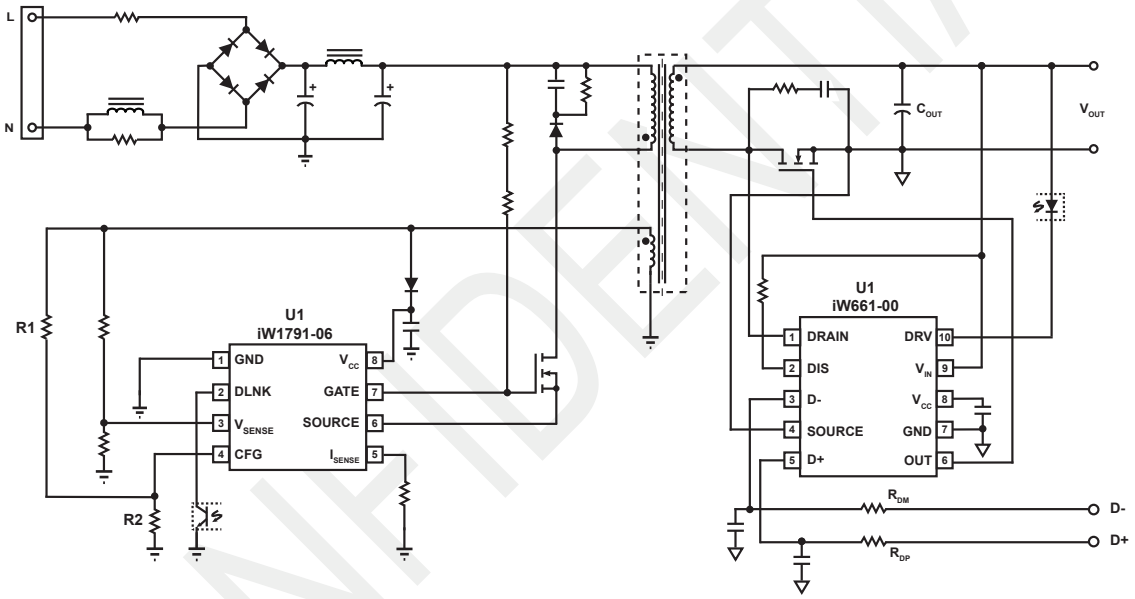


Figure 9.3 : iW661 Typical Application Circuit for Multi-Level Output Voltage and Current with RC Filtering at D+/D-. (Using iW1791-06 as Primary-side Controller. Achieving <20mW No-Load Power Consumption).

9.9 Layout Considerations

Since the iW661 integrates the SR function and protocol function, layout is very critical to guarantee correct operation of all functions. In order to minimize the SR sensing and driving noise, the trace between the MOSFET and the output capacitor, and the trace between the iW661 GND pin and the output capacitor should both be as short as possible. If both traces are very short, it is ok to directly connect the SOURCE and GND pins of iW661 together near the IC, as shown in Figure 9.4.

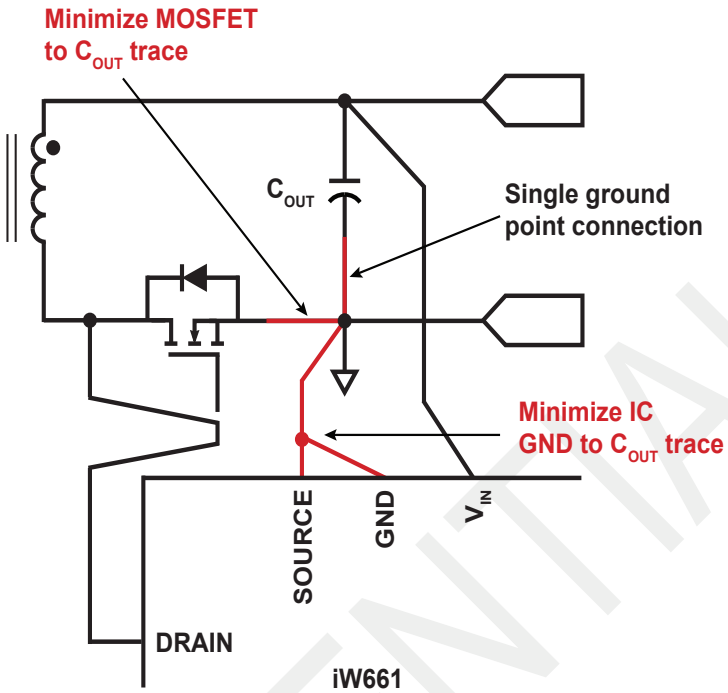


Figure 9.4 : PCB layout recommendation when the SR MOSFET, output capacitor and iW661 can be physically as close as possible with minimum length trace connections.

If the traces have to be long due to the physical placement, the PCB layout connection shown in Figure 9.5 is recommended. The trace between the MOSFET and the output capacitor should be still as short as possible. The SOURCE and GND pins should be connected separately to the MOSFET source and output capacitor.

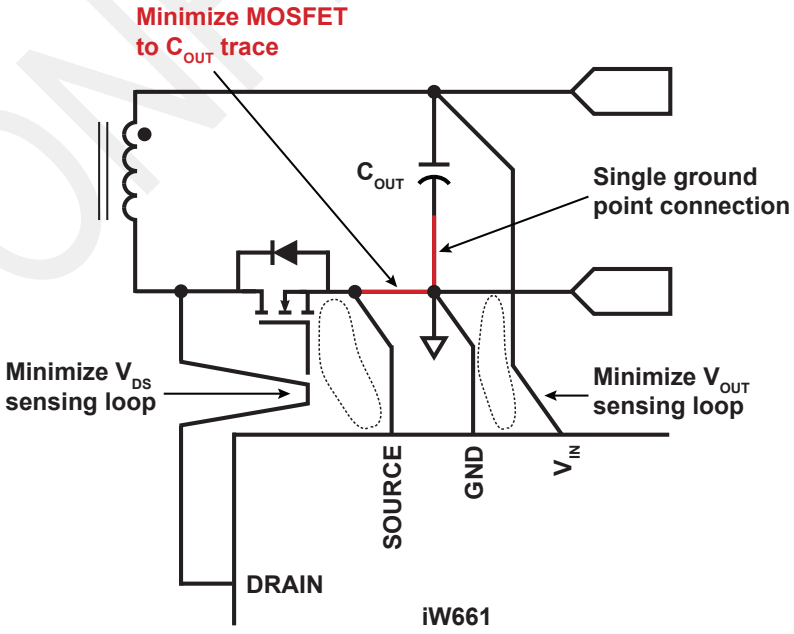
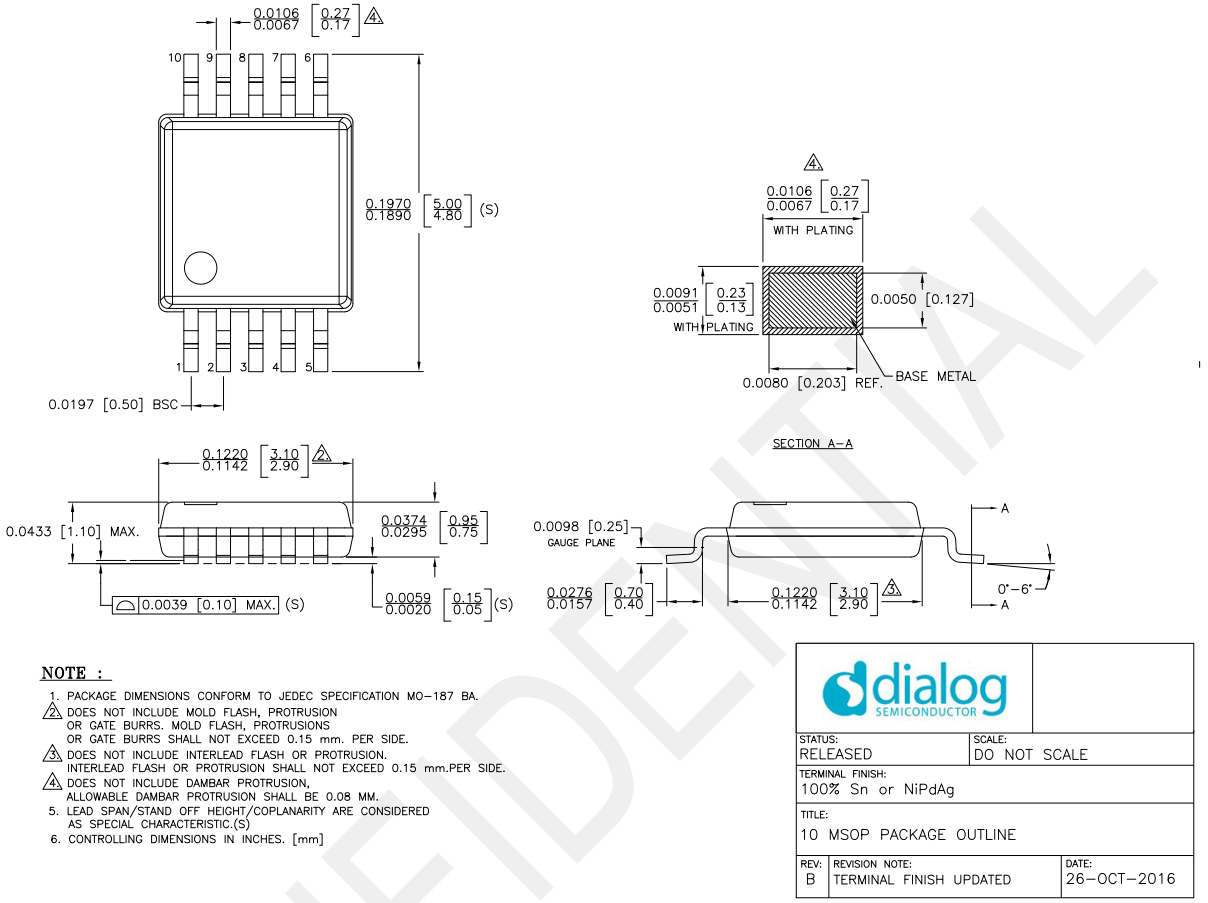


Figure 9.5 : PCB layout recommendation when iW661 cannot be too close to the MOSFET and output capacitor.

10 Physical Dimensions



NOTE :

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MO–187 BA.
2. DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 mm. PER SIDE.
3. DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 mm.PER SIDE.
4. DOES NOT INCLUDE DAMBAR PROTRUSION, ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 MM.
5. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)
6. CONTROLLING DIMENSIONS IN INCHES. [mm]

STATUS: RELEASED	SCALE: DO NOT SCALE
TERMINAL FINISH: 100% Sn or NiPdAg	
TITLE: 10 MSOP PACKAGE OUTLINE	
REV: B	REVISION NOTE: TERMINAL FINISH UPDATED
	DATE: 26–OCT–2016

11 Ordering Information

Part no.	Options				Package	Description
	Protocol and V/I Profile	k_{CC} at 2A/1.67A	Primary-Side Controller	D- Detection at D+ Falling Edge and after BC1.2		
iW661-00	15W AFC: 5V/2A, 9V/1.67A	0.5/0.422	iW1791-06	Enabled	MSOP-10	Tape & Reel[1]
iW661-01	15W AFC: 5V/2A, 9V/1.67A	0.5/0.422	iW1791-06	Disabled	MSOP-10	Tape & Reel[1]
iW661-11	15W AFC/QC 2.0 5V/2A, 9V/1.67A	0.5/0.422	iW1791-06	Disabled	MSOP-10	Tape & Reel[1]

Note 1: Tape & Reel packing quantity is 2,500/reel. Minimum packing quantity is 2,500.

12 Top Marking

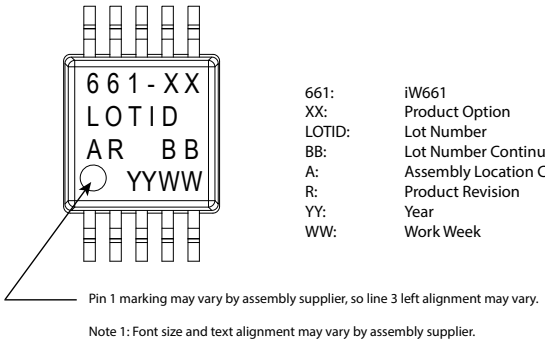


Figure 12.1 : Top Marking for the iW661